DOCUMENT CHANGE REQUEST

DCR number 637	Changes required for: General	Originator: S Jeffery
Date: 2010/12/15	Date sent: 2010/12/15	Organisation:
Status: IMPLEMENTED		

Title:	Integrated Circuits, Monolithic, CMOS Silicon on Sapphire 3.5 GHz Delta-Sigma Modulated		
Number:	9202/077	Issue:	1

Other documents affected:

Page:

Para 1.9 (Pages 11, 12); Para. 1.10.2.2 (Page 13); Para. 1.10.5 (Page 16); Para. 2.3.1 (Pages 19, 22, 23, 26, 28, 29); Para. 2.8.1 (Page 35)

See attached mark-up of 9202/077 Issue 1 for details.

Paragraph:

Para 1.9 (Pages 11, 12); Para. 1.10.2.2 (Page 13); Para. 1.10.5 (Page 16); Para. 2.3.1 (Pages 19, 22, 23, 26, 28, 29); Para. 2.8.1 (Page 35)

See attached mark-up of 9202/077 Issue 1 for details.

Original wording:

Proposed wording:

ESCC 9202/077 Issue 1 contains a number of editorial errors, shown below, which require correction.

Para. 1.9 Pin Assignment and Description - the Description of Pin No. 65 includes the text "...register bit s are..."; this requires correcting to "...register bits are..."

Para. 1.9 Pin Assignment and Description - Note 2, Table, Group No. 6: Pin Number 50 is currently (Cext), should be (CEXT)

Para. 1.10.2.2 Prescaler Bypass Mode - the 'active low' bar extends beyond the "N" of PRE_EN, this should therefore be corrected

Para. 1.10.5 Phase Detector - "Cext" (in four places) should be "CEXT"

Para. 2.3.1 Room Temperature Electrical Measurements - Test Conditions for Functional Test, Typical Voltage (Relaxed Limits): the "-" should be deleted from "IOL =-0A (Pin Group 7)"

Para. 2.3.1 Room Temperature Electrical Measurements - Parameters IIH_PD and IIH: the Test Conditions currently include "VIN(Under Test)=0V" and "VIN(Remaining Inputs)=3.45V". These need to be corrected to "VIN(Under Test)=3.

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45V" and "VIN(Remaining Inputs)=0V"

Para. 2.3.1 Room Temperature Electrical Measurements - third sentence begins "total..."; this requires correcting to "Total..."

Para. 2.3.1 Room Temperature Electrical Measurements - Note 9, Timing Generator Table, Timing Generator Numbers 8 and 12: Pin Groups "2 and 4" require correcting to Pin Groups "2 and 3"

Para. 2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing - Note 1: "-VCC+AMP=-5V" needs to be corrected to "-VCC_AMP=-5V"

ESCC 9202/077 Issue 1 also contains a few technical errors (incorrect convention and polarity for some parameters) which require correcting:

Para. 2.3.1 CMOS Input Leakage Current, Low Level - the limits are currently 15uA min, 50uA max. The correct polarity is -15uA min, -50uA max.

Para. 2.3.1 CMOS Input Leakage Current, High Level (with pull-down) - the limits are currently -75uA min, -30uA max. The correct convention and polarity is 30uA min, 75uA max.

Para. 2.3.1 CMOS Input Leakage Current, High Level - the limits are currently -50uA min, -15uA max. The correct convention and polarity is 15uA min, 50uA max.

Justification:

The changes proposed above will correct editorial and technical errors (some of which are potentially confusing) in ESCC 9202/077 Issue 1, and therefore will improve the content and clarity of this Spec.

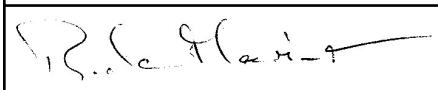
Attachments:

9202077_Issue_2_Draft_A.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2010-12-15

European Space Components Coordination

Pages 1 to 37

INTEGRATED CIRCUITS, MONOLITHIC, CMOS SILICON ON SAPPHIRE, 3.5GHZ DELTA-SIGMA MODULATED FRACTIONAL-N PLL FREQUENCY SYNTHESIZER

BASED ON TYPE PE33632

ESCC Detail Specification No. 9202/077

as applicable

Issue 2	November 2010

Document Custodian: European Space Agency - see https://escies.org

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
tba	Specification upissued to incorporate editorial and technical changes per DCR.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
48	$\overline{FIN}$	Input	RF	Both	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor directly to the ground plane.
49	V_{SS}	Ground	-	-	V_{SS}
50	CEXT	Output	CMOS (high resistance)	Both	Logical "NAND" of PD_U and PD_D terminated through an on-chip, 2kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Output	Open Drain	Both	Lock detect and open drain logical inversion of Cext. When the loop is in lock, LD is high impedance, otherwise LD is a logic "low" ("0").
52	DOUT	Output	CMOS (low current)	Both	Data Out function, enabled in enhancement mode.
53	V_{DD}	Power	-	-	Output driver V_{DD} (Note 1).
54	V_{SS}	Ground	-	-	V_{SS}
55	PD_D	Output	CMOS	Both	PD_D pulses down when f_p leads f_c.
56	NC	-	-	-	Not Connected.
57	PD_U	Output	CMOS	Both	PD_U pulses down when f_c leads f_p.
58	V_{SS}	Ground	-	-	V_{SS}
59	V_{DD}	Power	-	-	Output driver V_{DD} (Note 1).
60	V_{DD}	Power	-	-	Phase detector V_{DD} (Note 1).
Top side					
61	V_{SS}	Ground	-	-	V_{SS}
62	FR	Input	CMOS	Both	Reference frequency input.
63	V_{DD}	Power	-	-	Reference V_{DD} (Note 1).
64	V_{DD}	Power	-	-	Digital core V_{DD} (Note 1).
65	$\overline{ENH}$	Input	CMOS	Both	Enhancement mode. When asserted "low" ("0"), enhancement register ~~bits~~ bits are functional.
66	NC	-	-	-	Not Connected.
67	MS2_SEL	Input	CMOS	Both	MASH 1-1 select. "high" selects MASH 1-1 mode, "low" selects the MASH 1-1-1 mode.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
68	RAND_EN	Input	CMOS	Both	K register LSB toggle enable. "high" enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the Phase Detector comparison frequency / 2^{19}.

NOTES:
1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins (i.e. CMOS inputs of Group 1 below) have a 70kΩ pull-down resistor to ground.

The table below describes the pin groups to be tested.

Group No.	Type	Total No. of Pins	Pin Numbers
1	CMOS Input with Pull-down	42	1 to 8, 11 to 26, 29 to 43, 65, 67 and 68
2	CMOS Input	1	62 (FR)
3	RF Input	2	47 (FIN) and 48 ($\overline{\text{FIN}}$)
4	High Current CMOS Output	2	55 (PD_D) and 57 (PD_U)
5	Low Current CMOS Output	1	52 (DOUT)
6	High Resistance CMOS Output	1	50 (CExt) upper case
7	Open Drain Output	1	51 (LD)
8	Power	9	10, 27, 44, 46, 53, 59, 60, 63 and 64
9	Ground	7	9, 28, 45, 49, 54, 58 and 61

1.10 FUNCTIONAL DESCRIPTION

1.10.1 Overview

The PE33632 consists of a prescaler, several counters, an 18-bit delta-sigma modulator (DSM) and a phase detector. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters "R" and "M" divide the reference and prescaler outputs, respectively, by the integer values stored in a 20-bit register. An additional counter ("A") is used in the modulus select logic. The DSM modulates the A Counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via a three-wire serial bus. There are also various operational and test modes and a lock detect output.

1.10.2 Main Counter Chain

1.10.2.1 Normal Operating Mode

Setting the $\overline{\text{PRE\_EN}}$ control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (f_{in}) by an integer or fractional number derived from the values in the "M", "A" Counters and the DSM input word K. The accumulator size is 18-bit, so the fractional value is fixed from the ratio $K/2^{18}$. There is an additional bit in the DSM that acts like an extra bit (19th bit). This bit is enabled by asserting the pin RAND_EN to "high". Enabling this bit has the benefit of reducing the spurious levels. However, a small frequency offset will occur. This positive frequency offset is calculated with the following equation:

$$f_{offset} = (f_r/(R + 1))/2^{19} \quad (1)$$

All of the following equations do not take into account this frequency offset. If this offset is important to a specific frequency plan, appropriate account needs to be taken.

In the normal mode, the output from the main counter chain (f_p) is related to the VCO frequency (f_{in}) by the following equation:

$$f_p = f_{in}/[10 \times (M + 1) + A + K/2^{18}] \quad (2)$$

$$\text{Where } A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, f_{in} is related to the reference frequency (f_r) by the following equation:

$$f_{in} = [10 \times (M + 1) + A + K/2^{18}] \times (f_r/(R + 1)) \quad (3)$$

$$\text{Where } A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that f_{in} must be greater than or equal to $90 \times (f_r / (R + 1))$ to obtain contiguous channels. The A Counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M Counter with the minimum allowed value of "1" will result in a minimum M Counter divide ratio of "2".

1.10.2.2 Prescaler Bypass Mode

Setting the frequency control register bit $\overline{\text{PRE\_EN}}$ "high" allows f_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A Counter are powered down, and the input VCO frequency is divided by the M Counter directly. The following equation relates f_{in} to the reference frequency (f_r):

$$f_{in} = (M + 1) \times (f_r/(R + 1)) \quad (4)$$

$$\text{Where } 1 \leq M \leq 511$$

In this mode, neither the A Counter nor the K Counter is used and therefore only integer-N operation is possible.

Enhancement Register Programming

Interface Mode	$\overline{ENH}$	Reserved	Reserved	FP Output	Power Down	Counter Load	MSEL Output	FC Output	LD Disable
Serial (2)	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

↑MSB (first in) LSB (last in) ↑

NOTES:

1. Serial data clocked serially on SCLK rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.
2. Serial data clocked serially on SCLK rising edge while E_WR "high" and captured in double buffer on E_WR falling edge.

1.10.4.3 Enhancement Register

The functions of the enhancement register bits are shown below with all bits active "high".

Bit Number	Bit Function	Description
0	Reserved	Reserve bit - program to 0.
1	Reserved	Reserve bit - program to 0.
2	FP Output	Drives the M Counter output onto the DOUT output.
3	Power Down	Power down of all functions except programming interface.
4	Counter Load	Immediate and continuous load of counter programming.
5	MSEL Output	Drives the internal dual modulus prescaler modulus select (MSEL) output onto the DOUT output.
6	FC Output	Drives the reference counter output onto the DOUT output.
7	LD Disable	Disables the LD pin for quieter operation.

1.10.5 Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference Counter (f_c). It has two outputs, namely PD_U and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

For the UP and DOWN mode, PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to $V_{DD}/2\pi$.

PD_U pulses cause an increase in VCO frequency and PD_D pulses cause a decrease in VCO frequency, for a positive Kv VCO.

upper case

A "lock detect" output, LD, is also provided via the pin Cext. Cext is the logical "NAND" of PD_U and PD_D waveforms, which is driven through a serial 2kΩ resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_U and PD_D.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Dynamic Supply Current with Prescaler	$I_{DDOPENA}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	20	45	mA
Dynamic Supply Current without Prescaler	$I_{DDOPDIS}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	8	20	mA
Functional Test, Typical Voltage (Relaxed Limits)	-	3014	V_{DD}=3.3V, V_{SS}=0V V_{IH}=3.3V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=0A (Pin Group 7) C_{LOAD}<62pF Use patterns *main_pattern* (between labels "main_st" and "end_u_d") and *dsm_p1* @10MHz Note 4	Go/NoGo		-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Output Voltage, High Level (High Current Buffer at Minimum V_{DD})	V_{OH1_H}	3006	Pin Group 4 V_{DD}=2.85V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (Low Current Buffer at Minimum V_{DD})	V_{OH1_L}	3006	Pin Group 5 V_{DD}=2.85V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Minimum V_{DD})	V_{OH1_R}	3006	Pin Group 6 V_{DD}=2.85V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (High Current Buffer at Maximum V_{DD})	V_{OH2_H}	3006	Pin Group 4 V_{DD}=3.45V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Low Current Buffer at Maximum V_{DD})	V_{OH2_L}	3006	Pin Group 5 V_{DD}=3.45V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Maximum V_{DD})	V_{OH2_R}	3006	Pin Group 6 V_{DD}=3.45V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Input Leakage Current, Low Level (with Pull-down)	I_{IL_PD}	3009	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-250	250	nA
CMOS Input Leakage Current, Low Level	I_{IL}	3009	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-15	-50	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Input Leakage Current, High Level (with Pull-down)	I_{IH_PD}	3010	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=3.45V V_{IN}(Remaining Inputs)=0V	30	75	µA
CMOS Input Leakage Current, High Level	I_{IH}	3010	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=3.45V V_{IN}(Remaining Inputs)=0V	15	50	µA
High-Impedance Output Leakage Current, High Level	I_{OZH}	3021	Pin Group 7 V_{DD}=3.45V, V_{SS}=0V V_{OUT}=3.45V Use pattern *main_pattern*, stop at label "llzhh" Note 7	-	10	µA
Serial Clock Minimum Pulse Width High (Minimum V_{DD})	t_{CLKH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #35) to negedge SCLK (↓ #35) Use pattern *main_pattern* Note 10	-	30	ns
Serial Clock Minimum Pulse Width Low (Minimum V_{DD})	t_{CLKL1}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge SCLK (↓ #35) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	30	ns
Serial Data to Serial Clock Setup Time (Minimum V_{DD})	t_{DSU1}	3003	V_{DD}=2.85V, V_{SS}=0V From any edge of SDATA (#34) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	10	ns
Serial Data to Serial Clock Hold Time (Minimum V_{DD})	t_{DH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #35) to any edge of SDATA (#34) Use pattern *main_pattern* Note 10	-	10	ns
Serial Load Minimum Pulse Width High (Minimum V_{DD})	t_{PWH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge S_WR (↑ #33) to negedge S_WR (↓ #33) Use pattern *main_pattern* Note 10	-	30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Phase Noise @ 10kHz Offset, Typical Low V_{DD}	$PN_{10K}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-107	-89	dBc/Hz
Phase Noise @ 100Hz Offset, Typical High V_{DD}	$PN_{100}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-95	-83	dBc/Hz
Phase Noise @ 1kHz Offset, Typical High V_{DD}	$PN_{1K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-101	-91	dBc/Hz
Phase Noise @ 10kHz Offset, Typical High V_{DD}	$PN_{10K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-107	-96	dBc/Hz

NOTES:

1. Continuity test
   Comparison limit value, no measurement value recorded.
2. Dynamic current
   For measurement of the dynamic current, the pattern *main_pattern* is used and loops from first to last vector. Instantaneous current is measured and recorded (without any link to a specific vector number). Total combined current for all V_{DD} pins. During the test, outputs are loaded with a capacitive load < 62 pF (tester load) but without active load. Comparators are disabled during this test.
3. Quiescent current
   During quiescent current test, outputs are loaded without active current load but with a capacitive load < 62 pF (tester load).
   The measurement is performed with the device having been initialised using pattern *mode*, stopped at end of vector labelled *pdwn_sp*. Total combined current of all V_{DD} pins.
   The measurement accuracy is better than 1µA.
4. Functional test
   During functional test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Output comparison is performed as "strobe comparison". Strobe is placed 5% before the end of the period. For the open-drain output (i.e. pin 51, LD), comparison to the "High-Impedance" state may be masked for some vectors.
5. Input voltages
   During input voltage test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Measurements are performed using the test pattern *main_pattern* (between the labels "main_st" and "end_u_d"). The pattern is run with increasing or decreasing input voltage value of the pin under test until the first output fails. Remaining pins toggle with nominal input voltages.
   All the values are tested and recorded for each input.
   The measurement accuracy is better than 100mV.
6. Output voltages
   Measurements are performed using the test pattern *main_pattern*.
   The device is configured into correct state so that outputs are placed in high or low voltages. Output current is sourced/sinked and the resulting voltage is measured.
   All the values are tested and recorded for each output.
7. High impedance leakage current
   The device is configured into the correct state using the pattern *main_pattern* so that the pin under

generators:

Timing Generator Number	Period (ns)	Pin Group	Delay (ns)	Width (ns)	Comp. Start (ns)	Comp. Stop (ns)	Format
0	1000	1 to 3	0	-	-	-	NRZ
		4 to 7	-	-	-	900	EDGE
1	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
2	1000	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	250	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
3	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
4	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
5	100	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	25	-	-	-	NRZ
		2 and 3	10	-	-	-	NRZ
		4 to 7	-	-	-	95	EDGE
6	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
7	1000	1 and 2	0	-	-	-	NRZ
		3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
8	1000	1 (except S_WR, S_CLK and SDATA pins)	0	-	-	-	NRZ
		S_WR pin	600	-	-	-	NRZ
		SCLK pin	250	-	-	-	NRZ
		SDATA pin	100	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
10	1000	1	0	-	-	-	NRZ

Timing Generator Number	Period (ns)	Pin Group	Delay (ns)	Width (ns)	Comp. Start (ns)	Comp. Stop (ns)	Format
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
11	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
12		1 (except E_WR, S_CLK and SDATA pins)	0	-	-	-	NRZ
		E_WR pin	100	-	-	-	NRZ
		SCLK pin	150	-	-	-	NRZ
		SDATA pin	10	-	-	-	NRZ
		2 and ~~4~~ 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE

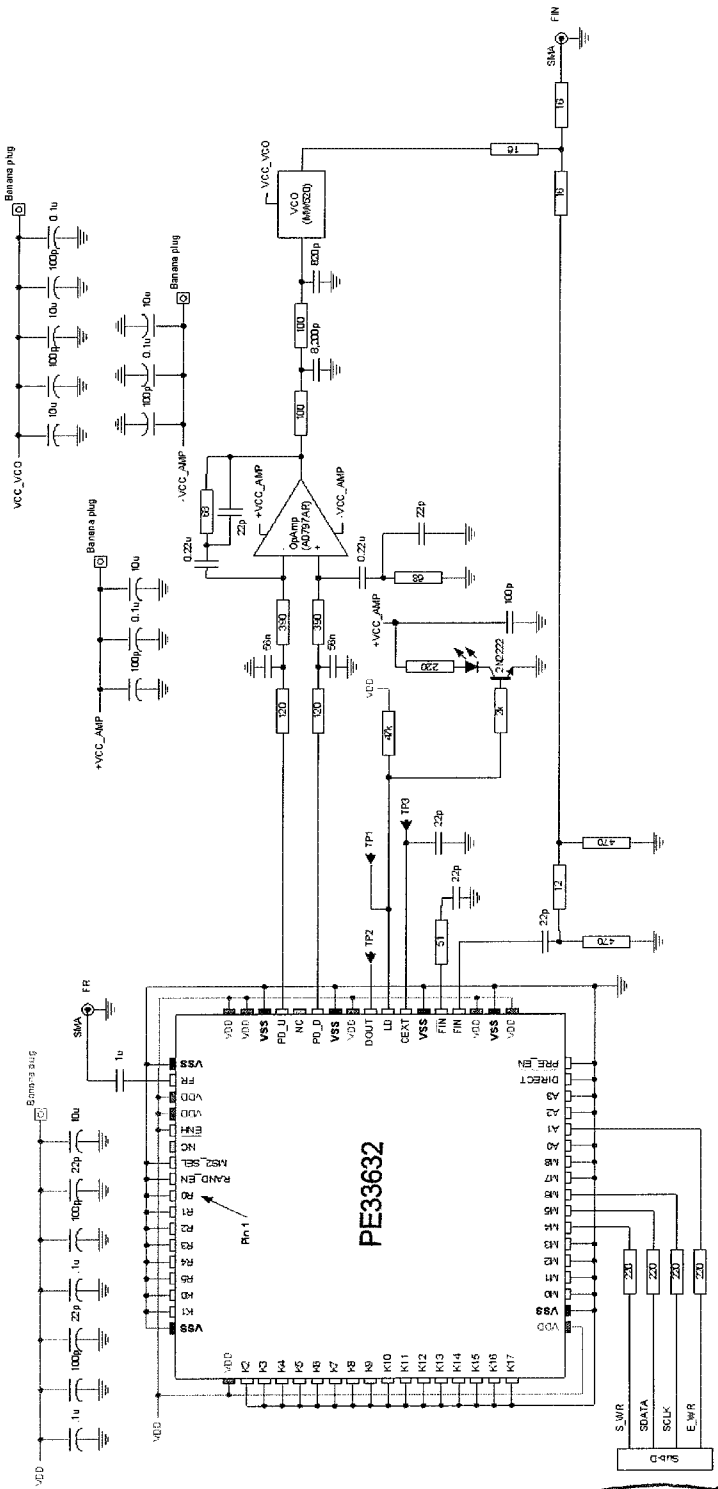
10. Dynamic measurements
    Parameters shall be measured and recorded for each dynamic parameter to be tested. The measurement accuracy is better than 0.5ns.
11. RF measurements
    The frequency is set to the target frequency and output level at the FIN pin. The resulting output power is measured on DOUT.
    The measurement accuracy is better than 0.1dB.
12. Phase Noise measurements
    The Phase Noise measurements use a "Stack-and-Rack" solution. The parametric test settings are described hereafter:
    - f_{IN} =1920.4MHz
    - f_r = 100 MHz (0dBm)
    - f_c = 20MHz
    - Loop Bandwidth = 50kHz
    - Register M = 8
    - Register R = 4
    - Register A = 6
    - Register K = 5243
    - Modulus = 10

13. Operating current during Phase Noise measurement
    The parametric test settings are described in Note 12 above.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+85 (+0 -5)°C and T_{amb}=- 40(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements, except as follows:



NOTES:

1. V_{DD}=3.3V, V_{CC}_VCO=5±0.2V, +V_{CC}_AMP=5V and -V_{CC}_AMP=-5V.
2. f_r=40MHz, V_P=V_{SS} to V_{DD}.
3. f_{IN}=1920.4 MHz, V_P=V_{SS} to V_{DD}.
4. All resistors have a tolerance of ±1%. All capacitors have a tolerance of ±10%.
5. TP1, TP2 and TP3 are the Test Probes.
6. The table below shows how the device shall be serially programmed during Total Dose Radiation