DOCUMENT CHANGE REQUEST

DCR number 487	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2009/04/14	Date sent: 2009/04/14	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Transistors High Power PNP, based on type 2N5153		
Number:	5204/002	Issue:	3

Other documents affected:

Page:

See attached mark-up of 5204/002 (Issue 4 - Draft A). Note that this mark-up also includes the changes of DCR 447 and DCR 430 (DCR 447 was approved 16th December 2008 and DCR 430 was approved 8th April 2009); it is proposed that once this DCR has been ap

Paragraph:

See attached mark-up of 5204/002 (Issue 4 - Draft A). Note that this mark-up also includes the changes of DCR 447 and DCR 430 (DCR 447 was approved 16th December 2008 and DCR 430 was approved 8th April 2009); it is proposed that once this DCR has been ap

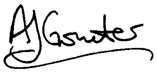
Original wording:

Proposed wording:

To introduce a number of editorial and technical changes (see the attached mark-up) which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types.

Justification:

Improve the appearance, content and clarity of the spec.

Attachments:
5204002_Issue_4_-_Draft_A.pdf, null
Modifications:
Page 6: Re-instate Note 1, with the other Notes reverting to their original numbers (e.g. Note 2 will remain Note 2 instead of becoming Note 1 as shown in the attached mark-up); Page 6, Note 2: add '', and any handling,'' between ''testing'' and ''performed''. Page 7: Note 5 will remain Note 5 (instead of becoming Note 4 as shown in the attached mark-up). Page 16, Paras. 2.9.1 and 2.9.2: There are to be no changes to the Power Dissipation Test Conditions.
Approval signature:

Date signed:
2009-04-14

Pages 1 to 17

TRANSISTORS, HIGH POWER, PNP

BASED ON TYPE 2N5153

ESCC Detail Specification No. 5204/002

as applicable

Issue 3,4 - Draft A	~~April 2007~~

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
~~187, 275~~	Specification up issued to incorporate editorial and technical changes per DCRs.

430, 447, tbd

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520400201

- Detail Specification Reference: 5204002
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g
01	2N5153	TO-39	D2	1.5
02	2N5153	TO-39	D3 or D4	1.5
03	2N5153	TO-39	D7	1.5
04	2N5153	TO-257	H2	5
05	2N5153	TO-257	H4	5
06	2N5153	SMD.5	Q14	2

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

07	2N5153	SMD.5	Q14	2

(DCR 430 refers)

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	-100	V	Over T_{op}
Collector-Emitter Voltage	V_{CEO}	-80	V	Over T_{op} Note ~~5~~ 4
Emitter-Base Voltage	V_{EBO}	-5.5	V	Over T_{op}
Collector Current	I_C	-5	A	Continuous Note ~~5~~ 4
Power Dissipation For TO-39 For TO-257 and SMD.5	P_{tot1}	 1 3.3	W	At $T_{amb} \leq +25^oC$ Note ~~1~~
For TO-39 For TO-257 and SMD.5	P_{tot2}	10 35	W	At $T_{case} \leq +25^oC$ Note ~~1~~
Operating Temperature Range	T_{op}	-65 to +200	^oC	Note ~~2~~ 1
Storage Temperature Range	T_{stg}	-65 to +200	^oC	Note ~~2~~ 1
Soldering Temperature For TO-39 and TO-257 For SMD.5	T_{sol}	 +260 +245	^oC	 Note ~~3~~ 2 Note ~~4~~ 3
Thermal ~~Resistance~~, Junction-to-Case For TO-39 For TO-257 and SMD.5	$R_{th(j-c)}$	 17.5 5	$^oC/W$	

NOTES:

~~1. For T_{amb} or $T_{case} > +25^oC$, derate linearly to 0W at $+200^oC$.~~

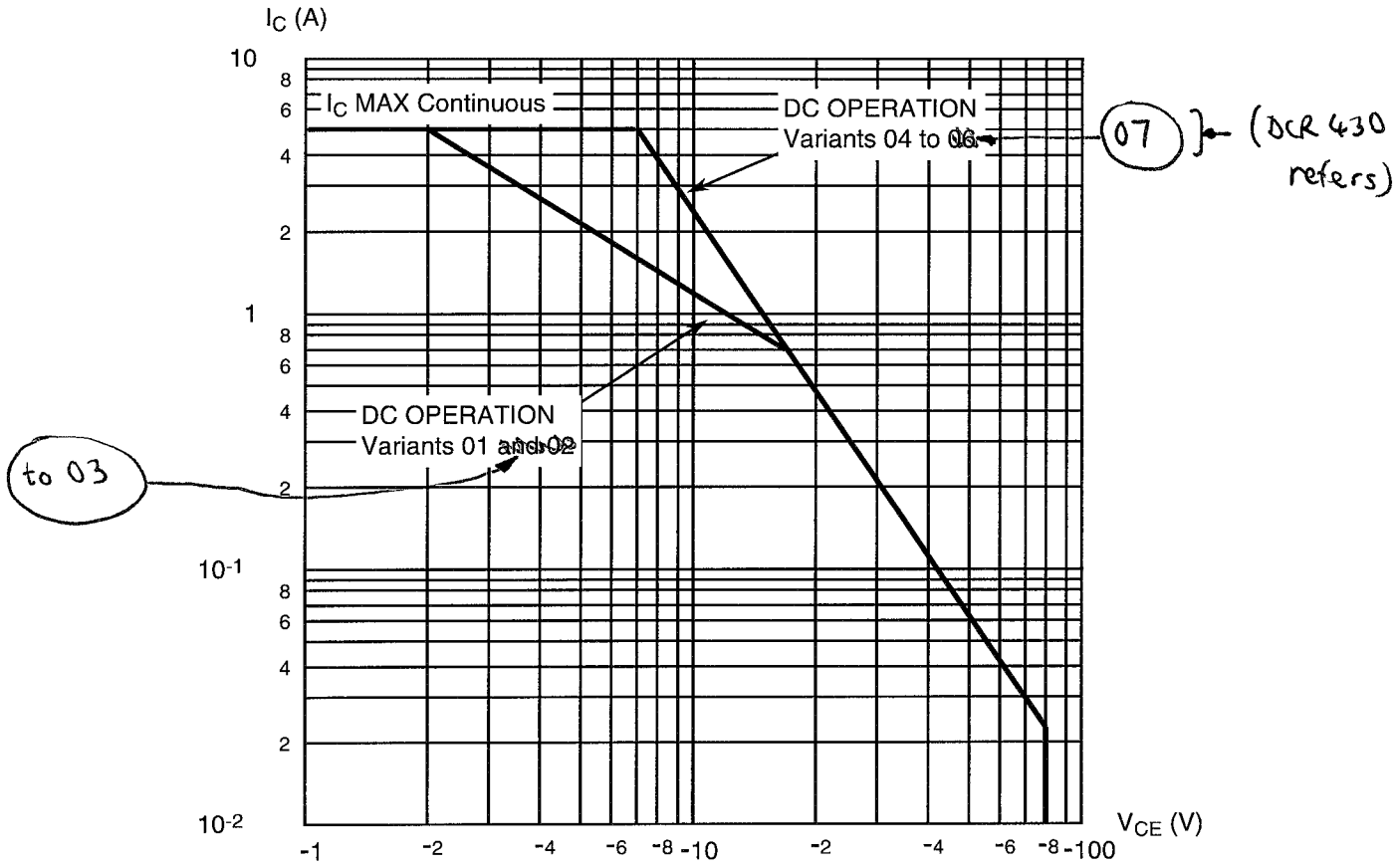
1. ~~2.~~ For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^oC$ shall be carried out in a 100% inert atmosphere.
2. ~~3.~~ Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
3. ~~4.~~ Duration 5 seconds maximum and the same package shall not be resoldered until 3 minutes have

Thermal Resistance, Junction-to-Ambient For TO-39 For TO-257 and SMD.5	$R_{th(j-a)}$	 175 53	°C/W	

elapsed.

4.5 Safe Operating Area applies as follows:

Maximum Safe Operating Area Graph



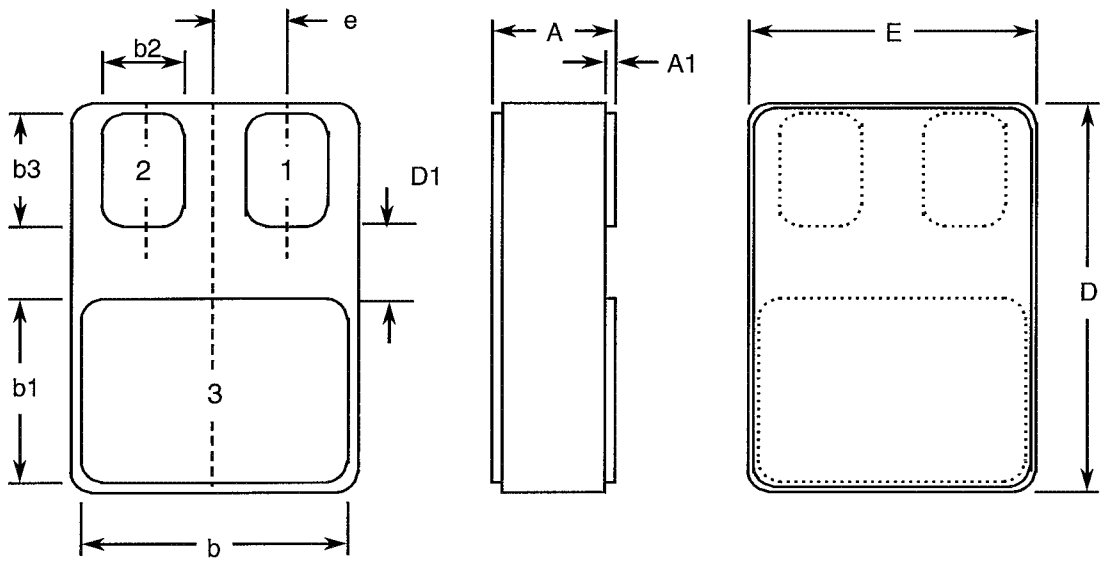
1.6 HANDLING PRECAUTIONS

The TO-257 package contains Beryllium Oxide (BeO) and therefore it must not be ground, machined, sandblasted or subjected to any mechanical operation which will produce dust. The case must not be subjected to any chemical process (e.g. etching) which will produce fumes.

Symbols	Dimensions mm		Notes
	Min	Max	
R	1.65 Typical		3

NOTES:
1. Terminal identification is specified by the components geometry where Lead 1 = emitter, Lead 2 = base and Lead 3 = collector.
2. Applies to all leads.
3. Radius of body corner, 4 places.

1.7.3 Surface Mount Package (SMD.5) - 3 terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.84	3.15	
A1	0.25	0.51	
b	7.13	7.39	
b1	5.58	5.84	
b2	2.28	2.54	2
b3	2.92	3.18	2
D	10.03	10.28	
D1	0.76	-	2
E	7.39	7.64	
e	1.91 BSC		2

NOTES:
1. Terminal identification is specified by the components geometry where Terminal 1 = emitter,

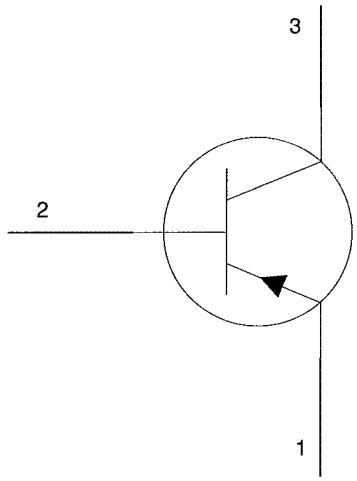
(base for Variant 07)

(emitter for Variant 07)

Terminal 2 = base and Terminal 3 = collector.

2. 2 places.

1.8 FUNCTIONAL DIAGRAM



Variants 01 to 06
1. Emitter
2. Base.
3. Collector

NOTES:

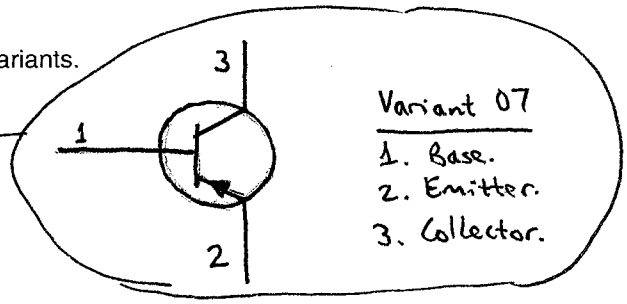
1. For TO-39, the collector is internally connected to the case.
2. For TO-257, the case is not connected to any lead.
3. For SMD.5, the lid is not connected to any terminal.

1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

a) Case
For the metal can package the case shall be hermetically sealed and have a metal body with hard glass seals.
For the metal flange mount package the case shall be hermetically sealed and have a metal body. The leads pass through ceramic eyelets brazed into the frame and the lid shall be welded.
For the surface mount package the case shall be hermetically sealed and have a ceramic body with a Kovar lid.

b) Leads/Terminals
As specified in Component Type Variants.



Variant 07
1. Base.
2. Emitter.
3. Collector.

(DCR 430 refers)

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.
Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this

2.8 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Conditions	Units
Ambient Temperature	T_{amb}	+150	°C
Emitter-Base Voltage	V_{EB}	-4.5	V
Collector-Base Voltage	V_{CB}	-60	V
Duration	t	48	hours

2.9 POWER BURN-IN CONDITIONS

2.9.1 Power Burn-in Conditions (TO-39)

. Derate

Characteristics	Symbols	Conditions	Units
Ambient Temperature	T_{amb}	+20 to +50 (1)	°C
Power Dissipation	P_{tot}	As per Maximum Ratings P_{tot1} derated at the chosen T_{amb}	W
Collector-Base Voltage	V_{CB}	-20	V

using the specified $R_{th(j-a)}$.

NOTES:
1. No heat sink nor forced air directly on the device shall be permitted.

2.9.2 Power Burn-in Conditions (TO-257 and SMD.5)

. Derate

Characteristics	Symbols	Conditions	Units
Case Temperature	T_{case}	+100(+0 -5)	°C
Power Dissipation	P_{tot}	As per Maximum Ratings P_{tot2} derated at the specified T_{case}	W
Collector-Base Voltage	V_{CB}	-20	V

using the specified $R_{th(j-c)}$.

2.10 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 3) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.

(Approved DCR 447 refers)