DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

42

Paragraph:

Chart F4

Original wording:

see issue 9

Proposed wording:

See attached draft issue 10.
The modifications are:
Note 11: deleted
Note 17: added (and Addition of reference to Note 17 in chart F4 in relation to Operating Life)
Added IGA under Assembly Capability Subgroup (and related Note 18)
Re-numbered Notes 19 and 20

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

none

Paragraph:

NEW CHART F0

Original wording:

none

Proposed wording:

See attached draft issue 10. Chart F0 becomes paragraph 12.1, the other Charts have to be re-numbered accordingly

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134	Changes required for: General	Originator: Fernando Martinez
Date: 2018/02/26	Date sent: 2018/01/25	Organisation: ESTEC
Status: IMPLEMENTED		

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

-none-

Paragraph:

ADD new paragraph 4.2.1 Single Phase Qualification (SPQ)

Original wording:

none

Proposed wording:

See attached draft 10

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

none

Paragraph:

NEW CHART F0

Original wording:

none

Proposed wording:

See attached draft issue 10. Chart F0 becomes paragraph 12.1 the other Charts have to be re-numbered accordingly

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134	Changes required for: General	Originator: Fernando Martinez	
Date: 2018/02/26	Date sent: 2018/01/25	Organisation: ESTEC	
Status: IMPLEMENTED			

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

10

Paragraph:

2.2 OTHER (REFERENCE) DOCUMENTS

Original wording:

See issue 9

Proposed wording:

ADD:
ECSS-Q-ST-70-08, Space Product Assurance: Manual soldering of high-reliability electrical connections
ECSS-Q-ST-70-38, Space Product Assurance: High-Reliability Soldering for Surface-Mount and Mixed Technology
JEP001 JEDEC FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

31

Paragraph:

8.25 OPERATING LIFE

Original wording:

Third bullet:
Data Points: As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours and 2000 ±48 hours. If drift values are specified, the drift shall always be related to the 0 hour measurement.

Proposed wording:

Third bullet:
Data Points: As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours and 2000 ±48 hours (and 4000 ±48 hours, if applicable, see Para. 4.2.1). If drift values are specified, the drift shall always be related to the 0 hour measurement.

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

9

Paragraph:

1.2

Original wording:

Bullets:

- Qualification of Standard Components per ESCC Basic Specification No. 20100.
- Qualification of a component within an approved capability domain per ESCC Basic Specification No. 24300.
- Technology Flow Qualification per ESCC Basic Specification No. 25400.

Proposed wording:

Bullets:

(a) Qualification of Standard Components per this ESCC Generic Specification and ESCC Basic Specification No. 20100.
(b) Qualification of a component within an approved capability domain per ESCC Basic Specification No. 24300.
(c) Technology Flow Qualification per ESCC Basic Specification No. 25400.

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134 Date: 2018/02/26 Status: IMPLEMENTED	Changes required for: General Date sent: 2018/01/25	Originator: Fernando Martinez Organisation: ESTEC

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

15

Paragraph:

4.6 ADD-ON COMPONENTS AND MATERIALS REQUIREMENTS

Original wording:

Second paragraph:
[...] (Capacitors only) [...]

Proposed wording:

Second paragraph:
[...] (Capacitors and Resistors only) [...]

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

ESCC

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

9

Paragraph:

2.1 ESCC SPECIFICATIONS

Original wording:

See issue 9

Proposed wording:

ADD:
No. 20200, Component Manufacturer Evalauation
No. 21001, Destructive Physical Analysis
No. 25100, Single Event Effects Test Method and Guidelines

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

11

Paragraph:

3 TERMS, DEFINITIONS, ETC ETC

Original wording:

[...]
Add-on Components: Capacitors mounted in and electrically connected to a Flip-chip Integrated Circuit assembly. Other component types are not permitted
[...]

Proposed wording:

[...]
Add-on Components: Capacitors and resistors mounted in and electrically connected to a Flip-chip Integrated Circuit assembly. Other component types are not permitted
[...]

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134	Changes required for: General	Originator: Fernando Martinez	
Date: 2018/02/26	Date sent: 2018/01/25	Organisation: ESTEC	
Status: IMPLEMENTED			

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

13

Paragraph:

4.2 Qualification and Qualification Maintenance requirements on a manufacturer

Original wording:

First paragraph:
To obtain and maintain the qualification of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100.

Proposed wording:

First paragraph:
To obtain and maintain the qualification of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100, except as amended in Para. 4.2.1.

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134	Changes required for: General		Originator: Fernando Martinez
Date: 2018/02/26	Date sent: 2018/01/25		Organisation: ESTEC
Status: IMPLEMENTED			

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

9

Paragraph:

1.1

Original wording:

second bullet:
Flip-chip Monolithic Microcircuits, solder ball bonded, hermetically and non-hermetically sealed packaged components with and without capacitors as Add-on Components

Proposed wording:

second bullet:
Flip-chip Monolithic Microcircuits, solder ball bonded, hermetically and non-hermetically sealed packaged components with and without passive (capacitors and resistors) as Add-on Components

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134

Changes required for: General

Originator: Fernando Martinez

Date: 2018/02/26

Date sent: 2018/01/25

Organisation: ESTEC

Status: IMPLEMENTED

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

none

Paragraph:

NEW PARAGRAPH 8.28 INTERNAL GAS ANALYSIS

Original wording:

none

Proposed wording:

MIL-STD-883, Test Method 1018

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

DOCUMENT CHANGE REQUEST

DCR number 1134	Changes required for: General		Originator: Fernando Martinez
Date: 2018/02/26	Date sent: 2018/01/25		Organisation: ESTEC
Status: IMPLEMENTED			

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	9

Other documents affected:

Page:

12

Paragraph:

4.1 General

Original wording:

First paragraph:
The requirements for the qualification of a component shall be in accordance with ESCC Basic Specification No. 20100

Proposed wording:

First paragraph:
Unless otherwise specified, the requirements for the qualification of a component shall be in accordance with ESCC Basic Specification No. 20100. Specifically for Wire-bonded Integrated Circuits, the requirements of Para. 4.2.1 shall also apply.

Justification:

Discussed and agreed by ad-hoc WG introducing Single Phase Qualification

Attachments:

dcr_attachment___escc9000_draft_10e_for_dcr1134.docx, escc9000_draft_10d_(single_phase_qual)_for_dcr.docx

Modifications:

The following modifications and additions to the original DCR1134 are included in this DCR; see replacement attachment ESCC 9000 Draft 10E for details (which highlights in yellow all changes from ESCC 9000 issue 9):

a) Editorial changes in the finalised specification for the purposes of clarification and consistency:

· Para. 2.1: addition of ESCC 2029000, 2269000

· Para. 4.1, 7.1.2.1, 7.1.2.2: add "unless otherwise specified, …"

· New Para. 4.2.1: several minor editorial changes are included

- Para. 8.25: option for the 4000h life test also added to the duration bullet.

- New Chart F0: redrawn with some editorial changes and clarifications to the contents

b) As agreed with and required by PSWG#83:

- Para. 8.12.2 & Chart F4A: Addition of temperature cycling test in Chart F4A for wire-bonded integrated circuits

- Chart F4A: change to the required quantity of life test samples (in the endurance subgroup) for Single Phase Qualification of wire-bonded integrated circuits to be 45 for qualification testing (retaining 15 etc samples for Periodic Testing).

Approval signature:

Date signed:

2018-02-26