ECI - Development & Qualification of an European Phase Locked-Loop

1. COMPANY PRESENTATION

- **PEREGRINE SEMICONDUCTOR EUROPE**

PEREGRINE SEMICONDUCTOR designs, manufactures and markets communication ICs for the wireless and broadband communications, space and avionics markets. Devices are manufactured on the UTSi® mixed-signal process technology. PEREGRINE'S facility in Aix-en-Provence, France is involved in the project. The contact person is Pascal LE BOHEC (PLebohec@psemi.com, +33 (0)4-4239-3361). www.psemi.com

- **ALCATEL ALENIA SPACE**

ALCATEL ALENIA SPACE is a major European satellite systems and orbital infrastructure manufacturer. The company's facilities at Toulouse, France and Rome, Italy are involved in the project. www.alcatel.com/space

- **HCM**

Located in La Rochelle, France, HCM has a 450 m^2 clean room equipped to allow a broad range of microelectronic assembly operations as well as the qualification of hi-rel components. In this project, HCM will undertake assembly and mechanical screening of the PLL in ceramic packages. www.hcm-france.com

- **ROOD TECHNOLOGY**

Located in Noerdlingen, Germany, ROOD TECHNOLOGY provides added value services to the semiconductor and electronics industries. In this project, ROOD TECHNOLOGY will undertake wafer probing, electrical testing and burn-in. www.roodtechnology.com

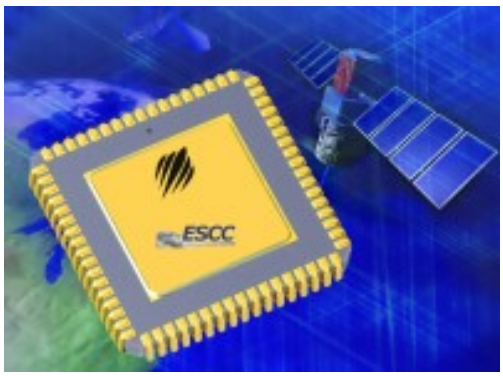
The **ESA Technical Officer** is Laurent MARCHAND (laurent.marchand@esa.int, +31 71-565-4282)

2. OVERVIEW

This activity is part of the European Component Initiative (ECI) put in place by the EUROPEAN SPACE AGENCY (ESA) with the aim to develop and qualify in Europe a number of critical space components in order to improve the competitive position of the European space industry. One such requirement is to develop an European supplier for phase lock loop components. This is considered to be essential in the context of the GALILEO program. The objective of the initial activity is to design, develop and qualify a specific Rad-Hard Phase Locked-Loop (PLL).

Main characteristics of this new PLL component are:

- 3.2 GHz operation÷10/11 dual-modulus prescaler
- Delta-Sigma modulator
- Phase detector output
- Serial and direct mode access
- Frequency selectivity: comparison frequency divided by 2^{18}
- Low Power
- Rad-Hard
- Ultra low phase noise
- 68-lead CQFPJ package



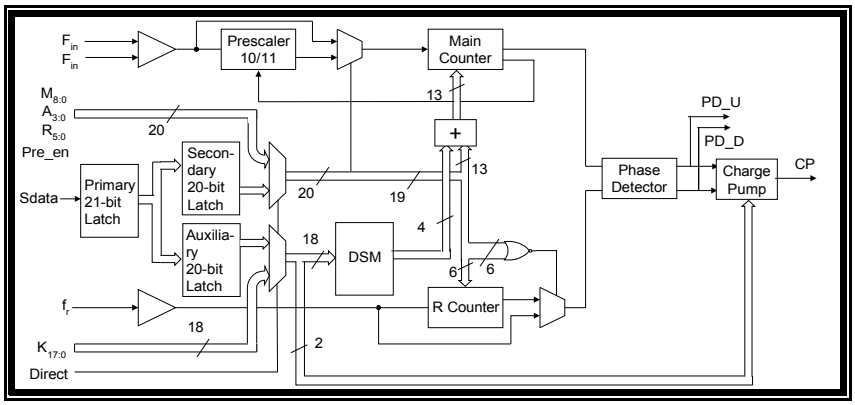
The overall project duration is planned to be 18 months with completion expected at the end of 2007.

3. WORK PACKAGES

The development approach and work structure are following the ESA Statement of Work (SoW). The project is divided into four (4) major technical tasks.

- **Task 1 – Technology and design trade-off analysis**

During Task 1, existing PLL components and technologies will be investigated.



- **WP1100** *(Assessment of non-European PLLs)*: A design survey shall be performed (WP1110) together with a review of the target performance required within the European space user community (WP1120).
- **WP1200** *(Technology process trade-off)*: This work package shall address the technology to be used, the packaging and testing of the European PLL.
- **WP1300** *(Design trade-off)*: This work package shall include all the design activities including circuit principles, electrical performance and testability.
- A Preliminary Design Review (**PDR**) will conclude the first task.

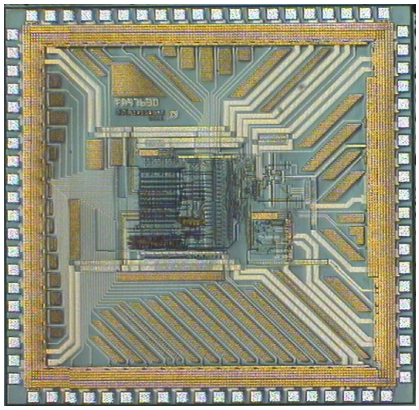
- **Task 2 – Process preparation and design activities**

During Task 2, all the design activities will occur on the UTSi® selected process.

- **WP2100** *(Process preparation)*: This work package shall demonstrate that the different processes (e.g. UTSi® technology and packaging) are appropriate for designing the PLL.
- **WP2200** *(Design activities)*: The work package shall include the electrical design of the PLL (WP2210) as well as the circuit layouts and the process design rules verifications (WP2220).
- **WP2300** *(Critical Design Review)*: A **CDR** shall be held to verify the design compliance for each of the electrical and technical key parameters.

- **Task 3 – PLLs fabrication and electrical characterization**

During Task 3, PLL wafers will be manufactured and qualified, PLL chips will be probe tested, packaged and electrically tested. An exhaustive electrical characterization and qualification shall be conducted on packaged PLLs.



- **WP3100** *(Processing, WLA and Characterization of the PLL chips)*: This work package includes the manufacturing of the PLL wafers with probe testing (WP3120) and the die singulation. It also includes all the upfront activities related to the special manufacturing steps (WP3110).
- **WP3200** *(In-process control, packaging and testing of the PLLs)*: This work package includes the assembly and screening of PLL dice (WP3210). A characterization shall verify that the devices meet the required electrical performance (WP3220) and the radiation level (WP3230).
- **WP3300** *(Production Control Review)*: During the **PCR** meeting, all results obtained shall be assessed.

- **Task 4 – PLLs screening and qualification**

The major activities to be carried out during this task are the screening and the qualification of the PLL devices in accordance with ESCC Generic Specification No. 9000.

- **WP4100** *(Preparation of PLLs Screening and Qualification)*: This work package includes all the activities dedicated to the preparation of the PLLs manufacturing. An audit of the different facilities shall be carried out (WP4110) and all documents shall be in place at the completion of the work package (WP4120).
- **WP4200** *(PLLs Screening)*: This work package covers all the activities performed as per ESCC 9000. Assembly (WP4210) and screening (WP4220) shall be performed.
- **WP4300** *(PLLs Qualification)*: This work package shall cover all the analysis related to any unexpected and/or unsatisfactory result that may occur (WP4310). A Final Report shall be issued together with a final update of all related documents such as the Detail Specification (WP4320).
- **WP4400** *(Qualification Review)*: A Qualification Readiness Review (**QRR**) will conclude the fourth task. All results of the screening and testing shall be assessed.