INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS 512K X 8-BIT, ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY

BASED ON TYPE 60142

ESCC Detail Specification No. 9301/052

Issue 2	October 2015

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
946	Specification upissued to incorporate editorial changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930105201R

- Detail Specification Reference: 9301052
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Access Time ns	Case	Terminal Material and/or Finish	Weight max g	Total Dose Radiation Level Letter
01	60142FT	17	MFP-F36	G2	4.5	R [100kRAD(Si)]
02	60142F	15	MFP-F36	G2	4.5	R [100kRAD(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 4.6	V	Note 1
Input Voltage Variant 01 Variant 02	V_{IN}	 -0.5 to 7 -0.5 to 4.6	V	Note 1
Output Voltage Variant 01 Variant 02	V_{OUT}	 -0.5 to 7 -0.5 to 4.6	V	Note 1
Input Current	I_{IN}	±10	mA dc	
Output Current	I_O	20	mA dc	Low condition
Device Power Dissipation (Continuous)	P_D	700	mW	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{case}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Soldering Temperature	T_{sol}	+300	°C	Note 2
Junction Temperature	T_j	+175	°C	
Thermal Resistance	$R_{th(j-c)}$	3	°C/W	

NOTES:

1. All voltages are with respect to V_{SS}. Devices are functional for $3V \leq V_{DD} \leq 3.6V$.
   Variant 01 is functional for $-0.3V \leq V_{IL} \leq 0.8V$; $2.2V \leq V_{IH} \leq 5.5V$.
   Variant 02 is functional for $-0.3V \leq V_{IL} \leq 0.8V$; $2.2V \leq V_{IH} \leq V_{DD}+0.3V$.
2. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

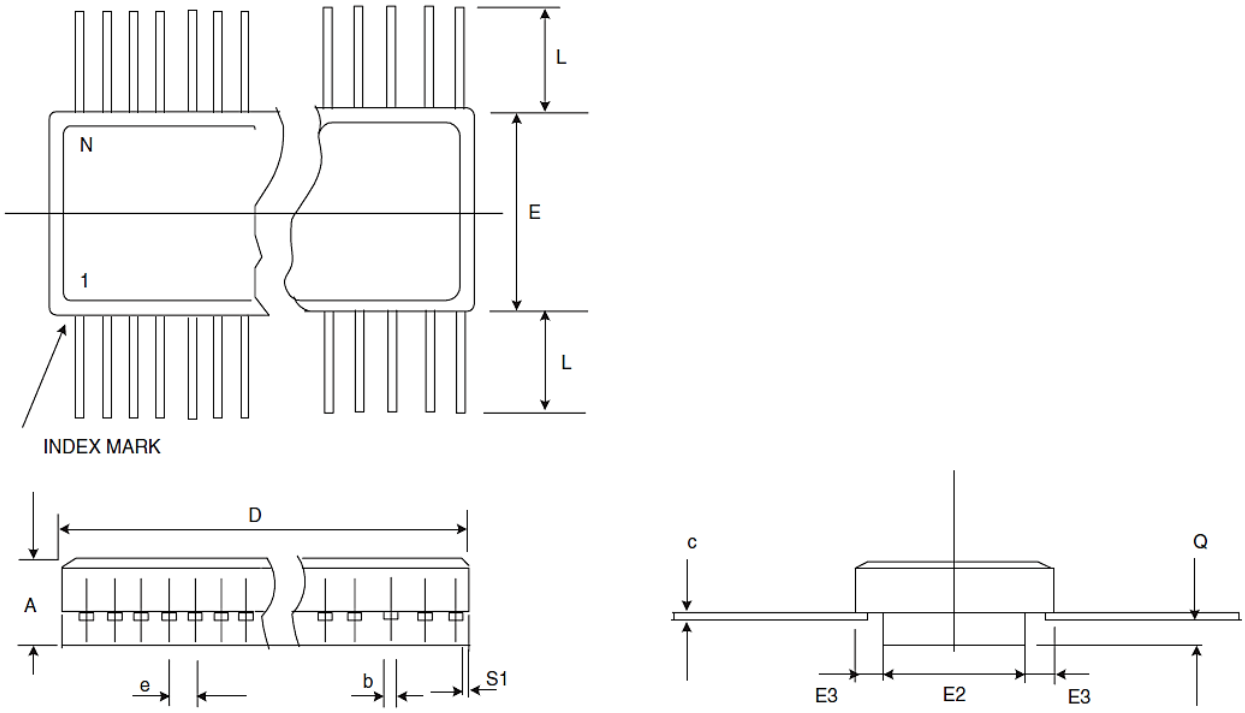
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling.

Variant 01 is categorised as Class 2 with a Minimum Critical Path Failure Voltage of 2000 Volts and Variant 02 is categorised as Class 3 with a Minimum Critical Path Failure Voltage of 4000 Volts per Basic Specification No. 23800.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Flat Leaded Multilayer Flat Package (MFP-F36) - 36 pins

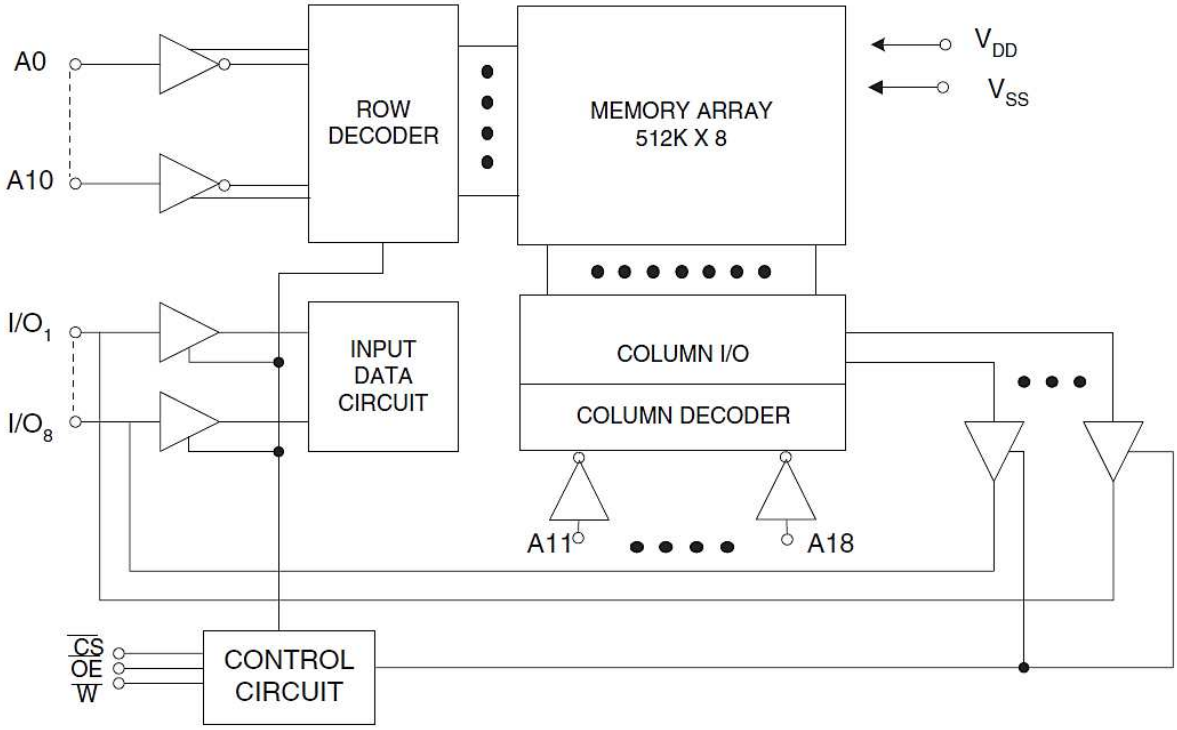


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.29	3.05	
b	0.38	0.51	2
c	0.1	0.18	2
D	-	23.62	
E	11.99	12.4	
E2	8.89	-	
E3	0.76	-	
e	1.27 BSC		3, 4
L	7.75	8.26	2
Q	0.66	1.14	5
S1	0.13	-	
N	36		

NOTES:
1. Index mark: a notch or pin 1 identification mark shall be located adjacent to pin 1.
2. All terminals.

3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. 34 spaces.
5. Dimension Q shall be measured at the point of exit of the lead from the body.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function	Pin	Function
1	A0 Input (Address)	19	-
2	A1 Input (Address)	20	A10 Input (Address)
3	A2 Input (Address)	21	A11 Input (Address)
4	A3 Input (Address)	22	A12 Input (Address)
5	A4 Input (Address)	23	A13 Input (Address)
6	$\overline{CS}$ Input (Chip Select)	24	A14 Input (Address)
7	I/O1 Input/Output (Data)	25	I/O5 Input/Output (Data)
8	I/O2 Input/Output (Data)	26	I/O6 Input/Output (Data)
9	V_{DD}	27	V_{DD}
10	V_{SS}	28	V_{SS}
11	I/O3 Input/Output (Data)	29	I/O7 Input/Output (Data)

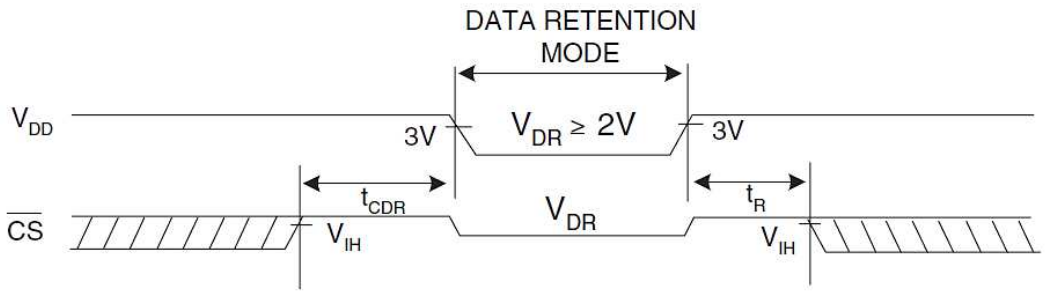
Pin	Function	Pin	Function
12	I/O4 Input/Output (Data)	30	I/O8 Input/Output (Data)
13	$\overline{W}$ Input (Write Enable)	31	$\overline{OE}$ Input (Output Enable)
14	A5 Input (Address)	32	A15 Input (Address)
15	A6 Input (Address)	33	A16 Input (Address)
16	A7 Input (Address)	34	A17 Input (Address)
17	A8 Input (Address)	35	A18 Input (Address)
18	A9 Input (Address)	36	-

1.10 TRUTH TABLE AND TIMING DIAGRAMS

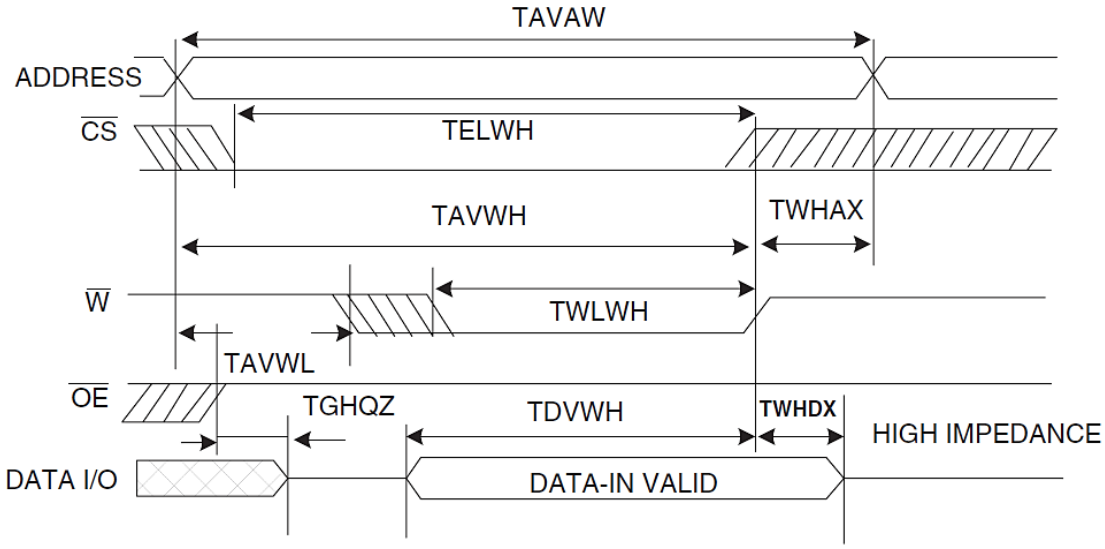
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance.

Inputs			Inputs/Outputs	Mode
$\overline{CS}$	$\overline{W}$	$\overline{OE}$		
H	X	X	Z	Deselect/Power down
L	H	L	Data out	Read
L	L	X	Data in	Write
L	H	H	Z	Output disable

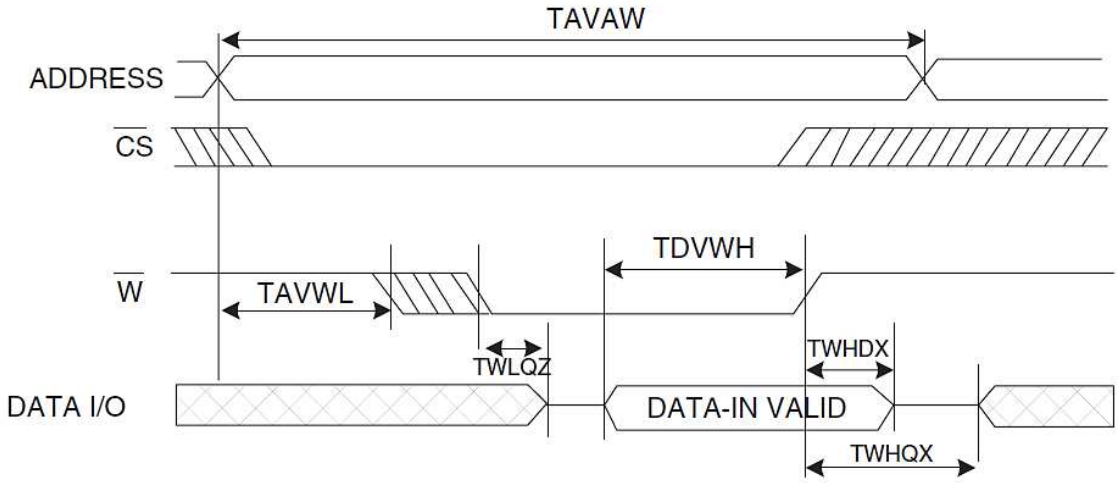
Data Retention



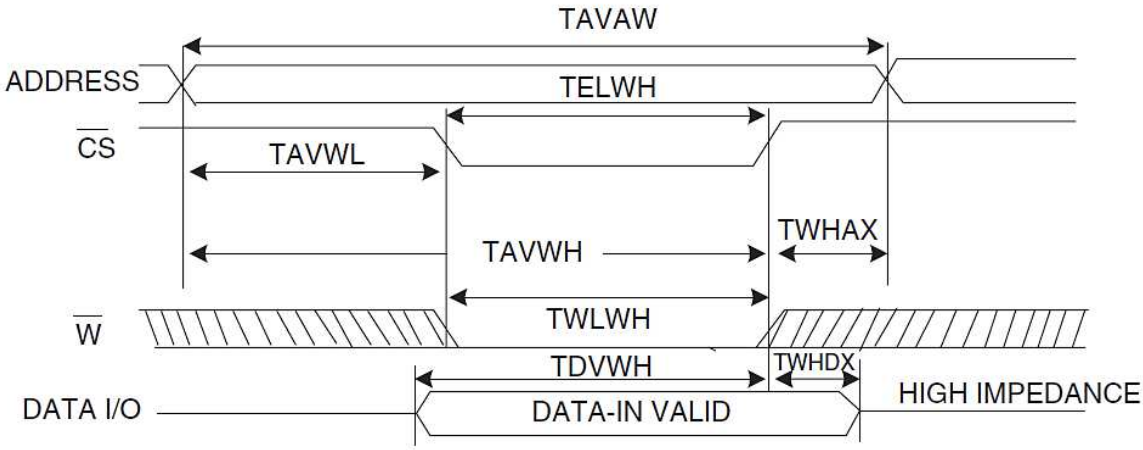
Write Cycle 1: $\overline{W}$ Controlled $\overline{OE}$ High During Write



Write Cycle 2: $\overline{W}$ Controlled $\overline{OE}$ Low



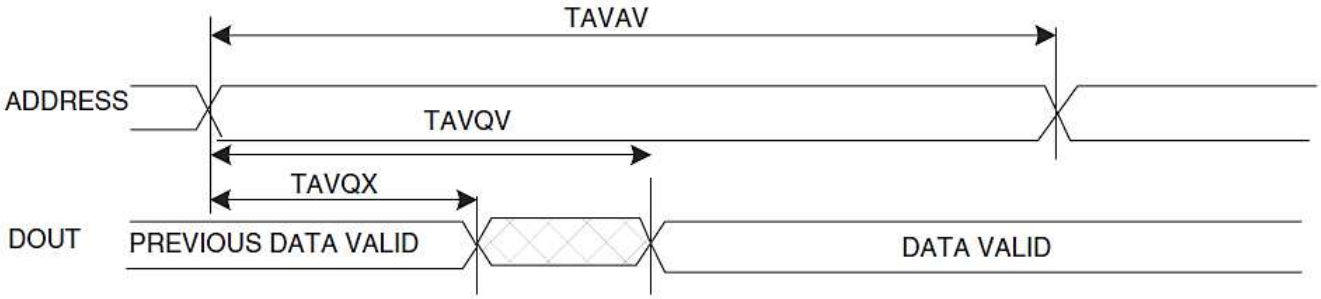
Write Cycle 3: $\overline{CS}$ Controlled (Note 1)



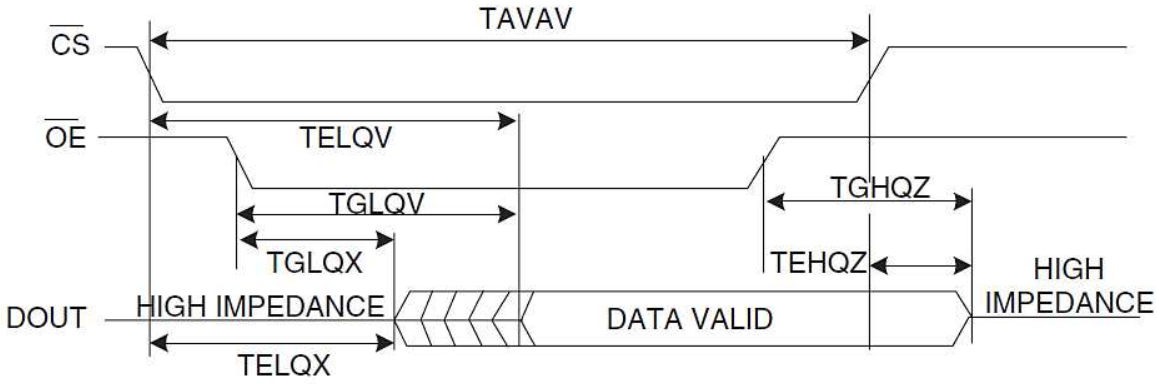
NOTES:

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ Low. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write.
   Data out is high impedance if $\overline{OE}$ = V_{IH}.

Read Cycle 1: Address Controlled $\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{W}$ = V_{IH}



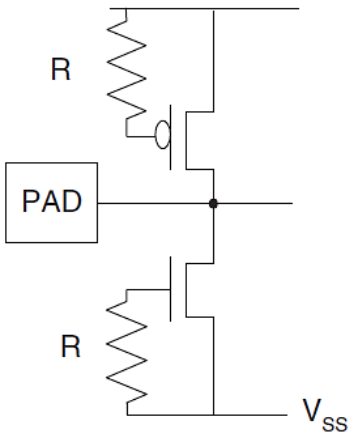
Read Cycle 2: $\overline{CS}$ Controlled $\overline{W}$ = V_{IH}



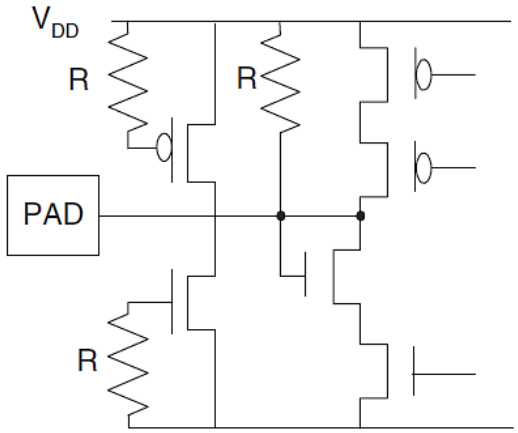
1.11 PROTECTION NETWORKS

Variant 01

Equivalent of Each Input



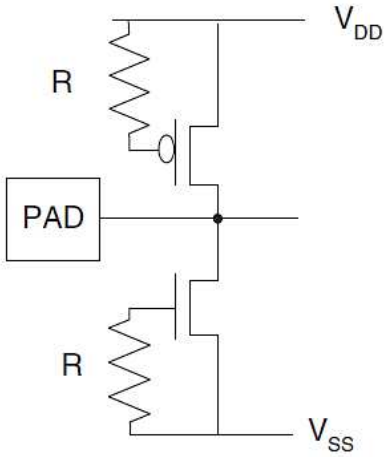
Equivalent of Each Output



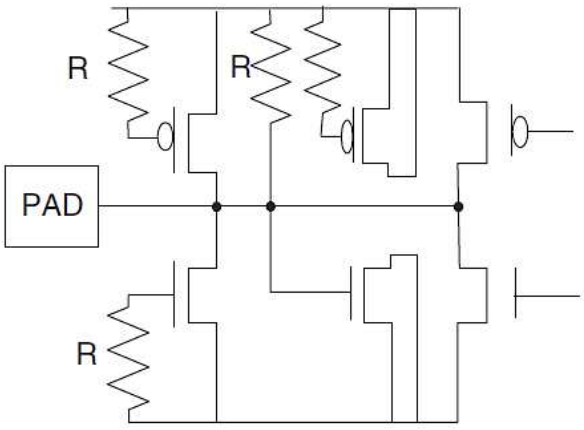
R = 500ohms

Variant 02

Equivalent of Each Input



Equivalent of Each Output



R = 500ohms

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{case} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 4	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage, to V_{SS}	V_{IC}	3008	I_{IN} (Under Test) = -100µA All Other Pins Open V_{DD} = Open, V_{SS} = 0V	-0.2	-2	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 3.6V V_{DD} = 3.6V, V_{SS} = 0V	-	-1	µA
High Level Input Current	I_{IH}	3010	Variant 01 V_{IN} (Under Test) = 3.6V V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 3.6V, V_{SS} = 0V	- -	1 10	µA
			Variant 02 V_{IN} (Under Test) = 3.6V V_{IN} (Remaining Inputs) = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	1	
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	3020	V_{IN} ($\overline{W}$, $\overline{OE}$) = 3V V_{IN} ($\overline{CS}$) = 0V V_{IN} (Output) = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	-1	µA
Output Leakage Current, Third State, High Level Applied	I_{OZH}	3021	Variant 01 V_{IN} ($\overline{W}$, $\overline{OE}$) = 3V V_{IN} ($\overline{CS}$) = 0V V_{IN} (Output) = 3.6V V_{IN} (Output) = 5.5V V_{DD} = 3.6V, V_{SS} = 0V	- -	1 10	µA
			Variant 02 V_{IN} ($\overline{W}$, $\overline{OE}$) = 3V V_{IN} ($\overline{CS}$) = 0V V_{IN} (Output) = 3.6V V_{DD} = 3.6V, V_{SS} = 0V	-	1	
Low Level Output Voltage	V_{OL}	3007	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} (Variant 01) = 6mA I_{OL} (Variant 02) = 8mA V_{DD} = 3V, V_{SS} = 0V	-	0.4	V
High Level Output Voltage	V_{OH}	3006	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OH} = -4mA V_{DD} = 3V, V_{SS} = 0V	2.4	-	V
Stand-by Supply Current	I_{DDSB}	3005	V_{IL} = 0.8V, V_{IH} = 2.2V V_{IN} ($\overline{CS}$) = 2.2V V_{DD} = 3.6V, V_{SS} = 0V	-	2.5	mA
Stand-by Supply Current 1	I_{DDSB1}	3005	V_{IL} = 0.8V, V_{IH} = 2.2V V_{IN} ($\overline{CS}$) = 3.3V V_{DD} = 3.6V, V_{SS} = 0V Note 3	-	2	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Dynamic Operating Current	I_{DDOP}	3005	V_{IN} ($\overline{W}$, $\overline{OE}$) = 2.2V V_{IN} (Remaining Inputs) = V_{SS} or V_{DD} I_{OUT} = 0mA V_{DD} = 3.6V, V_{SS} = 0V Variant 01 f = 59MHz Variant 02 f = 67MHz	 - -	 170 180	mA
Data Retention Current	I_{DDDR}	3005	V_{IN} ($\overline{CS}$) = 2V V_{IN} (Remaining Inputs) = V_{SS} or V_{DD} V_{DD} = 2V, V_{SS} = 0V Note 3	-	1.5	mA
V_{DD} for Data Retention	V_{DDDR}	-	Note 4	2	-	V
Input Capacitance	C_{IN}	3012	V_{IN} = V_{SS} = 0V V_{DD} = 3.3V f = 1MHz Note 8	-	12	pF
Output Capacitance	C_{OUT}	3012	V_{IN} = V_{SS} = 0 V_{DD} = 3.3V f = 1MHz Note 8	-	12	pF
Read Cycle Time	t_{AVAV}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 5 Variant 01 Variant 02	 17 15	 - -	ns
Address Access Time	t_{AVQV}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 6 Variant 01 Variant 02	 - -	 17 15	ns
Address Valid to Low Z	t_{AVQX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 5	5	-	ns
Write Cycle Time	t_{AVAW}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 5 Variant 01 Variant 02	 17 15	 - -	ns
Address Set-up Time	t_{AVWL}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 5	0	-	ns
Address Valid to End of Write	t_{AVWH}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 5	8	-	ns
Data Set-up Time	t_{DVWH}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 5	7	-	ns
$\overline{CS}$ Low to Write End	t_{ELWH}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 5	12	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Write Low to High Z	t_{WLQZ}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Note 7 Variant 01 Variant 02	 - -	 7 6	ns
Write Pulse Width	t_{WLWH}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 6	8	-	ns
Address Hold from End of Write	t_{WHAX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 5	0	-	ns
Data Hold Time	t_{WHDX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Notes 2, 5	0	-	ns
Write High to Low Z	t_{WHQX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Note 7	3	-	ns
$\overline{CS}$ Access Time	t_{ELQV}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 6 Variant 01 Variant 02	 - -	 17 15	ns
$\overline{CS}$ Low to Low Z	t_{ELQX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Note 7	5	-	ns
$\overline{CS}$ High to High Z	t_{EHQZ}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Note 7 Variant 01 Variant 02	 - -	 7 6	ns
Output Enable Access Time	t_{GLQV}	3003	V_{DD} = 3V, V_{SS} = 0V Notes 2, 5 Variant 01 Variant 02	 - -	 8 6	ns
$\overline{OE}$ Low to Low Z	t_{GHQX}	3003	V_{DD} = 3V & 3.6V V_{SS} = 0V Note 7	2	-	ns
$\overline{OE}$ High to High Z	t_{GHQZ}	3003	V_{DD} = 3V, V_{SS} = 0V Note 7 Variant 01 Variant 02	 - -	 6 5	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be V_{IN} = V_{SS} or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V)
March	100	3 and 3.6	0	0	3	0.5	-0.5	1.5
Checkerboard	100	3 and 3.6	0	0	3	0.5	-0.5	1.5
Imag	100	3 and 3.6	0	0	3	0.5	-0.5	1.5
Genbl	100	3	0	0	3	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V)
March	100	3.6	0	-0.3	Variant 01 = 5.5 Variant 02 = 3.9	0.5	-0.5	1.5
March	100	3	0	-0.3	3.3	0.5	-0.5	1.5
March	100	3.6	0	0	2.2	0.5	-0.5	1.5
March	100	3	0	0.8	0	0.5	-0.5	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V)
March	100	3	0	0	3	Variant 01 = 6 Variant 02 = 8	-4	Note (b)

FUNCTIONAL TEST 4

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V)
March	80	3 and 3.6	0	0	3	0.5	-0.5	1.5
Comarch	80	3 and 3.6	0	0	3	0.5	-0.5	1.5
Imag	80	3 and 3.6	0	0	3	0.5	-0.5	1.5
Checkerboard	80	3 and 3.6	0	0	3	0.5	-0.5	1.5

(a) A write cycle is followed by a read cycle. The time between start of write and start of read per the table is the specified timing parameter. $t_r = t_f = 5$ns maximum.
(b) 0.4V for low output level, 2.4V for high output level.
(c) Output load 1 TTL gate equivalent + $C_L < 30$pF.

3. Measurements are performed with the memory loaded with a background of zeros, then with a background of ones, for all inputs High, then Low. Only the worst case is recorded.

4. Data retention procedure:
   (a) Write memory at V_{DD} = 3V with CHECKERBOARD pattern with V_{IL} = 0V and V_{IH} = 3V.
   (b) Power down to V_{DD} = 2V for 250ms, V_{IN} ($\overline{CS}$) = 1.8V.
   (c) Restore V_{DD} to 3V, wait t_R (operation recovery time), read memory and compare with original pattern.
   (d) Repeat the procedure with $\overline{CHECKERBOARD}$ pattern.
   (e) t_R = 17ns for variant 01 and 15ns for variant 02.
   (f) During power up and power down transitions, V_{IN} ($\overline{CS}$) ≥ V_{DD}-0.2V, V_{IN} (Remaining Inputs) ≤ 0.2V or ≥ V_{DD}-0.2V.
5. Parameter tested go-no-go during Functional Test 4.
6. Parameter measured during Functional Test 4 using pattern March at 3V and 3.6V.
7. Guaranteed with output loading 5pF but not tested.
8. Guaranteed but not tested.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{case} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{case} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}				µA
Variant 01, V_{IN}=3.6V		±0.1	-	1	
Variant 01, V_{IN}=5.5V		±1	-	10	
Variant 02		±0.1	-	1	
Output Leakage Current, Third State Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current, Third State High Level Applied	I_{OZH}				µA
Variant 01, V_{IN} (Output) = 3.6V		±0.1	-	1	
Variant 01, V_{IN} (Output) = 5.5V		±1	-	10	
Variant 02		±0.1	-	1	
Low Level Output Voltage	V_{OL}	±0.1	-	0.4	V
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Stand-by Supply Current	I_{DDSB}	±0.25	-	2.5	mA

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Stand-by Supply Current 1	I_{DDSB1}	±0.2	-	2	mA
Data Retention Current	I_{DDDR}	±0.15	-	1.5	mA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

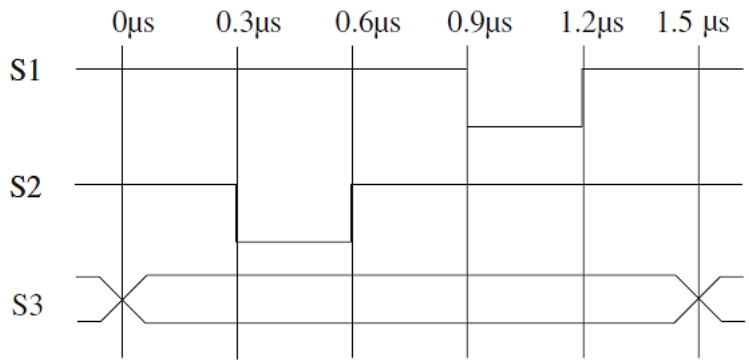
2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{case}	125 (+0 -5)	°C
Input $\overline{CS}$	V_{IN}	V_{SS}	V
Inputs A0 to A18	V_{IN}	$V_{GEN(S3)}$ to $V_{GEN(S21)}$ (Note 1)	V
Input $\overline{OE}$	V_{IN}	$V_{GEN(S1)}$ (Note 2)	V
Input $\overline{W}$	V_{IN}	$V_{GEN(S2)}$ (Note 2)	V
Inputs/Outputs I/O1, I/O3, I/O5, I/O7	V_{IN}	$V_{GEN(S22)}$ (Note 1)	V
Inputs/Outputs I/O2, I/O4, I/O6, I/O8	V_{IN}	$V_{GEN(S23)}$ (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	$f_{GEN(S3)}$	330 ±20%	kHz
Positive Supply Voltage	V_{DD}	3.7 ±0.1	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. $f_{GEN(Sn)} = \frac{1}{2} f_{GEN(Sn-1)}$ for n > 3.

2. Control Input:



3. Input and Output protection resistor/load = 1kΩ.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	°C
Inputs/Outputs I/O1 to I/O8	$V_{IN/OUT}$	Open	V
Inputs A0 to A18, $\overline{OE}$, $\overline{W}$ Variants 01 Variants 02	V_{IN}	 5.5 (+0 -0.1) 3.6 (+0 -0.1)	V
Input $\overline{CS}$	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	3.6 (+0 -0.1)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input protection resistors = 10kΩ.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{case} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.