INTEGRATED CIRCUITS, SILICON MONOLITHIC, 10-BIT, 2.2GSPS, ANALOGUE TO DIGITAL CONVERTER

BASED ON TYPE AT84AS008

ESCC Detail Specification No. 9407/004

Issue 1	October 2008

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

940700401R

- Detail Specification Reference: 9407004
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	AT84AS008	CI-CGA152	R1	9.1	R [100kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification no. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Analogue Positive Supply Voltage Range	V_{DD}	GND to 6	V	Note 1
Analogue Negative Supply Voltage Range	V_{SS}	GND to -5.5	V	Note 1
Digital Positive Supply Voltage Range	DV_{DD}	GND -1.1 to 2	V	Note 1
Digital Negative Supply Voltage Range	DV_{SS}	GND to -5.5	V	Note 1
Difference between Digital Supplies	DV_{DD} - DV_{SS}	7	V	
Difference between Negative Supplies	V_{SS} - DV_{SS}	0.3	V	
Analogue Input Voltage Range	V_A, V_B	-1.5 to 1.5	V	
Differential Analogue Input Voltage Range	V_A - V_B	-1.5 to 1.5	V	
Clock Input Common Mode Voltage Range	$(V_{CLK}+V_{CLKB})/2$	-1.5 to 0.6	V	
Differential Clock Input Voltage Range	V_{CLK} - V_{CLKB}	-1 to 1	V_{p-p}	
Static Input Voltage Range	V_{SI}	-1 to 0.8	V	Note 2
Digital Input Voltage Range	V_{DI}	-5 to +0.8	V	Note 3
Digital Output Voltage Range	V_{OD}	DV_{DD} min. operating -2.2 to DV_{DD} max. operating +0.8	V	
Device Power Dissipation (Continuous)	P_D	Note 4	W	Note 5
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Soldering Temperature	T_{sol}	+300	°C	
Junction Temperature	T_j	+130	°C	Note 5
Thermal Resistance Junction to Ambient	$R_{th(j-a)}$	30	°C/W	Note 5

NOTES:

1. The maximum ratings are limiting values referenced to GND = 0V.
2. Applies to the GA and SDA inputs.
3. Applies to the SDAEN, DRRB, B/GB, PGEB and DECB inputs.
4. The maximum device dissipation shall be determined by the formula: $P_D = |I_{DD}|x|V_{DD}| + |I_{SS}|x|V_{SS}| + |DI_{DD}|x|DV_{DD}| + |DI_{SS}|x|DV_{SS}|$
5. An external heatsink shall be used.

1.6 HANDLING PRECAUTIONS

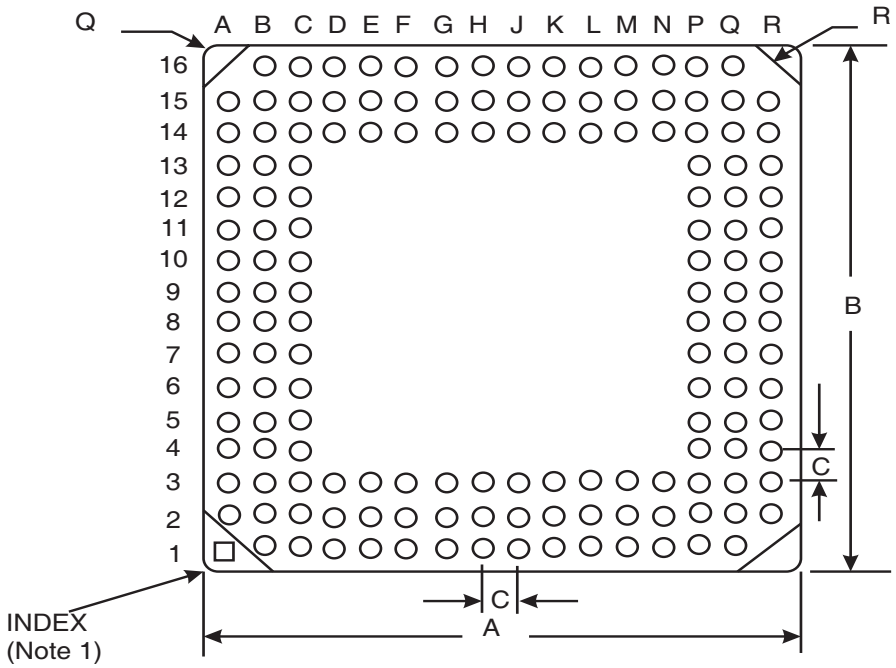
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 750 Volts.

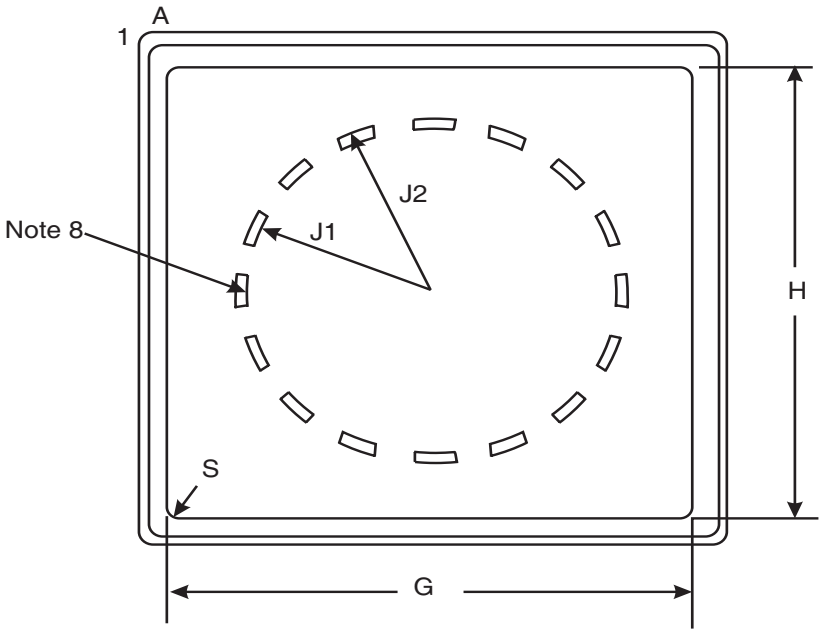
1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Column Grid Array Package (CI-CGA152) - 152 columns

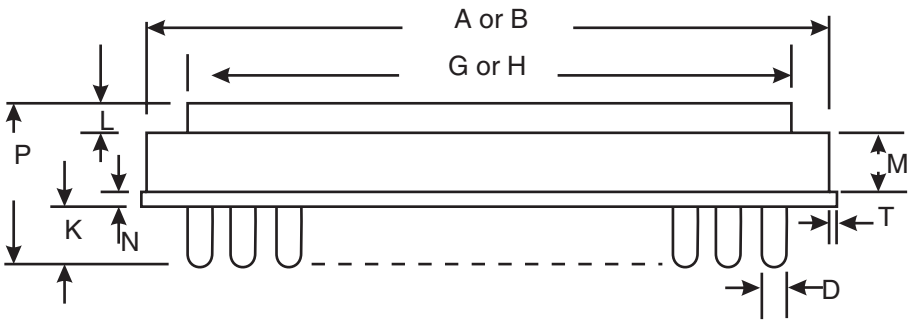
Bottom View



Top View



Side View

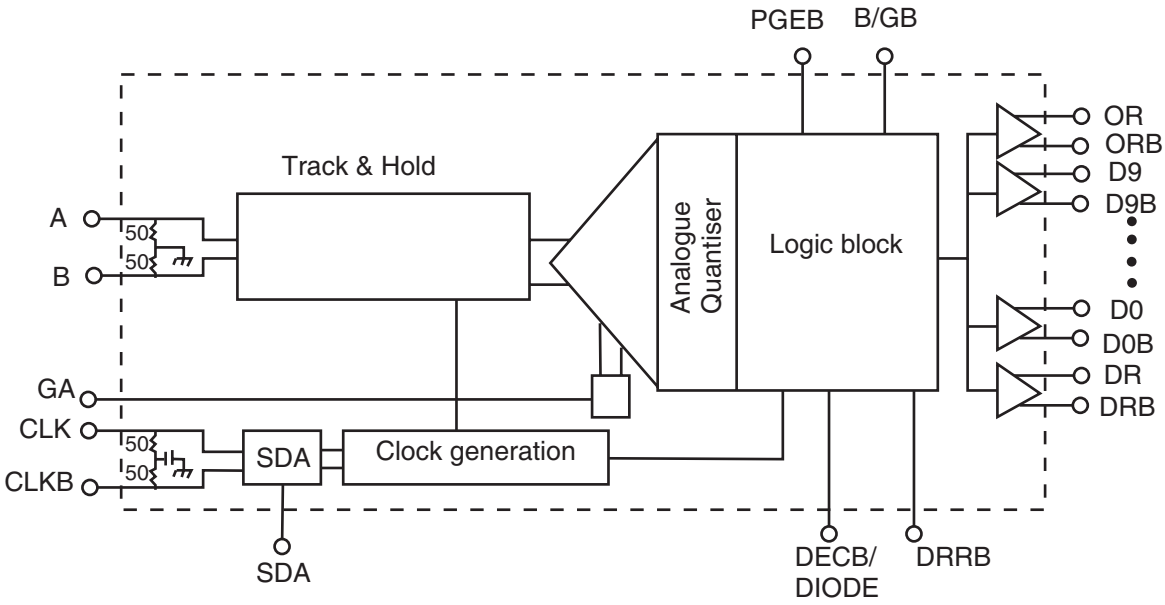


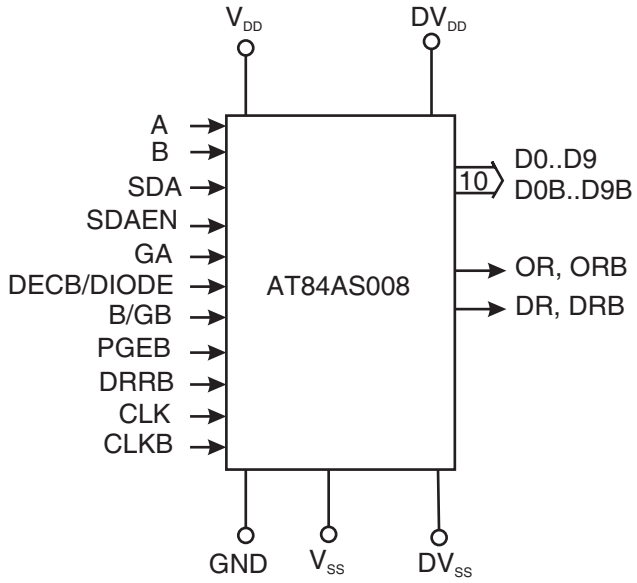
Symbols	Dimensions mm		Notes
	Min	Max	
A, B	20.8	21.2	
C	1.27 BSC		2
D	0.79	0.99	3, 4
G, H	18.32	18.68	
J1	6.5	6.9	5
J2	6.8	7.2	5
K	1.545	1.695	4, 9
L	0.71	0.89	
M	1.5	1.82	
N	0.25	0.35	
P	4.02	4.82	
Q	-	0.4	6
R	-	1.8	6
S	-	0.5	6
T	-	0.2	7

NOTES:

1. Index Mark: a terminal identification mark shall be located in the A1 position and shall have no column attached.
2. 152 columns. The true position column spacing is 1.27mm between centrelines. Each column shall be located within ±0.15mm of its true longitudinal position relative to A1 and the highest column or row number in each axis.
3. Diameter.
4. All columns.
5. Radius. J2 shall always be greater than J1.
6. Chamfer, applies to all four corners.
7. Nominal 0mm, applied all around the periphery.
8. Nickel Gold metallised marking that shall define the footprint for the external heatsink.
9. The column coplararity shall not exceed 150µm.

1.8 FUNCTIONAL DIAGRAMS





1.9 PIN ASSIGNMENT AND DESCRIPTION

Name	Pin number	Description
POWER SUPPLIES		
V_{DD}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	5V analogue supply (connected to same power supply plane)

Name	Pin number	Description
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analogue ground
V_{SS}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analogue supply (connected to same power supply plane)
DV_{DD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{SS}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V or -2.2V Digital negative supply
ANALOGUE INPUTS		
A	R5	In-phase (+) analogue input signal of the differential Sample & Hold preamplifier
B	R6	Inverted phase (-) analogue input signal of the differential Sample & Hold preamplifier
CLOCK INPUTS		
CLK	E1	In-phase (+) clock input
CLKB	F1	Inverted phase (-) clock input
DIGITAL OUTPUTS		
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	In-phase (+) digital outputs D0 is the LSB, D9 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	Inverted phase (-) digital outputs
OR	C16	In-phase (+) Out-of-Range output
ORB	C15	Inverted phase (-) Out-of-Range output
DR	H16	In-phase (+) Data Ready signal output
DRB	H15	Inverted phase (-) Data Ready signal output
ADDITIONAL FUNCTIONS		

Name	Pin number	Description
B/GB	A11	Binary or Gray select output format control -Binary output format if B/GB is floating or connected to GND -Gray output format if B/GB is connected to V_{SS}
DECB / DIODE	A10	Decimation Function Enable or Die junction temperature measurement: -Decimation active when LOW (Die junction temperature monitoring is then NOT POSSIBLE); -Normal mode when HIGH or left floating Die Junction temperature monitoring when current is applied
PGEB	A9	Active low Pattern Generator Enable -Digitised input delivered at outputs according to B/GB if PGEB is floating or connected to GND -Checker Board pattern delivered at outputs if PGEB is connected to V_{SS}
DRRB	N1	Asynchronous Data Ready Reset function (active at ECL low level)
GA	R9	Gain Adjust.
SDA	A6	Sampling delay adjust
SDAEN	P1	Sampling delay adjust enable inactive if floating or connected to GND active if connected to V_{SS}
UNUSED COLUMNS		
NC	A2, A15, R2, R15	Not connected but may be connected to GND

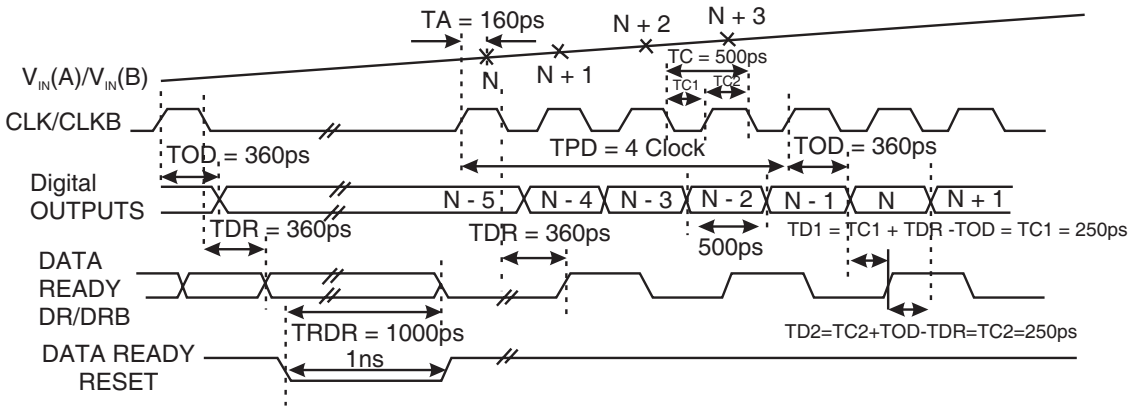
1.10 TRUTH TABLE AND TIMING DIAGRAMS

1. Logic Level Definitions: 1 = Digital High Level, 0 = Digital Low Level, MSB = Most Significant Bit, LSB = Least Significant Bit.

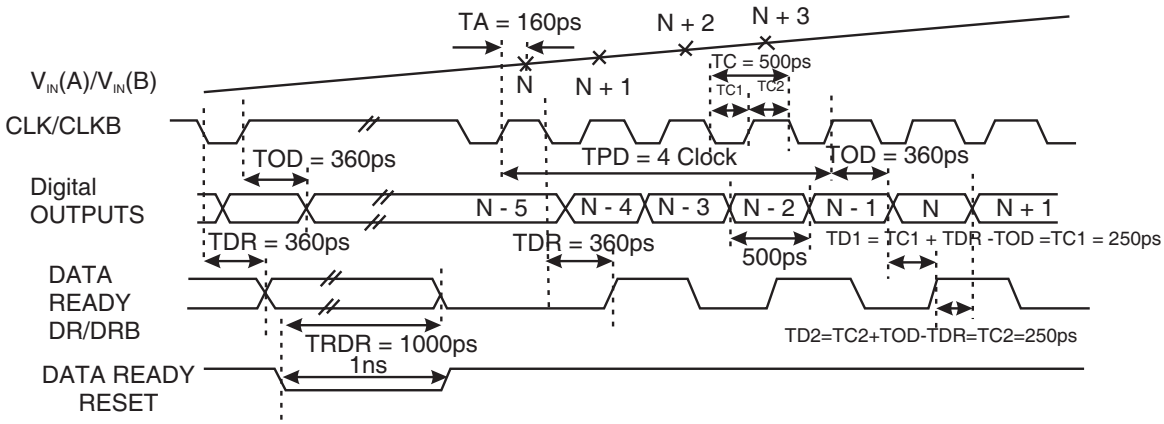
Differential Analogue Input	Voltage Level	Digital Output			
		Binary (B/GB = GND or floating)		Gray (B/GB = V_{SS})	
		MSB.....LSB	Out-of-Range	MSB.....LSB	Out-of-Range
> +250.25 mV	> Top end of full-scale + 1/2 LSB	1111111111	1	1000000000	1
+250.25 mV +249.75 mV	Top end of full-scale + 1/2 LSB Top end of full scale - 1/2 LSB	1111111111 1111111110	0 0	1000000000 1000000001	0 0

Differential Analogue Input	Voltage Level	Digital Output			
		Binary (B/GB = GND or floating)		Gray (B/GB = V_{SS})	
		MSB.....LSB	Out-of-Range	MSB.....LSB	Out-of-Range
+125.25 mV +124.75 mV	3/4 full-scale + 1/2 LSB 3/4 full-scale - 1/2 LSB	1100000000 1011111111	0 0	1010000000 1110000000	0 0
+0.25 mV -0.25 mV	Midscale + 1/2 LSB Midscale -1/2 LSB	1000000000 0111111111	0 0	1100000000 0100000000	0 0
-124.75 mV -124.25 mV	1/4 full-scale +1/2 LSB 1/4 full-scale - 1/2 LSB	0100000000 0011111111	0 0	0110000000 0010000000	0 0
-249.75 mV -250.25 mV	Bottom end of full-scale + 1/2 LSB Bottom end of full-scale - 1/2 LSB	0000000001 0000000000	0 0	0000000001 0000000000	0 0
< -250.25 mV	< Bottom end of full-scale - 1/2 LSB	0000000000	1	0000000000	1

Data Ready Reset, Clock held at Low Level (Notes 1 and 2)



Data Ready Reset, Clock held at High Level (Notes 1 and 2)



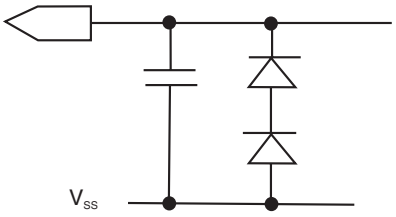
NOTES:

1. 2 Gsps Clock Rate
2. Definition of terms:
   - TA: Aperture Delay, TA is the delay between the rising edge of the differential clock inputs (CLK, CLKB) (zero crossing point) and the time at which (A or B input) is sampled.
   - TC: Encoding clock period. TC = TC1 + TC2.
   - TC1: Minimum clock pulse width (high)
   - TC2: Minimum clock pulse width (low).
   - TPD: Pipeline Delay. The number of clock cycles between the sampling edge of an input data and the associated output data being made available (not taking into account the TOD).
   - TOD: Digital data Output Delay, TOD is the delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
   - TDR: TIme delay from Clock to Data Ready, TDR is the time from the falling edge of the differential clock inputs (CLK, CLKB) to the next point of change in the differential output Data Ready outputs.
   - TD1: Time delay from Data to Data Ready. TD1 is the time difference between Data and Data

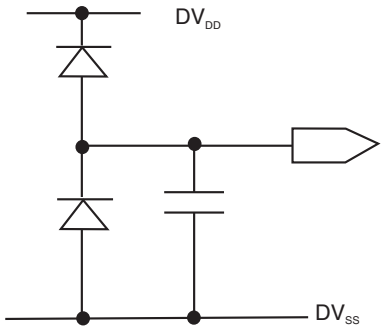
Ready. General expression is TD1 = TC1 + TDR - TDO with TC = TC1 + TC2 = 1 encoding clock period.

– TD2: Time delay from Data Ready to Data. General expression is TD2 = TC2 + TDR - TOD with TC = TC1 + TC2 =1 encoding clock period.
– TRDR: Time delay from Reset to Data Ready. When the pin DRRB is used as a reset pin, TRDR is the delay between the falling edge of the DRRB input and the corresponding falling edge of the Data Ready output.

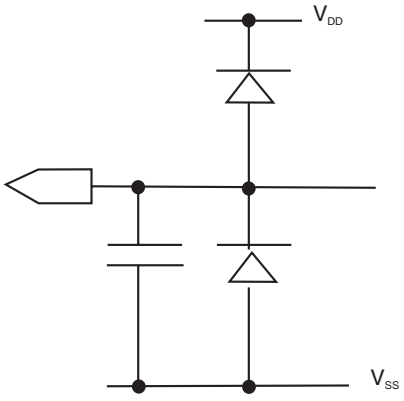
1.11 PROTECTION NETWORKS



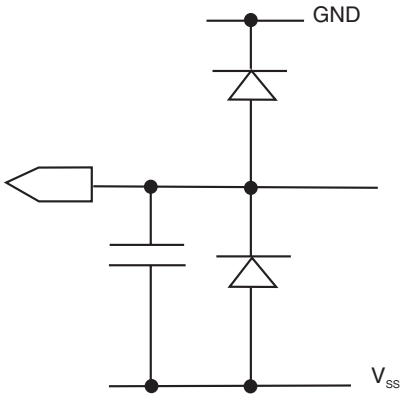
Analogue and Clock Inputs



Data Outputs



ADC Gain Adjust Input



DRRB, B/GB and PGEB Inputs

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.
(b) High and Low Temperature Electrical Measurement failures shall not be counted for Lot Failure.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test	-	3014	Verify Truth Table f_{IN}=695MHz f_{CLK}=1.4Gsps V_{DD}=5V, V_{SS}=-5V V_{DD}=1.45V DV_{SS}=-5V	-	-	-
Low Level Input Current, B/GB Input	I_{IL1}	3009	V_{IN}(B/GB)=-5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	500	800	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Input Current, DECB/DIODE Input	I_{IL2}	3009	V_{IN}(DIODE)=-5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	1	2.5	mA
Low Level Input Current, PGEB Input	I_{IL3}	3009	V_{IN}(PGEB)=-5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	500	800	µA
Low Level Input Current, DRRB Input	I_{IL4}	3009	V_{IN}(DRRB)=-1.8V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	100	600	µA
Low Level Input Current, SDAEN Input	I_{IL5}	3009	V_{IN}(SDAEN)=-5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	500	800	µA
Low Level Input Current, GA Input	I_{IL6}	3009	V_{IN}(GA)=-0.5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	0	4	µA
Low Level Input Current, SDA Input	I_{IL7}	3009	V_{IN}(SDA)=-0.5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	0	4	µA
High Level Input Current, B/GB Input	I_{IH1}	3010	V_{IN}(B/GB)=0V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	100	500	µA
High Level Input Current, DECB/DIODE Input	I_{IH2}	3010	V_{IN}(DIODE)=0V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	-2	500	µA
High Level Input Current, PGEB Input	I_{IH3}	3010	V_{IN}(PGEB)=0V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	100	500	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Current, DRRB Input	I_{IH4}	3010	V_{IN}(DRRB)=0V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	-50	200	µA
High Level Input Current, SDAEN Input	I_{IH5}	3010	V_{IN}(SDAEN)=0V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	100	500	µA
High Level Input Current, GA Input	I_{IH6}	3010	V_{IN}(GA)=0.5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	0	4	µA
High Level Input Current, SDA Input	I_{IH7}	3010	V_{IN}(SDA)=0.5V V_{IN}(CLK)=Open V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	0	10	µA
V_{IN} Input Resistance	R_{IN}	-	V_{IN}(A)=250mV V_{IN}(B)=0V via 50Ω Resistor V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	45	55	Ω
ECL Mode Low Level Output Voltage, D0 to D9 and OR Outputs	V_{OL1}	3007	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	-	-1.1	V
ECL Mode Low Level Output Voltage, D0B to D9B and ORB Outputs	V_{OL2}	3007	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	-	-1.1	V
LVDS Mode Low Level Output Voltage, D0 to D9 and OR Outputs	V_{OL3}	3007	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	0.75	1.18	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
LVDS Mode Low Level Output Voltage, D0B to D9B and ORB Outputs	V_{OL4}	3007	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	0.75	1.18	V
ECL Mode High Level Output Voltage D0 to D9 and OR Outputs	V_{OH1}	3006	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	-0.99	-	V
ECL Mode High Level Output Voltage, D0B to D9B and ORB Outputs	V_{OH2}	3006	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	-0.99	-	V
LVDS Mode High Level Output Voltage, D0 to D9 and OR Outputs	V_{OH3}	3006	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	1.18	1.425	V
LVDS Mode High Level Output Voltage, D0B to D9B and ORB Outputs	V_{OH4}	3006	V_{IN}(A)=-0.3V (DC) f_{CLK}=390Msps V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	1.18	1.425	V
ECL Mode Differential Output Voltage Swing (Signed Value)	V_{OD1}	-	Note 3	200	300	mV
LVDS Mode Differential Output Voltage Swing (Signed Value)	V_{OD2}	-	Note 3	200	450	mV
ECL Mode Common Mode Output Voltage	V_{CM1}	-	Note 3	-1.15	-0.95	V
LVDS Mode Common Mode Output Voltage	V_{CM2}	-	Note 3	0.95	1.275	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
ECL Mode Analogue Positive Supply Current 1	I_{DD1}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=-0.8V DV_{SS}=-5.25V Note 2	40	150	mA
ECL Mode Analogue Negative Supply Current 1	I_{SS1}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=-0.8V DV_{SS}=-5.25V Note 2	450	750	mA
ECL Mode Digital Positive Supply Current 1	I_{DVDD1}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=-0.8V DV_{SS}=-5.25V Note 2	50	200	mA
ECL Mode Digital Negative Supply Current 1	I_{DVSS1}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=-0.8V DV_{SS}=-5.25V Note 2	50	200	mA
LVDS Mode Analogue Positive Supply Current 2	I_{DD2}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=1.45V DV_{SS}=-5.25V Note 2	40	150	mA
LVDS Mode Analogue Negative Supply Current 2	I_{SS2}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=1.45V DV_{SS}=-5.25V Note 2	450	750	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
LVDS Mode Digital Positive Supply Current 2	I_{DVDD2}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=1.45V DV_{SS}=-5.25V Note 2	50	300	mA
LVDS Mode Digital Negative Supply Current 2	I_{DVSS2}	3005	f_{IN}=20MHz f_{CLK}=43.75MHz V_{DD}=5.25V V_{SS}=-5.25V DV_{DD}=1.45V DV_{SS}=-5.25V Note 2	50	300	mA
ECL Mode Power Consumption	P_{ECL}	-	Note 4	3	4.9	W
LVDS Mode Power Consumption	P_{LVDS}	-	Note 4	3	6	W
Data Ready Frequency with Decimation by 32	f_{DRD}	-	f_{CLK}=1.4GHz V_{IN}(DIODE)=-4V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	21.87	21.88	MHz
Decimation Factor 32	DF_{32}	-	f_{CLK}=1.4GHz V_{IN}(DIODE)=-4V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	31.96	32.04	-
Data Ready Frequency Without Decimation	f_{DR}	-	f_{CLK}=43.75MHz V_{IN}(DIODE)=0V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	21.87	21.88	MHz
Decimation Factor 1	DF_1	-	f_{CLK}=43.75MHz V_{IN}(DIODE)=0V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	0.96	1.04	-
Functional Test-Pattern Generator	-	3014	f_{CLK}=1.4GHz V_{IN}(A)=0V V_{IN}(DIODE)=-4V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Gain at Nominal Amplification	G_{TYP}	-	f_{CLK}=1.4Gsps V_{IN}(A)= ±0.2V V_{IN}(GA)=0V V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	0.9	1.1	-
Minimum Gain	G_{MIN}	-	f_{CLK}=1.4Gsps V_{IN}(A)= ±0.2V V_{IN}(GA)=-500mV V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-	0.995	-
Maximum Gain	G_{MAX}	-	f_{CLK}=1.4Gsps V_{IN}(A)= ±0.2V V_{IN}(GA)=500mV V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	1.0015	-	-
ECL Mode Effective Number of Bits, Gray Output 1	$ENOB_1$	-	f_{CLK}=1.4Gsps f_{IN}=100MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	7.3	-	Bit
LVDS Mode Effective Number of Bits, Gray Output 2	$ENOB_2$	-	f_{CLK}=1.4Gsps f_{IN}=695MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Notes 2, 5	7	-	Bit
ECL Mode Signal to Noise Ratio, Gray Output	SNR	-	f_{CLK}=1.4Gsps f_{IN}=100MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	49	-	dBc

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
ECL Mode Total Harmonic Distortion, Gray Output 1	THD_1	-	f_{CLK}=1.4Gsps f_{IN}=100MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	46	-	dBc
LVDS Mode Total Harmonic Distortion, Gray Output 2	THD_2	-	f_{CLK}=1.4Gsps f_{IN}=695MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	46	-	dBc
ECL Mode Spurious Free Dynamic Range, Gray Output 1	$SFDR_1$	-	f_{CLK}=1.4Gsps f_{IN}=100MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=-0.8V DV_{SS}=-5V Note 2	48	-	dBc
LVDS Mode Spurious Free Dynamic Range, Gray Output 2	$SFDR_2$	-	f_{CLK}=1.4Gsps f_{IN}=695MHz P_{IN}=-1dBFS V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	50	-	dBc
Minimum Differential Non-Linearity	DNL_{MIN}	-	f_{CLK}=390Msps f_{IN}=100MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-1	-	LSB
Maximum Differential Non-Linearity	DNL_{MAX}	-	f_{CLK}=390Msps f_{IN}=100MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-	1.5	LSB
RMS Differential Non-Linearity	DNL_{rms}	-	f_{CLK}=390Msps f_{IN}=100MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-	0.3	LSB

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Minimum Integral Non-Linearity	INL_{MIN}	-	f_{CLK}=390Msps f_{IN}=100MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-4	-	LSB
Maximum Integral Non-Linearity	INL_{MAX}	-	f_{CLK}=390Msps f_{IN}=100MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-	4	LSB
Input Offset Voltage	V_{IO}	-	f_{CLK}=1.4Gsps f_{IN}=695MHz V_{DD}=5V, V_{SS}=-5V DV_{DD}=1.45V DV_{SS}=-5V Note 2	-9	9	mV

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. All outputs are 50Ω Transmission Lines differentially terminated into 100Ω (2 x 50Ω) via 47pF capacitors to 0V.
3. Calculated from the V_{OH} and V_{OL} measurements.
4. Calculated from the Supply Current measurements.
5. This limit is defined by correlation and not tested, due to test equipment limitation.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5)°C and T_{amb}=- 55(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements, except that the Low Level Input Current DECB/DIODE Input (I_{IL2}) shall only be tested at Room Temperature.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics Note 1	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
ECL Mode Low Level Output Voltage, D0 Output	V_{OL1}	+0.02, -0	-	-1.1	V
ECL Mode Low Level Output Voltage, D0B Output	V_{OL2}	+0.02, -0	-	-1.1	V
ECL Mode High Level Output Voltage, D0 Output	V_{OH1}	-0.02, +0	-0.99	-	V
ECL Mode High Level Output Voltage, D0B Output	V_{OH2}	-0.02, +0	-0.99	-	V
ECL Mode Differential Output Voltage Swing (Signed Value)	V_{OD1}	±20	200	300	mV
ECL Mode Common Mode Output Voltage, D0 and D0B Outputs	V_{CM1}	±0.02	-1.15	-0.95	V
ECL Mode Analogue Positive Supply Current 1	I_{DD1}	±5%	40	150	mA
ECL Mode Analogue Negative Supply Current 1	I_{SS1}	±5%	450	750	mA
ECL Mode Digital Positive Supply Current 1	I_{DVDD1}	±5%	50	200	mA
ECL Mode Digital Negative Supply Current 1	I_{DVSS1}	±5%	50	200	mA
ECL Mode Power Consumption	P_{ECL}	±5%	3	4.9	W
Gain at Nominal Amplification	G_{TYP}	±5%	0.9	1.1	-
ECL Mode Effective Number of Bits, Gray Output	$ENOB_1$	–0.4, +0	7.3	-	Bit
LVDS Mode Effective Number of Bits, Gray Output	$ENOB_2$	–0.4, +0	7	-	Bit
ECL Mode Signal to Noise Ratio	SNR	-4, +0	49	-	dBc
ECL Mode Total Harmonic Distortion, Gray Output	THD_1	-4, +0	46	-	dBc
LVDS Mode Total harmonic Distortion, Gray Output	THD_2	-4, +0	46	-	dBc
ECL Mode Spurious Free Dynamic Range, Gray Output	$SFDR_1$	-4, +0	48	-	dBc
LVDS Mode Spurious Free Dynamic Range, Gray Output	$SFDR_1$	-4, +0	50	-	dBc
Minimum Differential Non-Linearity	DNL_{MIN}	-0.5, +0	-1	-	LSB
Maximum Differential Non-Linearity	DNL_{MAX}	+0.5, +0	-	1.5	LSB
RMS Differential Non-Linearity	DNL_{rms}	+0.5, +0	-	0.3	LSB

Characteristics Note 1	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Minimum Integral Non-Linearity	INL_{MIN}	-0.5, +0	-4	-	LSB
Maximum Integral Non-Linearity	INL_{MAX}	+0.5, +0	-	4	LSB
Input Offset Voltage	V_{IO}	±5	-9	9	mV

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Junction Temperature	T_J	+125 (-5 +10)	°C
Clock Frequency	f_{CLK}, f_{CLKB}	625	kHz
Input Voltage, A Input	V_A	±250	mV
Input Frequency, A Input	f_{IN}	312	kHz
Input Voltage, B Input	V_B	0	V
Analogue Positive Supply Voltage	V_{DD}	5.3	V
Analogue Negative Supply Voltage	V_{SS}	-5.3	V
Digital Positive Supply Voltage	DV_{DD}	1.5	V
Digital Negative Supply Voltage	DV_{SS}	-5.3	V

NOTES:
1. The SDA, DRRB, SDAEN and GA inputs shall be connected to ground via 50Ω resistors.
2. All outputs shall be connected to ground via 50Ω Loads.
3. Decoupling capacitors of 100pF in parallel with 10nF shall be connected to all supplies at each burn-in position.
4. Decoupling capacitors of 1µF in parallel with 10nF shall be connected to all supplies on each burn-in board.
5. The PGEB input shall be connected to ground.
6. The B/GB and DECB/DIODE inputs shall be open circuit.
7. The CLK, CLKB and B inputs shall have 50Ω input protection resistors.
8. The A input shall have a series 100nF capacitor and a 50Ω input resistor.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in, performed without the Solder Column Interposer (SCI).

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	^{o}C
Clock Frequency	f_{CLK}	625	kHz
Input Voltage, A Input	V_A	±250	mV
Input Frequency, B Input	f_{IN}	312	kHz
Analogue Positive Supply Voltage	V_{DD}	5.25	V
Analogue Negative Supply Voltage	V_{SS}	-5.25	V
Digital Positive Supply Voltage	DV_{DD}	2.4	V
Digital Negative Supply Voltage	DV_{SS}	-5.25	V

NOTES:

1. The same bias configuration as the Power Burn-in shall apply.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb}=22±3˚C. The test methods and test conditions shall be as per the corresponding test defined in electrical measurements at Room Temperature.

The parameters to be measured during and on completion of radiation testing are shown below. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbol	Limits		Units
		Min.	Max.	
Input Resistance, A Input	R_{INA}	45	55	Ω
ECL Mode Low Level Output Voltage, D7 to D9 Outputs	V_{OL1}	-	-1.1	V
ECL Mode Low Level Output Voltage, D7B to D9B Outputs	V_{OL2}	-	-1.1	V

Characteristics	Symbol	Limits		Units
		Min.	Max.	
LVDS Mode Low Level Output Voltage, D7 to D9 Outputs	V_{OL3}	0.75	1.18	V
LVDS Mode Low Level Output Voltage, D7B to D9B Outputs	V_{OL4}	0.75	1.18	V
ECL Mode High Level Output Voltage, D7 to D9 Outputs	V_{OH1}	-0.99	-	V
ECL Mode High Level Output Voltage, D7B to D9B Outputs	V_{OH2}	-0.99	-	V
LVDS Mode High Level Output Voltage, D7 to D9 Outputs	V_{OH3}	1.18	1.425	V
LVDS Mode High Level Output Voltage, D7B to D9B Outputs	V_{OH4}	1.18	1.425	V
ECL Mode Analogue Positive Supply Current 1	I_{DD1}	40	150	mA
ECL Mode Analogue Negative Supply Current 1	I_{SS1}	450	750	mA
ECL Mode Digital Positive Supply Current 1	I_{DVDD1}	50	200	mA
ECL Mode Digital Negative Supply Current 1	I_{DVSS1}	50	200	mA
LVDS Mode Analogue Positive Supply Current 2	I_{DD2}	40	150	mA
LVDS Mode Analogue Negative Supply Current 2	I_{SS2}	450	750	mA
LVDS Mode Digital Positive Supply Current 2	I_{DVDD2}	50	300	mA
LVDS Mode Digital Negative Supply Current 2	I_{DVSS2}	50	300	mA
ECL Mode Power Consumption	P_{ECL}	3	4.9	W
LVDS Mode Power Consumption	P_{LDVS}	3	6	W
ECL Mode Effective Number of Bits, Gray Output 1	$ENOB_1$	7.3	-	Bit
LVDS Mode Effective Number of Bits, Gray Output 2	$ENOB_2$	7	-	Bit
ECL Mode Signal to Noise Ratio, Gray Output	SNR	49	-	dBc
ECL Mode Total Harmonic Distortion, Gray Output 1	THD_1	46	-	dBc
LVDS Mode Total Harmonic Distortion, Gray Output 2	THD_2	46	-	dBc

Characteristics	Symbol	Limits		Units
		Min.	Max.	
ECL Mode Spurious Free Dynamic Range, Gray Output 1	$SFDR_1$	48	-	dBc
LVDS Mode Spurious Free Dynamic Range, Gray Output 2	$SFDR_2$	50	-	dBc
Minimum Differential Non-Linearity	DNL_{MIN}	-1	-	LSB
Maximum Differential Non-Linearity	DNL_{MAX}	-	1.5	LSB
RMS Differential Non-Linearity	DNL_{rms}	-	0.3	LSB
Minimum Integral Non-Linearity	INL_{MIN}	-4	-	LSB
Maximum Integral Non-Linearity	INL_{MAX}	-	4	LSB