



Pages 1 to 30

**INTEGRATED CIRCUITS, SILICON MONOLITHIC, HCMOS**

**TRIPLE 2-CHANNEL ANALOGUE**

**MULTIPLEXER/DEMULTIPLEXER**

**BASED ON TYPE 54HC4053**

**ESCC Detail Specification No. 9408/065**

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DCR No.	CHANGE DESCRIPTION
245, 447, 551, 612	Specification upissued to incorporate editorial and technical changes per DCR.

**TABLE OF CONTENTS**

<b>1.</b>	<b><u>GENERAL</u></b>	<b>5</b>
1.1	Scope	5
1.2	Applicable Documents	5
1.3	Terms, Definitions, Abbreviations, Symbols and Units	5
1.4	The ESCC Component Number and Component Type Variants	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	Maximum Ratings	6
1.6	Handling Precautions	6
1.7	Physical Dimensions and Terminal Identification	7
1.7.1	Flat Package (FP) - 16 Pin	7
1.7.2	Dual-in-line Package (DIP) - 16 Pin	8
1.7.3	Chip Carrier Package (CCP) - 20 Terminal	9
1.7.4	Small Outline Ceramic Package (SO) - 16 Pin	11
1.7.5	Notes to Physical Dimensions and Terminal Identification	12
1.8	Functional Diagram	12
1.9	Pin Assignment	13
1.10	Truth Table	13
1.11	Protection Networks	14
<b>2.</b>	<b><u>REQUIREMENTS</u></b>	<b>15</b>
2.1	General	15
2.1.1	Deviations from the Generic Specification	15
2.2	Marking	15
2.3	Electrical Measurements at Room, High and Low Temperatures	15
2.3.1	Room Temperature Electrical Measurements	15
2.3.2	High and Low Temperatures Electrical Measurements	20
2.3.3	Notes to Electrical Measurement Tables	22
2.4	Parameter Drift Values	24
2.5	Intermediate and End-Point Electrical Measurements	24
2.6	High Temperature Reverse Bias Burn-in Conditions	25
2.6.1	N-Channel HTRB	25
2.6.2	P-Channel HTRB	26
2.7	Power Burn-in Conditions	26
2.8	Operating Life Conditions	28
2.9	Total Dose Radiation Testing	28
2.9.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	28
2.9.2	Electrical Measurements for Total Dose Radiation Testing	29
	APPENDIX 'A'	30

**1. GENERAL**

**1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

**1.2 APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000.
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

**1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

**1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS**

**1.4.1 The ESCC Component Number**

The ESCC Component number shall be constituted as follows:

Example: 940806501F

- Detail Specification Reference: 9408065
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: F (as required)

**1.4.2 Component Type Variants**

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g	Total Dose Radiation Level Letter
01	54HC4053	FP	G2	0.7	F [50kRAD(Si)]
02	54HC4053	FP	G4	0.7	F [50kRAD(Si)]
05	54HC4053	CCP	2	0.6	F [50kRAD(Si)]
10	54HC4053	DIP	G2	2.2	F [50kRAD(Si)]
11	54HC4053	DIP	G4	2.2	F [50kRAD(Si)]
12	54HC4053	SO	G2	0.7	F [50kRAD(Si)]
13	54HC4053	SO	G4	0.7	F [50kRAD(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 **MAXIMUM RATINGS**

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	$V_{DD}$	-0.5 to 7	V	Note 1
Supply Voltage Range	$V_{DD}-V_{EE}$	-0.5 to 13	V	Note 2
Control Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V	Notes 1, 3
Channel Input/Output Voltage	$V_{IN}$	$V_{EE} - 0.5$ to $V_{DD} + 0.5$	V	Notes 2, 4
Device Power Dissipation (Continuous)	$P_D$	300	mW	Note 5
Supply Current	$I_{DDop}$	50	mA	
Operating Temperature Range	$T_{op}$	-55 to +125	°C	$T_{amb}$
Storage Temperature Range	$T_{stg}$	-65 to +150	°C	
Soldering Temperature For FP, DIP and SO For CCP	$T_{sol}$	+265 +245	°C	Note 6 Note 7

**NOTES:**

1. Device is functional for  $2V \leq V_{DD} \leq 6V$  with reference to  $V_{SS}$ .
2. Device is functional for  $2V \leq V_{DD} - V_{EE} \leq 12V$ ,  $-6V \leq V_{EE} \leq 0V$
3. Input current limited to  $I_{IC} = \pm 20mA$
4. Channel Input/Output Clamp Current limited to  $I_{IC} = \pm 20mA$ . Channel Input/Output Through Current limited to  $I_{CH} = \pm 25mA$ .
5. The maximum device dissipation is determined by  $I_{DDop} \max (50mA) \times 6V$ .
6. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
7. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 **HANDLING PRECAUTIONS**

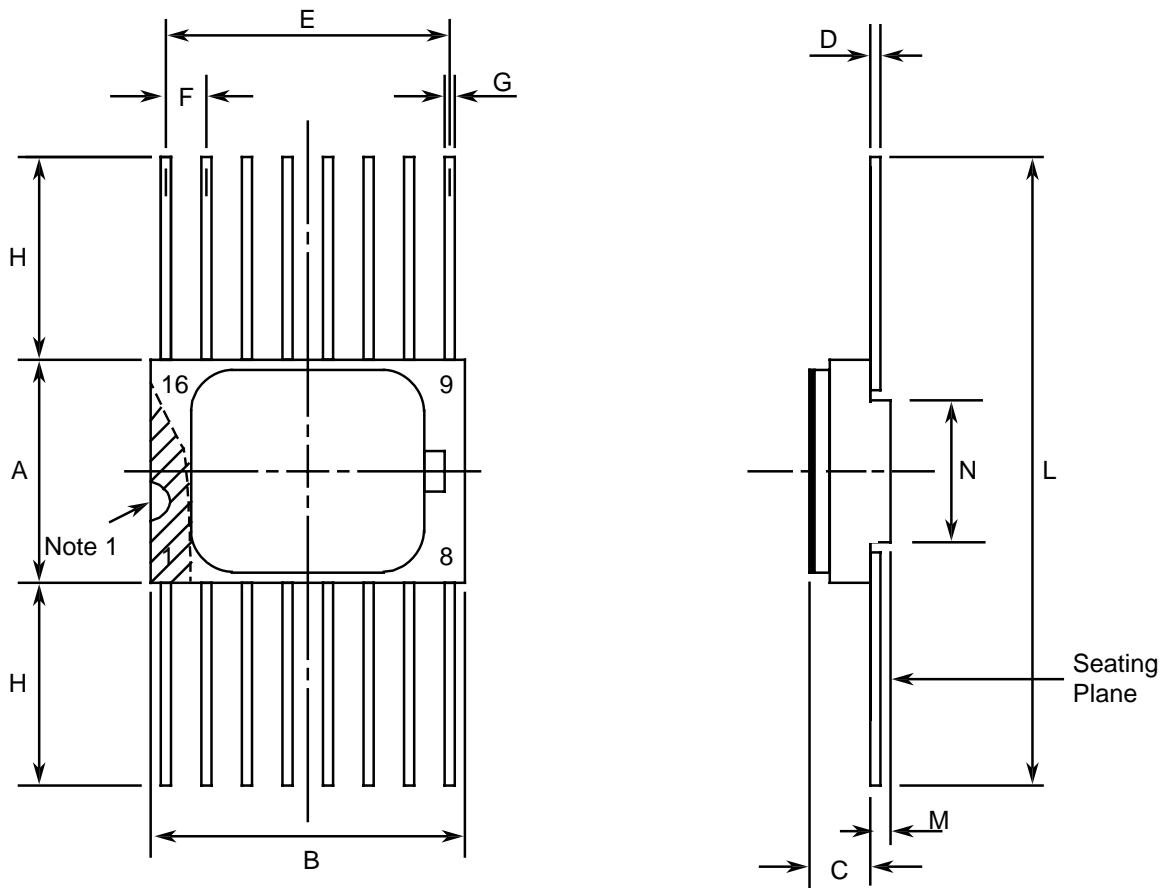
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.7 **PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION**

Consolidated Notes are given following the case drawings and dimensions.

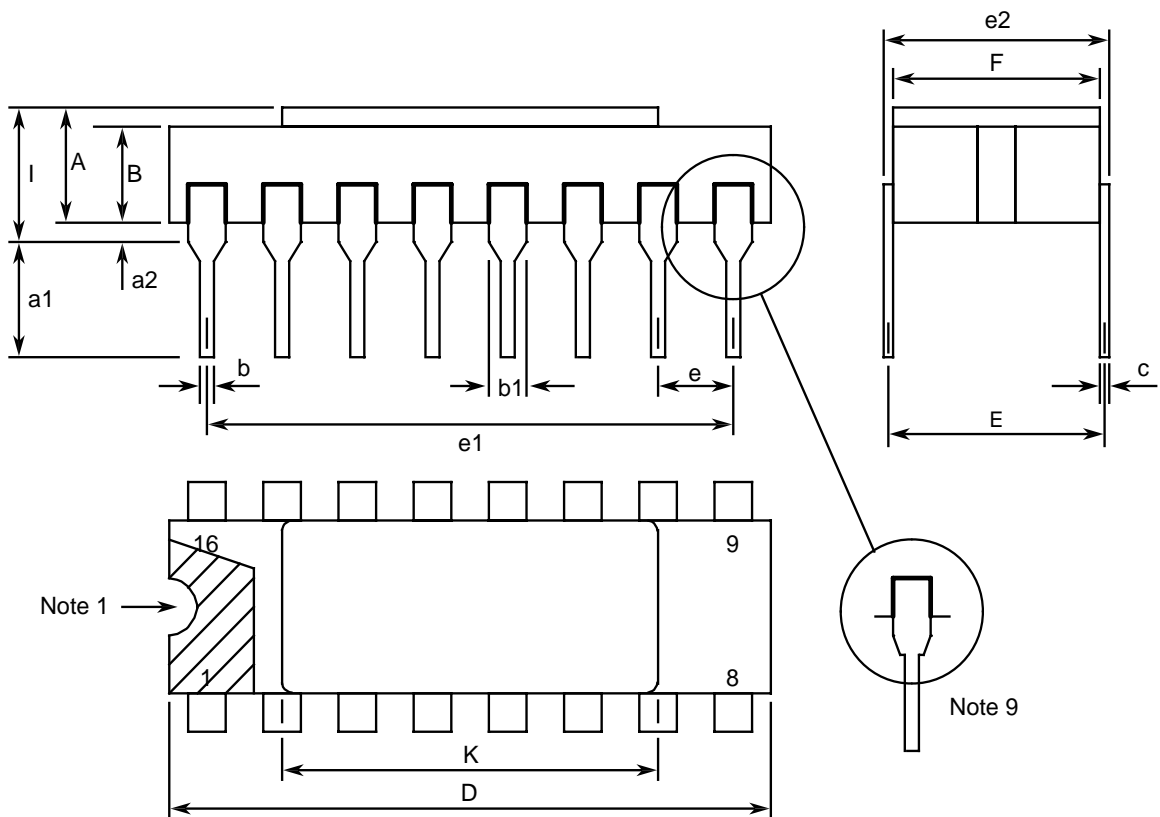
1.7.1 **Flat Package (FP) - 16 Pin**



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	

Symbols	Dimensions mm		Notes
	Min	Max	
N	4.32 TYPICAL		

1.7.2 Dual-in-line Package (DIP) - 16 Pin

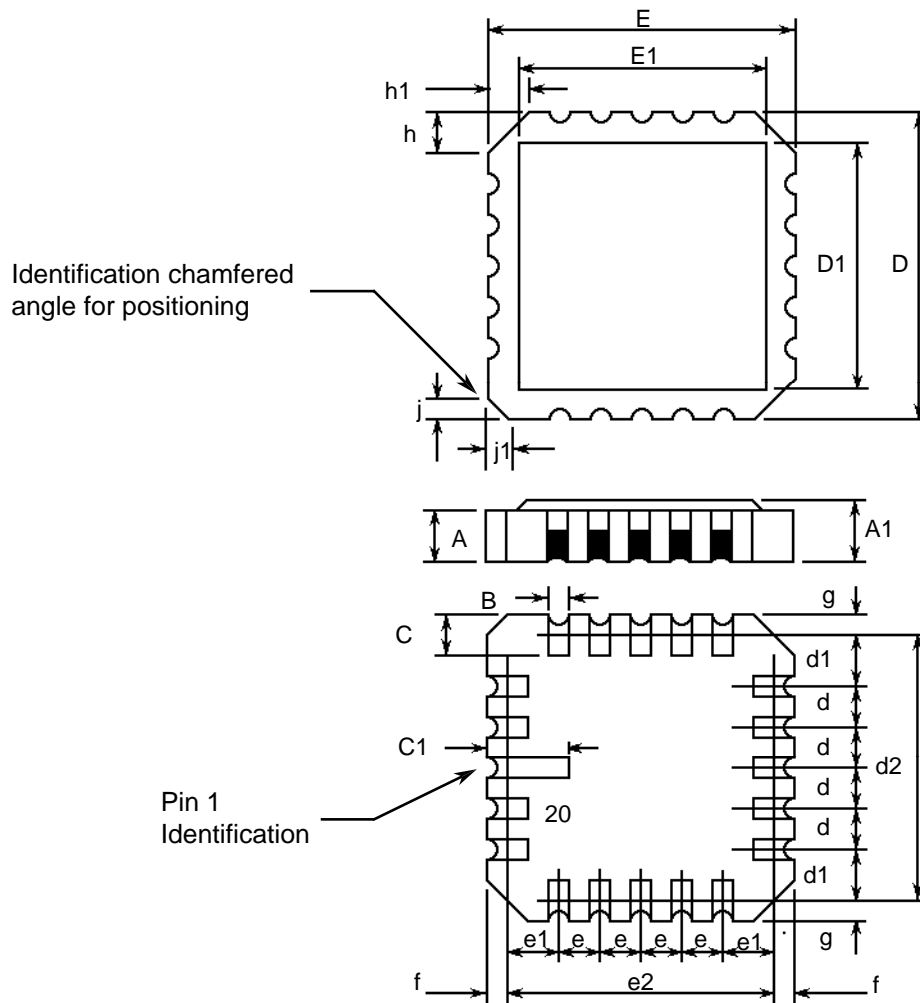


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.71	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.4	0.5	5
b1	1.14	1.5	5
c	0.2	0.3	5
D	20.06	20.58	
E	7.36	7.87	



Symbols	Dimensions mm		Notes
	Min	Max	
e	2.54 BSC		4, 6
e1	17.65	17.9	
e2	7.62	8.12	
F	7.29	7.7	
l	-	3.83	
K	10.9	12.1	

1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 BSC		3
d2	7.62 BSC		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 BSC		3
e2	7.62 BSC		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

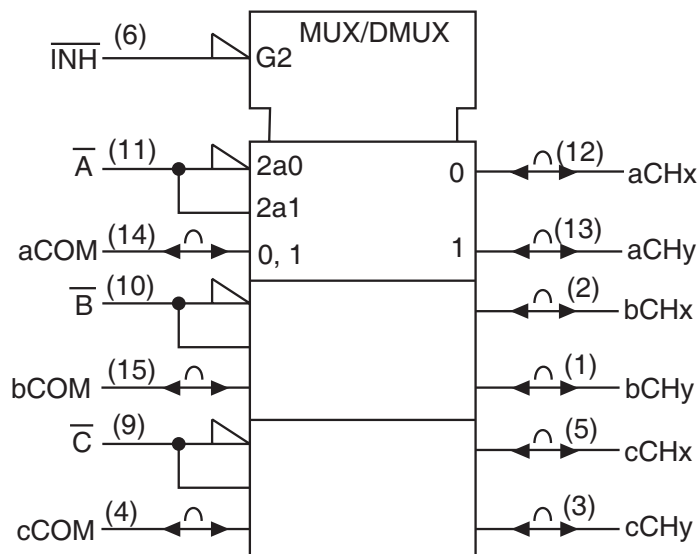
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within  $\pm 0.13\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within  $\pm 0.25\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	bCHy Input/ Output (Channel)	-	11	$\bar{A}$ Input (Select)	-
2	bCHx Input/ Output (Channel)	bCHy Input/ Output (Channel)	12	aCHx Input/ Output (Channel)	$\bar{C}$ Input (Select)
3	cCHy Input/ Output (Channel)	bCHx Input/ Output (Channel)	13	aCHy Input/ Output (Channel)	$\bar{B}$ Input (Select)
4	cCOM Output/Input (Common)	cCHy Input/ Output (Channel)	14	aCOM Output/Input (Common)	$\bar{A}$ Input (Select)
5	cCHx Input/ Output (Channel)	cCOM Output/Input (Common)	15	bCOM Output/Input (Common)	aCHx Input/ Output (Channel)
6	$\overline{INH}$ Input (Inhibit)	-	16	$V_{DD}$	-
7	$V_{EE}$ (Analogue Negative Supply)	cCHx Input/ Output (Channel)	17	-	aCHy Input/ Output (Channel)
8	$V_{SS}$ (Digital Negative Supply)	$\overline{INH}$ Input (Inhibit)	18	-	aCOM Output/Input (Common)
9	$\bar{C}$ Input (Select)	$V_{EE}$ (Analogue Negative Supply)	19	-	bCOM Output/Input (Common)
10	$\bar{B}$ Input (Select)	$V_{SS}$ (Digital Negative Supply)	20	-	$V_{DD}$

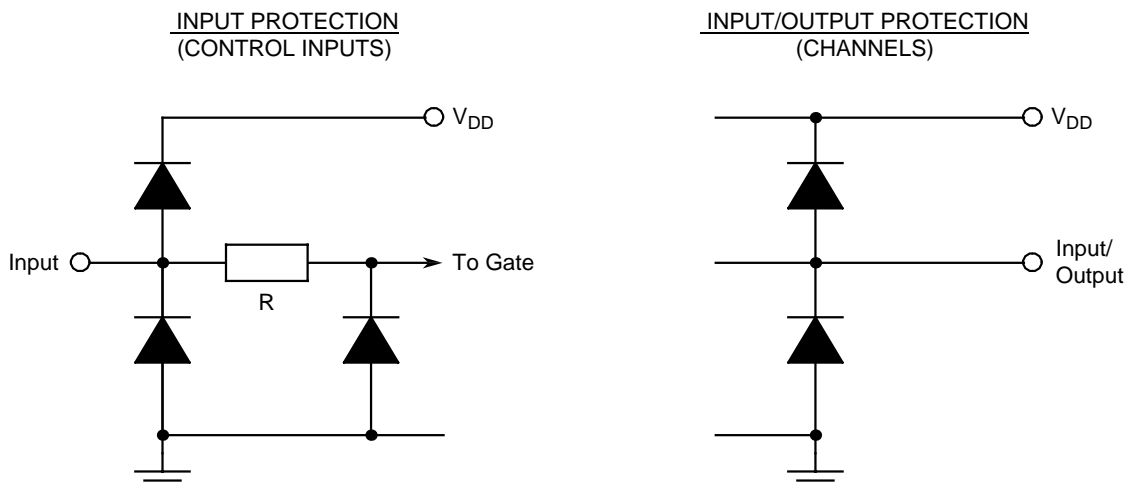
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.

CONTROL INPUTS				ON CHANNELS
$\overline{INH}$	SELECT			
	$\bar{A}$	$\bar{B}$	$\bar{C}$	
L	L	L	L	aCHx to aCOM, aCOM to aCHx bCHx to bCOM, bCOM to bCHx cCHx to cCOM, cCOM to cCHx
L	L	L	H	aCHx to aCOM, aCOM to aCHx bCHx to bCOM, bCOM to bCHx cCHy to cCOM, cCOM to cCHy

CONTROL INPUTS				ON CHANNELS
$\overline{\text{INH}}$	SELECT			
	$\overline{\text{A}}$	$\overline{\text{B}}$	$\overline{\text{C}}$	
L	L	H	L	aCHx to aCOM, aCOM to aCHx bCHy to bCOM, bCOM to bCHy cCHx to cCOM, cCOM to cCHx
L	L	H	H	aCHx to aCOM, aCOM to aCHx bCHy to bCOM, bCOM to bCHy cCHy to cCOM, cCOM to cCHy
L	H	L	L	aCHy to aCOM, aCOM to aCHy bCHx to bCOM, bCOM to bCHx cCHx to cCOM, cCOM to cCHx
L	H	L	H	aCHy to aCOM, aCOM to aCHy bCHx to bCOM, bCOM to bCHx cCHy to cCOM, cCOM to cCHy
L	H	H	L	aCHy to aCOM, aCOM to aCHy bCHy to bCOM, bCOM to bCHy cCHx to cCOM, cCOM to cCHx
L	H	H	H	aCHy to aCOM, aCOM to aCHy bCHy to bCOM, bCOM to bCHy cCHy to cCOM, cCOM to cCHy
H	X	X	X	NONE (High Impedance)

1.11 PROTECTION NETWORKS



**2. REQUIREMENTS**

**2.1 GENERAL**

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

**2.1.1 Deviations from the Generic Specification**

None.

**2.2 MARKING**

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

**2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES**

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

**2.3.1 Room Temperature Electrical Measurements**

The measurements shall be performed at  $T_{amb}=+22 \pm 3^{\circ}C$ .

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table $V_{IL}=0.3V, V_{IH}=1.5V$ $V_{DD}=2V$ $V_{SS} = V_{EE} =0V$ $t_r < 1\mu s$ Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table $V_{IL}=0.9V, V_{IH}=3.15V$ $V_{DD}=4.5V$ $V_{SS} = V_{EE} =0V$ $t_r = t_f < 500ns$ Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3	-	3014	Verify Truth Table $V_{IL}=1.2V, V_{IH}=4.2V$ $V_{DD}=6V$ $V_{SS} = V_{EE} =0V$ $t_r=t_f<400ns$ Note 2	-	-	-
Quiescent Current	$I_{DD}$	3005	$V_{IL}=0V, V_{IH}=6V$ $V_{DD}=6V, V_{SS}=0V$ Note 3	-	400	nA
Low Level Input Current, Control Inputs	$I_{IL}$	3009	$V_{IN}(\text{Under Test})=0V$ $V_{IN}(\text{Remaining Inputs})=6V$ $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	-50	nA
High Level Input Current, Control Inputs	$I_{IH}$	3010	$V_{IN}(\text{Under Test})=6V$ $V_{IN}(\text{Remaining Inputs})=0V$ $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	50	nA
Channel OFF Leakage Current 1, Any Channel CH	$I_{OFF1}$	-	$V_{IL} =0V, V_{IH}=6V$ Channel Under Test: $V_{IN}(\text{CH})=6V$ $V_{IN}(\text{COM}) =0V$ All Other Channels Open $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	-100	nA
Channel OFF Leakage Current 2, Any Channel CH	$I_{OFF2}$	-	$V_{IL} =0V, V_{IH}=6V$ Channel Under Test: $V_{IN}(\text{CH})=0V$ $V_{IN}(\text{COM}) =6V$ All Other Channels Open $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	100	nA
Channel OFF Leakage Current 3, All Channels Tested Together	$I_{OFF3}$	-	$V_{IL} =0V, V_{IH}=6V$ $V_{IN}(\text{CH})=0V$ $V_{IN}(\text{COM}) = 6V$ $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	100	nA
Channel OFF Leakage Current 4, All Channels Tested Together	$I_{OFF4}$	-	$V_{IL} =0V, V_{IH}=6V$ $V_{IN}(\text{CH})=6V$ $V_{IN}(\text{COM}) = 0V$ $V_{DD}=6V$ $V_{SS}= V_{EE} =0V$	-	-100	nA



Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Channel ON Resistance 1	$R_{ON1}$	-	$V_{IL}=0V, V_{IH}=3.15V$ $V_{DD}=4.5V$ $V_{SS}=V_{EE}=0V$ Note 4	-	180	$\Omega$
Channel ON Resistance 2	$R_{ON2}$	-	$V_{IL}=0V, V_{IH}=4.2V$ $V_{DD}=6V$ $V_{SS}=V_{EE}=0V$ Note 4	-	160	$\Omega$
Channel ON Resistance Matching 1	$\Delta R_{ON1}$	-	Note 4	-20	+20	$\Omega$
Channel ON Resistance Matching 2	$\Delta R_{ON2}$	-	Note 4	-20	+20	$\Omega$
Threshold Voltage N-Channel	$V_{THN}$	-	$\overline{INH}$ input and $V_{EE}$ at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	-	$\overline{INH}$ input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=V_{EE}=-5V$ $I_{DD}=10\mu A$	0.45	1.35	V
Input Clamp Voltage 1, to $V_{SS}$ and Control Inputs	$V_{IC1}$	-	$I_{IN}$ (Under Test) = $-100\mu A$ $V_{DD}=\text{Open}, V_{SS}=0V$ All Other Pins Open	-400	-900	mV
Input Clamp Voltage 2, to $V_{DD}$ and Control Inputs	$V_{IC2}$	-	$I_{IN}$ (Under Test) = $100\mu A$ $V_{DD}=0V, V_{SS}=\text{Open}$ All Other Pins Open	400	900	mV
Input Clamp Voltage 3, to $V_{SS}$ , COM and CH Inputs	$V_{IC3}$	-	$I_{IN}$ (Under Test) = $-100\mu A$ $V_{DD}=\text{Open}, V_{SS}=0V$ All Other Pins Open	-200	-900	mV
Input Clamp Voltage 4, to $V_{DD}$ , COM and CH Inputs	$V_{IC4}$	-	$I_{IN}$ (Under Test) = $100\mu A$ $V_{DD}=0V, V_{SS}=\text{Open}$ All Other Pins Open	200	900	mV
Input Capacitance, Control Inputs	$C_{IN}$	3012	$V_{IN}$ (Not Under Test) = $0V$ $V_{DD}=V_{SS}=V_{EE}=0V$ $f = 100 \text{ kHz to } 1 \text{ MHz}$ Note 5	-	10	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input or Output Capacitance, CH inputs	$C_{CH}$	3012	$V_{IN}$ (Not Under Test) = 0V $V_{DD} = V_{SS} = V_{EE} = 0V$ $f = 100 \text{ kHz to } 1 \text{ MHz}$ Note 5	-	10	pF
Output or Input Capacitance, COM inputs	$C_{COM}$	3012	$V_{IN}$ (Not Under Test) = 0V $V_{DD} = V_{SS} = V_{EE} = 0V$ $f = 100 \text{ kHz to } 1 \text{ MHz}$ Note 5	-	38	pF
Propagation Delay Low to High 1, bCHy to bCOM bCOM to bCHy	$t_{PLH1}$	3003	$V_{IN}$ (Under Test) = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL} = 0V, V_{IH} = 4.5V$ $V_{DD} = 4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	12	ns
Propagation Delay High to Low 1, bCHy to bCOM bCOM to bCHy	$t_{PHL1}$	3003	$V_{IN}$ (Under Test) = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL} = 0V, V_{IH} = 4.5V$ $V_{DD} = 4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	12	ns
Propagation Delay Low to High 2, $\bar{A}$ to aCOM (Channels ON)	$t_{PLH2}$	3003	$V_{IN} (\bar{A})$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IN}(aCHx) = 0.9V$ $V_{IN}(aCHy) = 3.15V$ $V_{IL} = 0V, V_{IH} = 4.5V$ $V_{DD} = 4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	44	ns
Propagation Delay High to Low 2, $\bar{A}$ to aCOM (Channels ON)	$t_{PHL2}$	3003	$V_{IN} (\bar{A})$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IN}(aCHx) = 0.9V$ $V_{IN}(aCHy) = 3.15V$ $V_{IL} = 0V, V_{IH} = 4.5V$ $V_{DD} = 4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	44	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Enable Time High Impedance to Low Output 1, $\bar{A}$ to aChy	$t_{PZL1}$	3003	$V_{IN}(\bar{A})$ = Pulse Generator $V_{IN}(\text{Remaining Inputs})$ $V_{IN}(aCOM)=0.9V$ = Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS}=V_{EE}=0V$ Note 6	-	44	ns
Output Enable Time High Impedance to Low Output 2, $\bar{INH}$ to aChx $\bar{INH}$ to aCOM	$t_{PZL2}$	3003	$V_{IN}(\bar{INH})$ = Pulse Generator $V_{IN}(\text{Remaining Inputs})$ = Truth Table $V_{IN}(aChx \text{ or } aCOM)=0.9V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS}=V_{EE}=0V$ Note 6	-	44	ns
Output Enable Time High Impedance to High Output 1, $\bar{A}$ to aChy	$t_{PZH1}$	3003	$V_{IN}(\bar{A})$ = Pulse Generator $V_{IN}(\text{Remaining Inputs})$ = Truth Table $V_{IN}(aCOM)=3.15V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS}=V_{EE}=0V$ Note 6	-	44	ns
Output Enable Time High Impedance to High Output 2, $\bar{INH}$ to aChx $\bar{INH}$ to aCOM	$t_{PZH2}$	3003	$V_{IN}(\bar{INH})$ = Pulse Generator $V_{IN}(\text{Remaining Inputs})$ = Truth Table $V_{IN}(aChx \text{ or } aCOM)=3.15V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS}=V_{EE}=0V$ Note 6	-	44	ns
Output Disable Time Low Output to High Impedance 1, $\bar{A}$ to aChy	$t_{PLZ1}$	3003	$V_{IN}(\bar{A})$ = Pulse Generator $V_{IN}(\text{Remaining Inputs})$ = Truth Table $V_{IN}(aCOM)=0.9V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS}=V_{EE}=0V$ Note 6	-	42	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Disable Time Low Output to High Impedance 2, $\overline{INH}$ to aCHx $\overline{INH}$ to aCOM	$t_{PLZ2}$	3003	$V_{IN}(\overline{INH})$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IN}(aCHx$ or $aCOM)=0.9V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	42	ns
Output Disable Time High Output to High Impedance 1, $\overline{A}$ to aCHy	$t_{PHZ1}$	3003	$V_{IN}(\overline{A})$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IN}(aCOM)=3.15V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	42	ns
Output Disable Time High Output to High Impedance 2 $\overline{INH}$ to aCHx $\overline{INH}$ to aCOM	$t_{PHZ2}$	3003	$V_{IN}(\overline{INH})$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IN}(aCHx$ or $aCOM)=3.15V$ $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V,$ $V_{SS} = V_{EE} = 0V$ Note 6	-	42	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at  $T_{amb}=+125 (+0 -5) ^\circ C$  and  $T_{amb}=- 55(+5-0)^\circ C$ .

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table $V_{IL}=0.3V, V_{IH}=1.5V$ $V_{DD}=2V$ $V_{SS} = V_{EE} = 0V$ $t_r < 1\mu s,$ Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table $V_{IL}=0.9V, V_{IH}=3.15V$ $V_{DD}=4.5V$ $V_{SS} = V_{EE} = 0V$ $t_r = t_f < 500ns$ Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3	-	3014	Verify Truth Table $V_{IL}=1.2V, V_{IH}=4.2V$ $V_{DD}=6V$ $V_{SS} = V_{EE} = 0V$ $t_r=t_f < 400ns$ Note 2	-	-	-
Quiescent Current	$I_{DD}$	3005	$V_{IL}=0V, V_{IH}=6V$ $V_{DD}=6V, V_{SS}=V_{EE} = 0V$ Note 3	-	8	$\mu A$
Low Level Input Current, Control inputs	$I_{IL}$	3009	$V_{IN}$ (Under Test)=0V $V_{IN}$ (Remaining Inputs)=6V $V_{DD}=6V, V_{SS} = V_{EE} = 0V$	-	-1	$\mu A$
High Level Input Current, Control inputs	$I_{IH}$	3010	$V_{IN}$ (Under Test)=6V $V_{IN}$ (Remaining Inputs)=0V $V_{DD}=6V, V_{SS}=V_{EE}=0V$	-	1	$\mu A$
Channel OFF Leakage Current 1, Any Channel CH	$I_{OFF1}$	-	$V_{IL} = 0V, V_{IH}=6V$ Channel Under Test: $V_{IN}$ (CH) =6V $V_{IN}$ (COM) =0V All Other Channels Open $V_{DD} = 6V$ $V_{SS} = V_{EE} = 0V$	-	-1	$\mu A$
Channel OFF Leakage Current 2, Any Channel CH	$I_{OFF2}$	-	$V_{IL} = 0V, V_{IH}=6V$ Channel Under Test: $V_{IN}$ (CH) =0V $V_{IN}$ (COM) =6V All Other Channels Open $V_{DD} = 6V$ $V_{SS} = V_{EE} = 0V$	-	1	$\mu A$
Channel OFF Leakage Current 3, All Channels Tested Together	$I_{OFF3}$	-	$V_{IL} = 0V, V_{IH}=6V$ $V_{IN}$ (CH) =0V $V_{IN}$ (COM) =6V $V_{DD} = 6V$ $V_{SS} = V_{EE} = 0V$	-	1	$\mu A$
Channel OFF Leakage Current 4, All Channels Tested Together	$I_{OFF4}$	-	$V_{IL} = 0V, V_{IH}=6V$ $V_{IN}$ (CH) =6V $V_{IN}$ (COM) =0V $V_{DD} = 6V$ $V_{SS} = V_{EE} = 0V$	-	-1	$\mu A$
Channel On Resistance 1	$R_{ON1}$	-	$V_{IL} = 0V, V_{IH}=3.15V$ $V_{DD} = 4.5V$ $V_{SS} = V_{EE} = 0V$ Note 4	-	270	$\Omega$

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Channel On Resistance 2	$R_{ON2}$	-	$V_{IL}=0V, V_{IH}=4.2V$ $V_{DD}=6V$ $V_{SS}=V_{EE}=0V$ Note 4	-	240	$\Omega$
Channel ON Resistance Matching 1	$\Delta R_{ON1}$	-	Note 4	-20	+20	$\Omega$
Channel ON Resistance Matching 2	$\Delta R_{ON2}$	-	Note 4	-20	+20	$\Omega$
Input Clamp Voltage 1, to $V_{SS}$ and Control Inputs	$V_{IC1}$	-	$I_{IN}$ (Under Test)= -100 $\mu A$ $V_{DD}$ =Open, $V_{SS}$ =0V All Other Pins Open	-0.1	-1.2	V
Input Clamp Voltage 2, to $V_{DD}$ and Control Inputs	$V_{IC2}$	-	$I_{IN}$ (Under Test)=100 $\mu A$ $V_{DD}$ =0V, $V_{SS}$ =Open All Other Pins Open	0.1	1.2	V
Input Clamp Voltage 3, to $V_{SS}$ , COM and CH Inputs	$V_{IC3}$	-	$I_{IN}$ (Under Test)= -100 $\mu A$ $V_{DD}$ =Open, $V_{SS}$ =0V All Other Pins Open	-0.05	-1.2	V
Input Clamp Voltage 4, to $V_{DD}$ , COM and CH Inputs	$V_{IC4}$	-	$I_{IN}$ (Under Test)=100 $\mu A$ $V_{DD}$ =0V, $V_{SS}$ =Open All Other Pins Open	0.05	1.2	V

## 2.3.3

## Notes to Electrical Measurement Tables

- Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be  $V_{IN} = V_{SS}$  or  $V_{DD}$  and outputs not under test shall be open.
- Functional tests shall be performed with  $f = 10$  kHz (min). The maximum time to output comparator strobe=30 $\mu s$ .
- Quiescent Current shall be tested using the following input conditions:
  - $\overline{INH} = \overline{A} = \overline{B} = \overline{C} = V_{IL}$ ; All CH and COM inputs =  $V_{IH}$
  - $\overline{INH} =$  All CH and COM inputs =  $V_{IL}$ ;  $\overline{A} = \overline{B} = \overline{C} = V_{IH}$
- Channel ON Resistance shall be tested for each channel, in both directions using the following input conditions:
  - $\overline{INH} = V_{IL}$
  - $\overline{A}, \overline{B}, \overline{C} = V_{IL}$  or  $V_{IH}$  per Truth Table to select channel under test.
  - $I_{IN}(CH \text{ or } COM) = 1$  mA
  - $R_{ON1}$  shall be tested with  $V_{IN}(CH \text{ or } COM) = 0.5V, 1V, 3.5V, 4V$   
 $R_{ON2}$  shall be tested with  $V_{IN}(CH \text{ or } COM) = 1V, 3V, 5V$

Channel ON Resistance Matching shall be calculated as follows: The results of the Channel ON Resistance measurements of each Channel's Input/Output to the Common Output/Input, and reverse, shall be compared and shall not exceed the specified Limits.

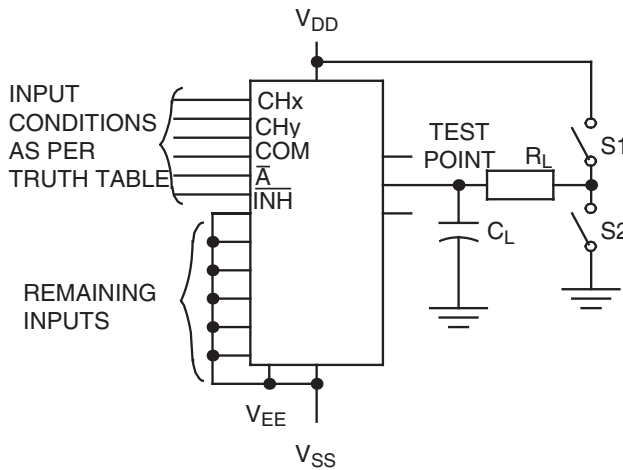
- Guaranteed but not tested.

6. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.

The pulse generator shall have the following characteristics:

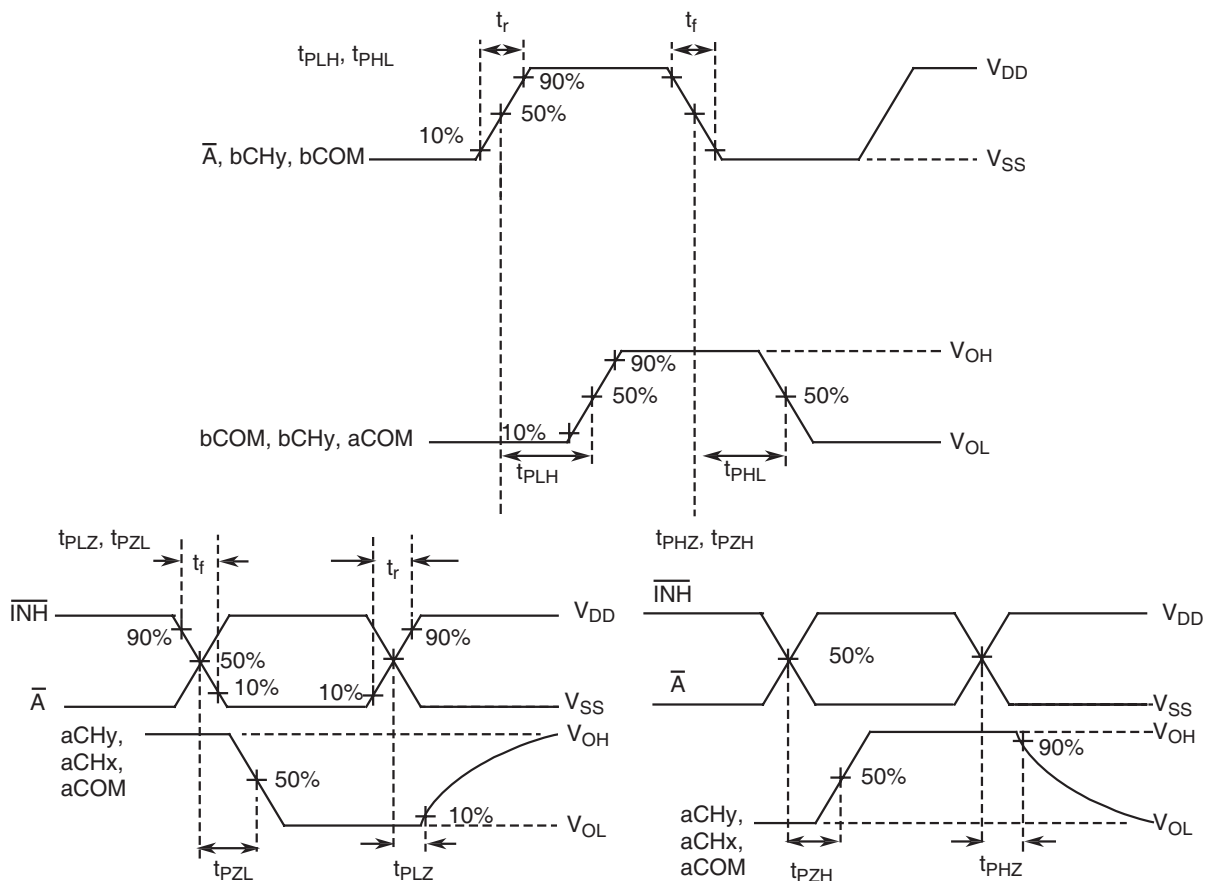
$V_{GEN} = 0$  to  $V_{DD}$ ;  $f_{GEN} = 1$  MHz minimum;  $t_r$  and  $t_f \leq 6$  ns (10% to 90%); duty cycle = 50%;  $Z_{out} = 50\Omega$ . Output load capacitance  $C_L = 50\text{pF} \pm 5\%$  including scope probe, wiring and stray capacitance without component in the test fixture and channel bias resistance  $R_L = 1\text{k}\Omega \pm 5\%$ .

Propagation delay times and output enable times shall be measured as follows:



PARAMETER	$R_L$	$C_L$	$S_1$	$S_2$
$t_{pZH}$	$1\text{k}\Omega$	$50\text{pF}$	OPEN	CLOSED
$t_{pZL}$			CLOSED	OPEN
$t_{pHZ}$	$1\text{k}\Omega$	$50\text{pF}$	OPEN	CLOSED
$t_{pLZ}$			CLOSED	OPEN
$t_{PHL}, t_{PLH}$	-	$50\text{pF}$	OPEN	OPEN

VOLTAGE WAVEFORMS



2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Quiescent Current	$I_{DD}$	$\pm 120$	-	400	nA
Low Level Input Current, Control inputs	$I_{IL}$	$\pm 20$	-	-50	nA
High Level Input Current, Control inputs	$I_{IH}$	$\pm 20$	-	50	nA
Channel ON Resistance 1, bCHy to bCOM bCOM to bCHy Note 2	$R_{ON1}$	$\pm 20$	-	180	$\Omega$
Channel ON Resistance 2, bCHy to bCOM bCOM to bCHy Note 2	$R_{ON2}$	$\pm 20$	-	160	$\Omega$
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.45	1.35	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Channel ON Resistance shall be tested at each input voltage level specified in Room Temperature Electrical Measurements in both directions for bCHy to bCOM only.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.



Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Functional Test 2	-	-	-	-	-
Functional Test 3	-	-	-	-	-
Quiescent Current	$I_{DD}$	$\pm 120$	-	400	nA
Low Level Input Current, Control inputs	$I_{IL}$	$\pm 20$	-	-50	nA
High Level Input Current, Control inputs	$I_{IH}$	$\pm 20$	-	50	nA
Channel OFF Leakage Current 1, Any Channel CH	$I_{OFF1}$	-	-	-100	nA
Channel OFF Leakage Current 3, All Channels Tested Together	$I_{OFF3}$	-	-	100	nA
Channel ON Resistance 1	$R_{ON1}$	$\pm 20$	-	180	$\Omega$
Channel ON Resistance 2	$R_{ON2}$	$\pm 20$	-	160	$\Omega$
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.45	1.35	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values ( $\Delta$ ) are applicable to the Operating Life test only.

**2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS**
**2.6.1 N-Channel HTRB**

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	$^{\circ}\text{C}$
Outputs aCOM, bCOM, cCOM	$V_{OUT}$	Open or $V_{SS}$	V
Inputs aCHx, aCHy, bCHx, bCHy, cCHx, cCHy	$V_{IN}$	$V_{SS}$	V
Inputs $\overline{INH}$ , $\overline{A}$ , $\overline{B}$ , $\overline{C}$	$V_{IN}$	$V_{DD}$	V
Positive Supply Voltage	$V_{DD}$	6 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V
Negative Supply Voltage	$V_{EE}$	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

 2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	°C
Outputs aCOM, bCOM, cCOM	$V_{OUT}$	Open or $V_{SS}$	V
Inputs aCHx, aCHy, bCHx, bCHy, cCHx, cCHy	$V_{IN}$	$V_{DD}$	V
Inputs $\overline{INH}$ , $\overline{A}$ , $\overline{B}$ , $\overline{C}$	$V_{IN}$	$V_{SS}$	V
Positive Supply Voltage	$V_{DD}$	6 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V
Negative Supply Voltage	$V_{EE}$	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 2kΩ min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

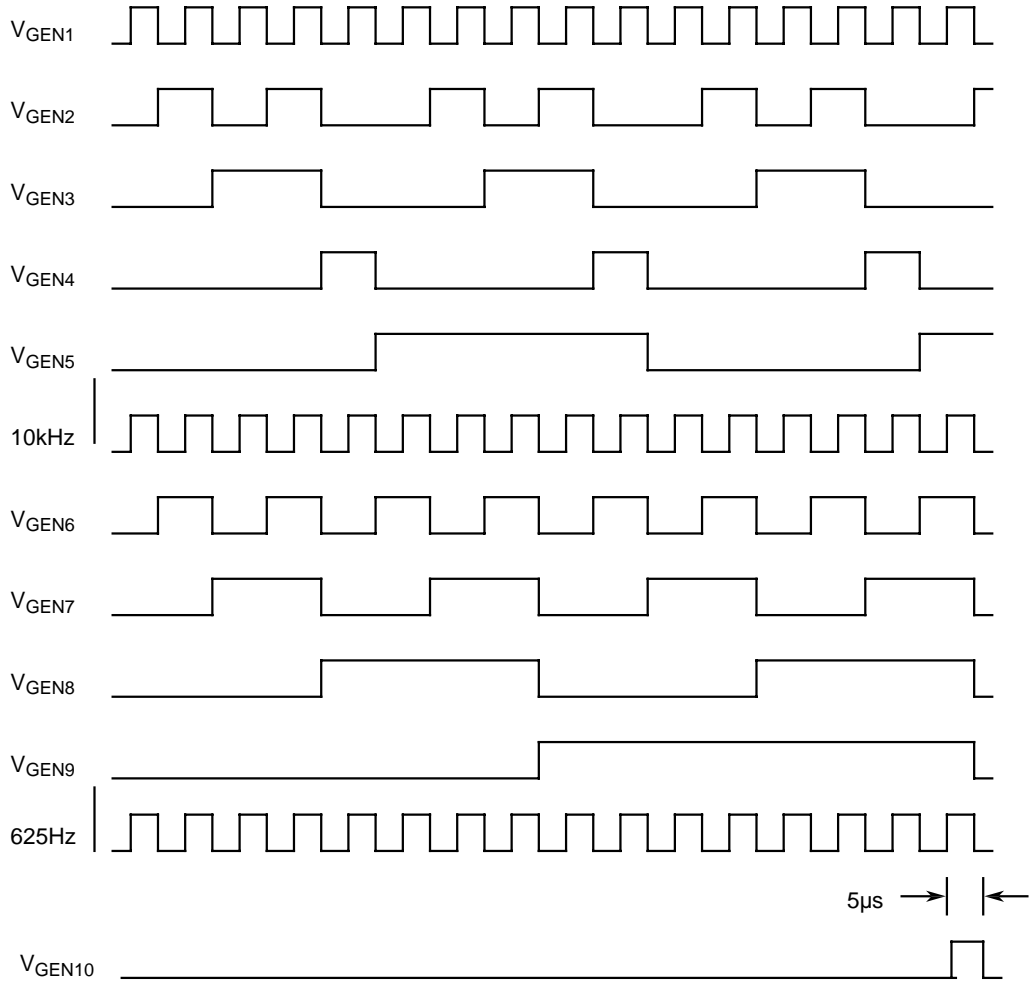
 2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	°C
Outputs aCOM, bCOM, cCOM	$V_{OUT}$	$V_{DD}$	V
Input $\overline{A}$	$V_{IN}$	$V_{GEN1}$	V
Input $\overline{B}$	$V_{IN}$	$V_{GEN2}$	V
Input $\overline{C}$	$V_{IN}$	$V_{GEN3}$	V
Input aCHx	$V_{IN}$	$V_{GEN4}$	V
Input bCHx	$V_{IN}$	$V_{GEN5}$	V
Input cCHx	$V_{IN}$	$V_{GEN6}$	V
Input aCHy	$V_{IN}$	$V_{GEN7}$	V
Input bCHy	$V_{IN}$	$V_{GEN8}$	V
Input cCHy	$V_{IN}$	$V_{GEN9}$	V
Input $\overline{INH}$	$V_{IN}$	$V_{GEN10}$	V
Pulse Voltage	$V_{GEN}$	0V to $V_{DD}$	V

Characteristics	Symbols	Test Conditions	Units
Pulse Frequency Square Wave	f <sub>GEN1</sub> f <sub>GEN2</sub> f <sub>GEN3</sub> f <sub>GEN4</sub> f <sub>GEN5</sub> f <sub>GEN6</sub> f <sub>GEN7</sub> f <sub>GEN8</sub> f <sub>GEN9</sub> f <sub>GEN10</sub>	100k ± 10% 20k ± 10% 20k ± 10% 20k ± 10% 10k ± 10% 5k ± 10% 2.5k ± 10% 1.25k ± 10% 625 ± 10% One 5µs positive pulse each 35ms t <sub>r</sub> = t <sub>f</sub> ≤ 400ns see Note 3	Hz
Positive Supply Voltage	V <sub>DD</sub>	6 (+0 -0.5)	V
Negative Supply Voltage	V <sub>SS</sub>	0	V
Negative Supply Voltage	V <sub>EE</sub>	0	V

**NOTES:**

1. Input Protection Resistor = 680Ω min to 100kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.
3. Input waveforms to indicate required timing and phase relationship:



2.8 OPERATING LIFE CONDITIONS  
 The conditions shall be as specified for Power Burn-in.

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing  
 Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	$+ 22 \pm 3$	$^{\circ}C$
Outputs aCOM, bCOM, cCOM	$V_{OUT}$	Open	V
Inputs aCHx, bCHx, cCHx, $\bar{A}$ , $\bar{B}$ , $\bar{C}$	$V_{IN}$	$V_{DD}$	V
Inputs aCHy, bCHy, cCHy, $\overline{INH}$	$V_{IN}$	$V_{SS}$	V
Positive Supply Voltage	$V_{DD}$	$6 \pm 0.3$	V
Negative Supply Voltage	$V_{SS}$	0	V
Negative Supply Voltage	$V_{EE}$	0	V

**NOTES:**

1. Input Protection Resistor = 680 $\Omega$  min to 47k $\Omega$  max.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits			Units
		Drift Values $\Delta$	Absolute		
			Min	Max	
Quiescent Current	$I_{DD}$	-	-	40	$\mu A$
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.6$	-0.4	-1.5	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.6$	0.4	1.4	V

**APPENDIX 'A'**

**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
<p>Deviations from Screening Tests - Chart F3</p>	<p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> <p>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.</p> <p>Solderability is not applicable unless specifically stipulated in the Purchase Order.</p>
<p>Deviations from Qualification and Periodic Tests - Chart F4</p>	<p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p>
<p>Deviations from High and Low Temperatures Electrical Measurements</p>	<p>The Channel ON Resistance Matching (1 and 2) calculations are not performed.</p> <p>High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
<p>Deviations from Room Temperature Electrical Measurements</p>	<p>The Channel ON Resistance Matching (1 and 2) calculations are not performed.</p> <p>All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>