



Pages 1 to 27

INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS

DUAL 4-BIT LATCH WITH

3-STATE OUTPUTS

BASED ON TYPE 4508B

ESCC Detail Specification No. 9202/063

| | |
|---------|-------------|
| Issue 2 | August 2004 |
|---------|-------------|



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| DCR No. | CHANGE DESCRIPTION |
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| 90 | Specification up issued to incorporate editorial and technical changes per DCR. |

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920206301

- Detail Specification Reference: 9202063
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and /or Finish | Weight max g |
|----------------|---------------|------|----------------------------------|--------------|
| 01 | 4508B | FP | G2 | 1.7 |
| 02 | 4508B | FP | G4 | 1.7 |
| 03 | 4508B | DIP | G2 | 5.2 |
| 04 | 4508B | DIP | G4 | 5.2 |
| 07 | 4508B | CCP | 2 | 0.9 |
| 08 | 4508B | SO | G2 | 1.1 |
| 09 | 4508B | SO | G4 | 1.1 |

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

| Characteristics | Symbols | Maximum Ratings | Units | Remarks |
|--|-----------|------------------------|-------------|--------------------|
| Supply Voltage | V_{DD} | -0.5 to 18 | V | Note 1 |
| Input Voltage | V_{IN} | -0.5 to $V_{DD} + 0.5$ | V | Note 1 Power on |
| Input Current | I_{IN} | ± 10 | mA | - |
| Device Power Dissipation (Continuous) | P_D | 200 | mW | - |
| Power Dissipation per Output | P_{DSO} | 100 | mW | - |
| Operating Temperature Range | T_{op} | -55 to +125 | $^{\circ}C$ | T_{amb} |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}C$ | - |
| Soldering Temperature For FP, DIP and SO For CCP | T_{sol} | +265 +245 | $^{\circ}C$ | Note 2 Note 3 |

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

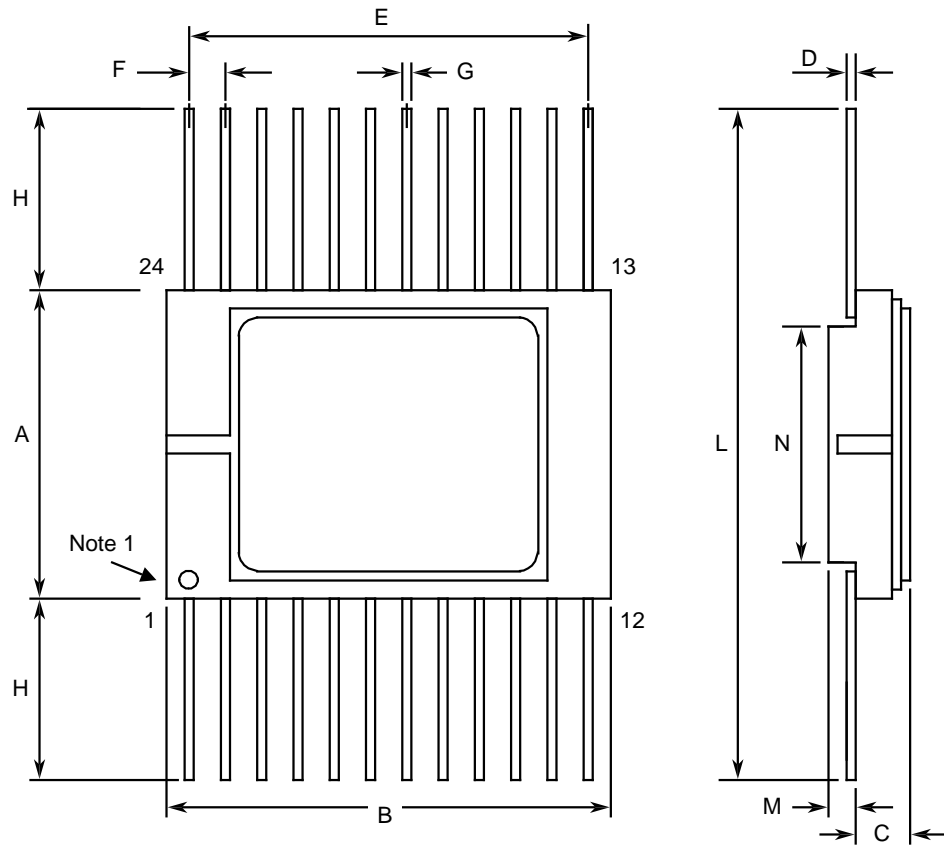
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

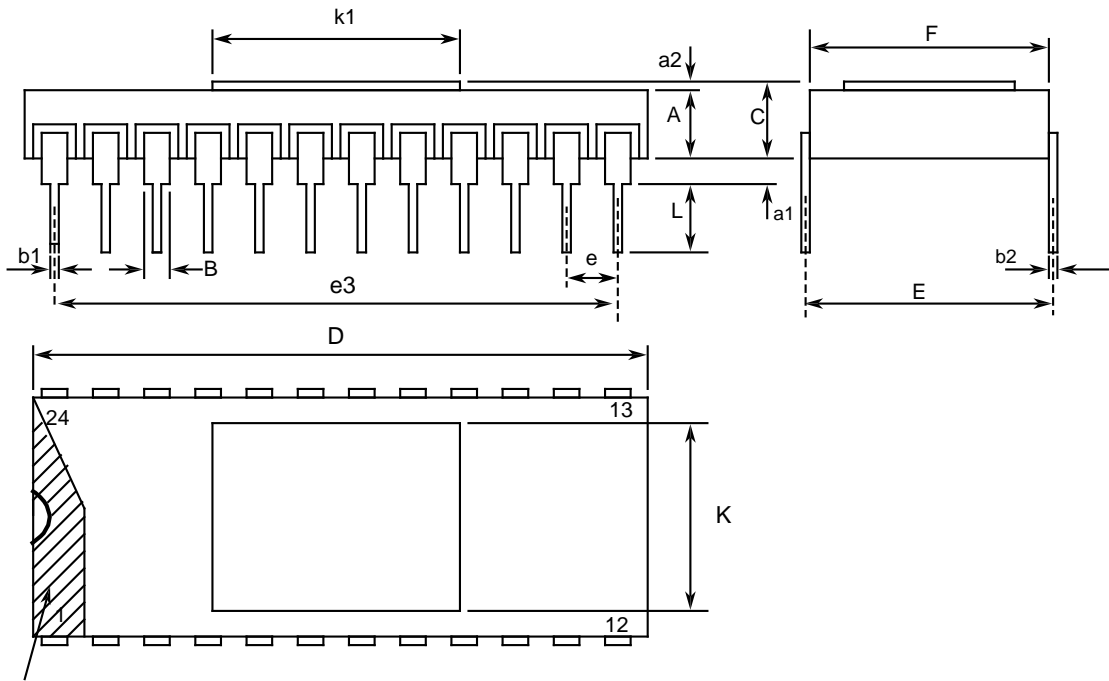
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 24Pin



| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| A | 10.7 | 11.3 | |
| B | 15.3 | 15.7 | |
| C | 1.45 | 1.9 | |
| D | 0.23 | 0.3 | 5 |
| E | 13.84 | 14.1 | |
| F | 1.22 | 1.32 | 3, 6 |
| G | 0.45 | 0.55 | 5 |
| H | 7.25 | 8.25 | 5 |
| L | 25 | 28 | |
| M | 0.45 | 0.55 | |
| N | 7 TYPICAL | | |

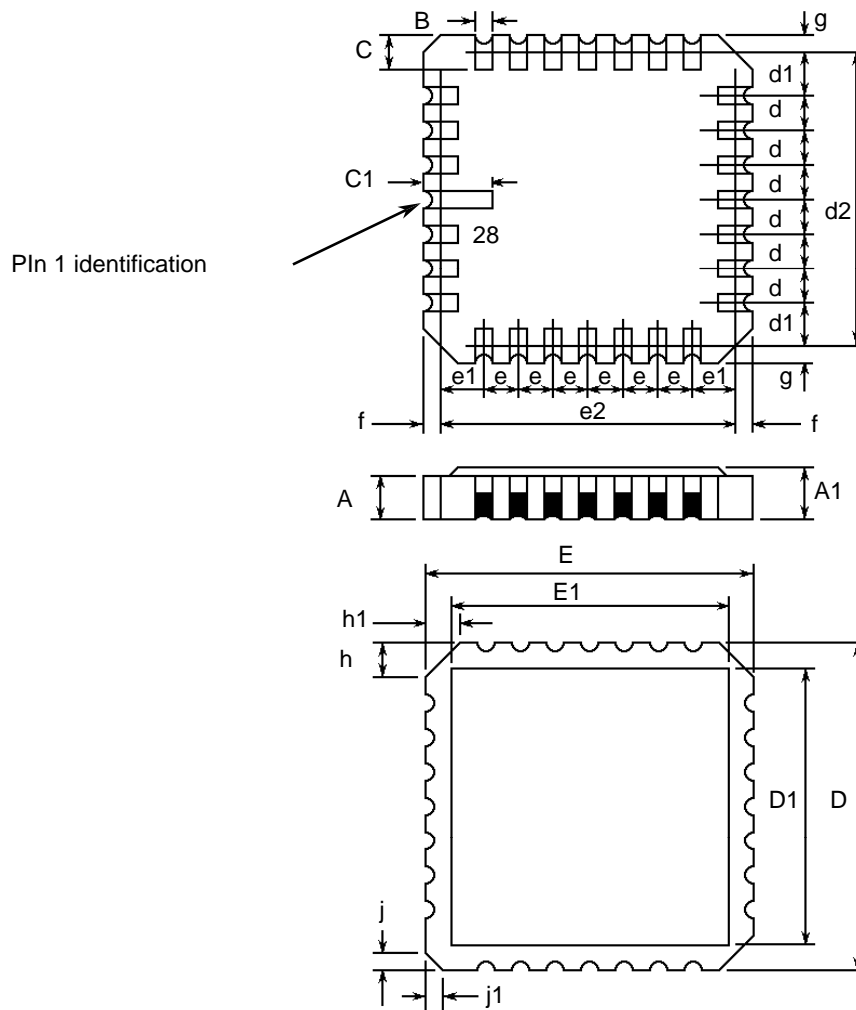
1.7.2 Dual-in-line Package (DIP) - 24Pin



NOTE 1

| Symbols | Dimensions mm | | Notes |
|---------|---------------|--------|-------|
| | Min | Max | |
| A | 1.931 | 2.387 | |
| a1 | 1.016 | 1.524 | 2 |
| a2 | 0.274 | 0.34 | |
| B | 1.274 TYPICAL | | 5 |
| b1 | 0.407 | 0.507 | 5 |
| b2 | 0.229 | 0.304 | 5 |
| C | 2.205 | 2.727 | |
| D | 30.176 | 30.784 | |
| E | 14.986 | 15.494 | |
| e | 2.413 | 2.667 | 4, 6 |
| e3 | 27.813 | 28.067 | |
| F | 14.859 | 15.367 | |
| L | 3 | 3.8 | |
| K | 12.6 | 13 | |
| k1 | 12.6 | 13 | |

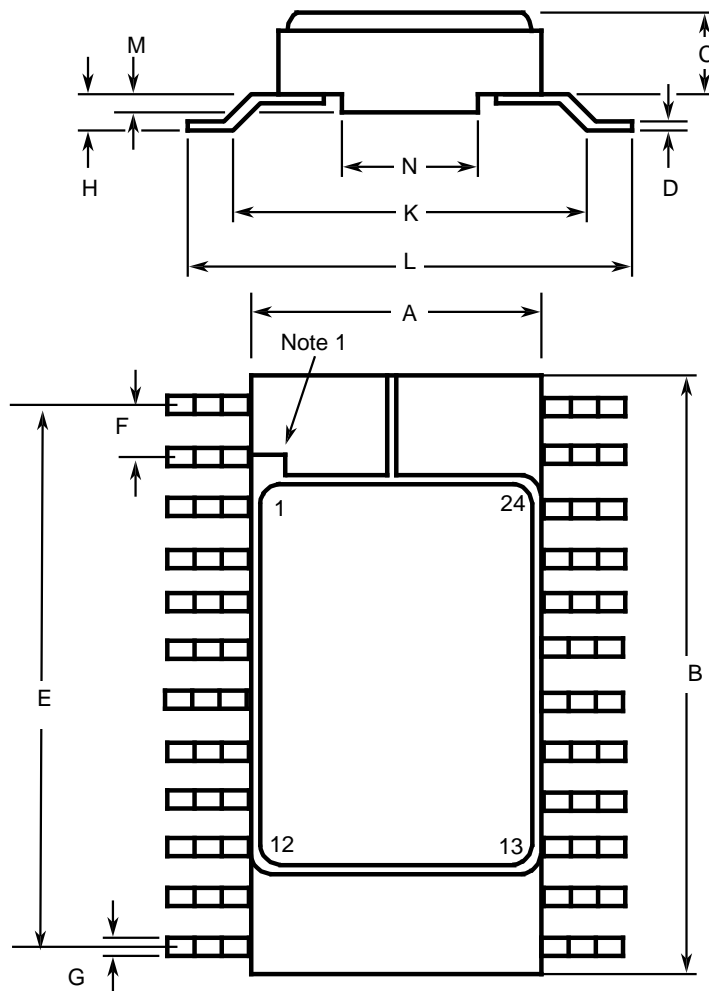
1.7.3 Chip Carrier Package (CCP) - 28 Terminal



| Symbols | Dimensions mm | | Notes |
|---------|---------------|-------|-------|
| | Min | Max | |
| A | 1.14 | 1.95 | |
| A1 | 1.63 | 2.36 | |
| B | 0.55 | 0.72 | 5 |
| C | 1.06 | 1.47 | 5 |
| C1 | 1.91 | 2.41 | |
| D | 11.23 | 11.63 | |
| D1 | 9.4 | 9.78 | |
| d, d1 | 1.27 TYPICAL | | 3, 6 |
| d2 | 10.16 TYPICAL | | |
| E | 11.23 | 11.63 | |
| E1 | 9.4 | 9.78 | |

| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| e, e1 | 1.27 TYPICAL | | 3, 6 |
| e2 | 10.16 TYPICAL | | |
| f, g | - | 0.76 | |
| h, h1 | 1.01 TYPICAL | | 8 |
| j, j1 | 0.51 TYPICAL | | 7 |

1.7.4 Small Outline Ceramic Package (SO) - 24 Pin



| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| A | 7.3 | 7.6 | |
| B | 15.2 | 15.6 | |
| C | 1.58 | 1.88 | |

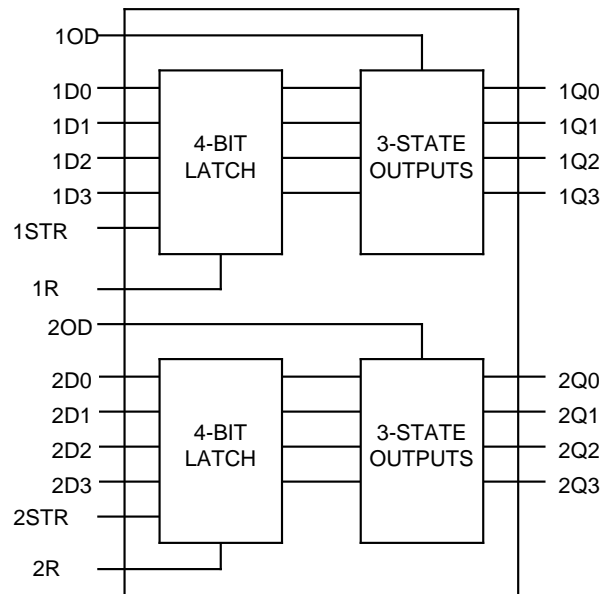
| Symbols | Dimensions mm | | Notes |
|---------|---------------|-------|-------|
| | Min | Max | |
| D | 0.17 | 0.23 | 5 |
| E | 13.82 | 14.12 | |
| F | 1.27 TYPICAL | | 3, 6 |
| G | 0.37 | 0.47 | 5 |
| H | 0.6 | 0.9 | 5 |
| K | 9 TYPICAL | | |
| L | 10 | 10.65 | |
| M | 0.55 TYPICAL | | |
| N | 4.7 TYPICAL | | |

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13 mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25 mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 22 spaces for flat, dual-in-line and small outline packages.
24 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only



1.9 PIN ASSIGNMENT

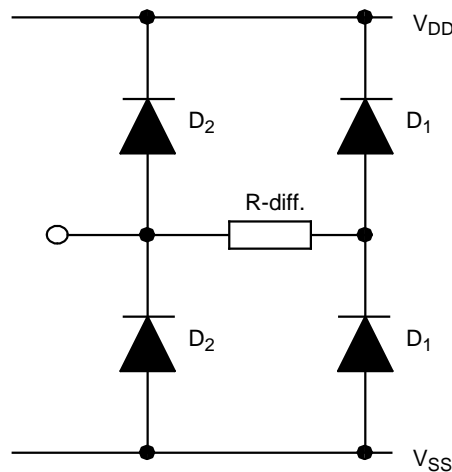
| Pin | Function | | Pin | Function | |
|-----|----------------------------|----------------------------|-----|----------------------------|----------------------------|
| | FP, DIP and SO | CCP | | FP, DIP and SO | CCP |
| 1 | 1R Input (Reset) | 1R Input (Reset) | 15 | 2OD Input (Output Disable) | 2R Input (Reset) |
| 2 | 1STR Input (Strobe) | 1STR Input (Strobe) | 16 | 2D0 Input | 2STR Input (Strobe) |
| 3 | 1OD Input (Output Disable) | 1OD Input (Output Disable) | 17 | 2Q0 Output | 2OD Input (Output Disable) |
| 4 | 1D0 Input | - | 18 | 2D1 Input | - |
| 5 | 1Q0 Output | 1D0 Input | 19 | 2Q1 Output | 2D0 Input |
| 6 | 1D1 Input | 1Q0 Output | 20 | 2D2 Input | 2Q0 Output |
| 7 | 1Q1 Output | 1D1 Input | 21 | 2Q2 Output | 2D1 Input |
| 8 | 1D2 Input | 1Q1 Output | 22 | 2D3 Input | 2Q1 Output |
| 9 | 1Q2 Output | 1D2 Input | 23 | 2Q3 Output | 2D2 Input |
| 10 | 1D3 Input | 1Q2 Output | 24 | V _{DD} | 2Q2 Output |
| 11 | 1Q3 Output | - | 25 | - | - |
| 12 | V _{SS} | 1D3 Input | 26 | - | 2D3 Input |
| 13 | 2R Input (Reset) | 1Q3 Output | 27 | - | 2Q3 Output |
| 14 | 2STR Input (Strobe) | V _{SS} | 28 | - | V _{DD} |

1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance.
EACH LATCH

| INPUTS | | | | OUTPUTS |
|--------|----|-----|----|---------|
| R | OD | STR | Dn | Qn |
| L | L | H | H | H |
| L | L | H | L | L |
| L | L | L | X | latched |
| H | L | X | X | L |
| X | H | X | X | Z |

1.11 INPUT PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb}=+22 \pm 3^{\circ}C$.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|-----------|-------------------------|---|--------|-----|---------|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=3V$ $V_{DD}=3V, V_{SS}=0V$ Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 2 | - | - | - |
| Quiescent Current | I_{DD} | 3005 | $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 3 | - | 1 | μA |
| Low Level Input Current | I_{IL} | 3009 | V_{IN} (Under Test)=0V $V_{DD}=15V, V_{SS}=0V$ | - | -50 | nA |
| High Level Input Current | I_{IH} | 3010 | V_{IN} (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$ | - | 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | 3007 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | 3007 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$ | - | 500 | mV |
| Low Level Output Voltage 3 (Noise Immunity) | V_{OL3} | 3007 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 1.5 | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|--|-----------|----------------------------|--|--------|------|---------|
| | | | | Min | Max | |
| High Level Output Voltage 1 | V_{OH1} | 3006 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | 3006 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$ | 4.5 | - | V |
| High Level Output Voltage 3 (Noise Immunity) | V_{OH3} | 3006 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 13.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 | 510 | - | μA |
| Low Level Output Current 2 | I_{OL2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 | 3.4 | - | mA |
| High Level Output Current 1 | I_{OH1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 | -510 | - | μA |
| High Level Output Current 2 | I_{OH2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 | -3.4 | - | mA |
| Threshold Voltage N-Channel | V_{THN} | - | 1STR Input at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$ | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | - | 1STR Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$ | 0.7 | 3 | V |
| Output Leakage Current Third State, Low Level Applied | I_{OZL} | 3020 | $V_{IL}=0V$ $V_{IH}=15V$ $V_{OL}=0V$ $V_{DD}=15V, V_{SS}=0V$ | - | -400 | nA |
| Output Leakage Current Third State, High Level Applied | I_{OZH} | 3021 | $V_{IL}=0V$ $V_{IH}=15V$ $V_{OH}=15V$ $V_{DD}=15V, V_{SS}=0V$ | - | 400 | nA |
| Input Clamp Voltage 1, to V_{SS} | V_{IC1} | - | I_{IN} (Under Test)= -100 μA $V_{DD}=\text{Open}, V_{SS}=0V$ All Other Pins Open | - | -2 | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|------------|----------------------------|--|--------|-----|-------|
| | | | | Min | Max | |
| Input Clamp Voltage 2, to V_{DD} | V_{IC2} | - | V_{IN} (Under Test)=6V $R=30k\Omega$, V_{SS} =Open All Other Pins Open Note 5 | 3 | - | V |
| Input Capacitance 1, 1OD, 2OD, 1STR, 2STR, 1Dn, 2Dn | C_{IN1} | 3012 | V_{IN} (Not Under Test)=0V $V_{DD}=V_{SS}=0V$ $f = 100$ kHz to 1 MHz Note 6 | - | 7.5 | pF |
| Input Capacitance 2, 1R, 2R | C_{IN2} | 3012 | V_{IN} (Not Under Test)=0V $V_{DD}=V_{SS}=0V$ $f = 100$ kHz to 1 MHz Note 6 | - | 18 | pF |
| Propagation Delay Low to High 1, 1STR to 1Q2 | t_{PLH1} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V$, $V_{IH}=5V$, $V_{DD}=5V$, $V_{SS}=0V$ Note 7 | - | 260 | ns |
| Propagation Delay High to Low 1, 1STR to 1Q2 | t_{PHL1} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V$, $V_{IH}=5V$, $V_{DD}=5V$, $V_{SS}=0V$ Note 7 | - | 260 | ns |
| Propagation Delay Low to High 2, 1D2 To 1Q2 | t_{PLH2} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V$, $V_{IH}=5V$, $V_{DD}=5V$, $V_{SS}=0V$ Note 7 | - | 210 | ns |
| Propagation Delay High to Low 2, 1D2 To 1Q2 | t_{PHL2} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V$, $V_{IH}=5V$, $V_{DD}=5V$, $V_{SS}=0V$ Note 7 | - | 210 | ns |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|------------|----------------------------|---|--------|-----|-------|
| | | | | Min | Max | |
| Propagation Delay Low to High 3, 1R to 1Q2 | t_{PLH3} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Propagation Delay High to Low 3, 1R to 1Q2 | t_{PHL3} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Output Enable Time High Impedance to Low Output, 1OD to 1Q3 | t_{PZL} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Output Disable Time Low Output to High Impedance, 1OD to 1Q3 | t_{PLZ} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Output Enable Time High Impedance to High Output, 1OD to 1Q3 | t_{PZH} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Output Disable Time High Output to High Impedance, 1OD to 1Q3 | t_{PHZ} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 180 | ns |
| Transition Time Low to High, 1Q2 | t_{TLH} | 3004 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 200 | ns |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|----------------------------------|-----------|-------------------------|---|--------|-----|-------|
| | | | | Min | Max | |
| Transition Time High to Low, 1Q2 | t_{THL} | 3004 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 200 | ns |

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{amb}=+125 (+0 -5) ^\circ C$ and $T_{amb}=- 55(+5-0)^\circ C$.

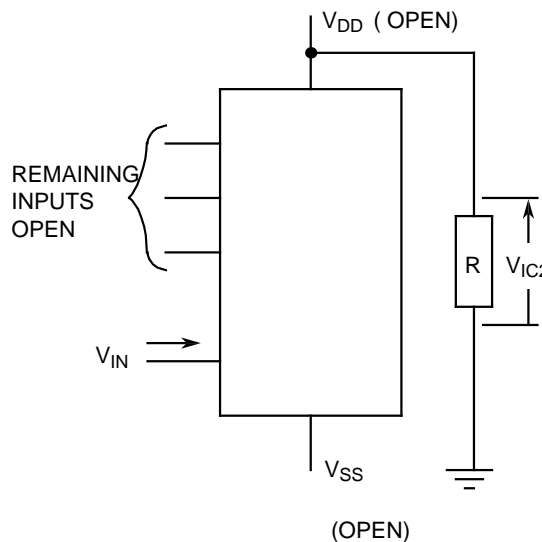
| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|-----------|-------------------------|--|--------|-------------|---------|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=3V$ $V_{DD}=3V, V_{SS}=0V$ Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 2 | - | - | - |
| Quiescent Current | I_{DD} | 3005 | $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 3 $T_{amb}=+125^\circ C$ $T_{amb}=- 55^\circ C$ | - | 30 1 | μA |
| Low Level Input Current | I_{IL} | 3009 | V_{IN} (Under Test)=0V $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^\circ C$ $T_{amb}=- 55^\circ C$ | - | -100 -50 | nA |
| High Level Input Current | I_{IH} | 3010 | V_{IN} (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^\circ C$ $T_{amb}=- 55^\circ C$ | - | 100 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | 3007 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | 3007 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$ | - | 500 | mV |
| Low Level Output Voltage 3 (Noise Immunity) | V_{OL3} | 3007 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 1.5 | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|--|-----------|----------------------------|--|--------------|--------------|---------|
| | | | | Min | Max | |
| High Level Output Voltage 1 | V_{OH1} | 3006 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | 3006 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$ | 4.5 | - | V |
| High Level Output Voltage 3 (Noise Immunity) | V_{OH3} | 3006 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 13.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 360 640 | - - | μA |
| Low Level Output Current 2 | I_{OL2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 2.4 4.2 | - - | mA |
| High Level Output Current 1 | I_{OH1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -360 -640 | - - | μA |
| High Level Output Current 2 | I_{OH2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -2.4 -4.2 | - - | mA |
| Threshold Voltage N-Channel | V_{THN} | - | 1STR Input at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -0.3 -0.7 | -3.5 -3.5 | V |
| Threshold Voltage P-Channel | V_{THP} | - | 1STR Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 0.3 0.7 | 3.5 3.5 | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|--|-----------|-------------------------|---|--------|-----|---------|
| | | | | Min | Max | |
| Output Leakage Current Third State, Low Level Applied | I_{OZL} | 3020 | $V_{IL}=0V$ $V_{IH}=15V$ $V_{OL}=0V$ $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | - | -12 | μA |
| Output Leakage Current Third State, High Level Applied | I_{OZH} | 3021 | $V_{IL}=0V$ $V_{IH}=15V$ $V_{OH}=15V$ $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | - | 12 | μA |

2.3.3 Notes to Electrical Measurement Tables

- Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
- Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD} - 0.5V$, $V_{OL} \leq 0.5V$. The Maximum time to output comparator strobe = 300 μs .
- Quiescent Current shall be tested using the following input conditions:
 - Inputs 1STR = 2STR = V_{IH} ; all other inputs = V_{IL} .
 - Inputs 1R = 2R = 1OD = 2OD = V_{IL} ; all other inputs = V_{IH} .
 - Inputs 1R = 2R = V_{IL} ; all other inputs = V_{IH} .
 - All inputs = V_{IH} .
 - Inputs 1STR = 2STR = 1OD = 2OD = V_{IL} ; all other inputs = V_{IH} .
- Interchange of forcing and measuring parameters is permitted.
- Input Clamp Voltage 2 to V_{DD} , V_{IC2} , shall be tested on each input as follows:-

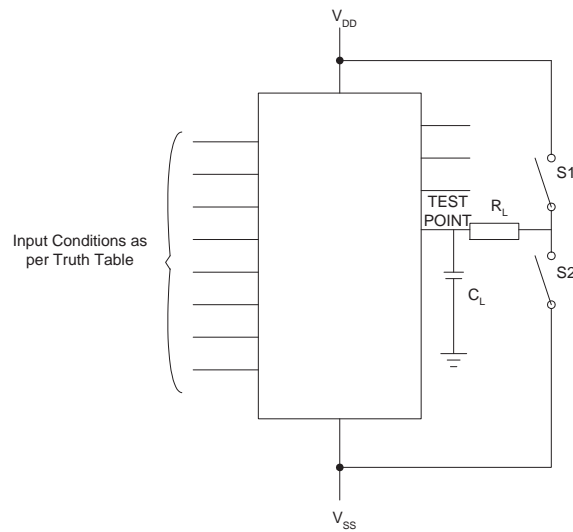


- Guaranteed but not tested.
- Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.

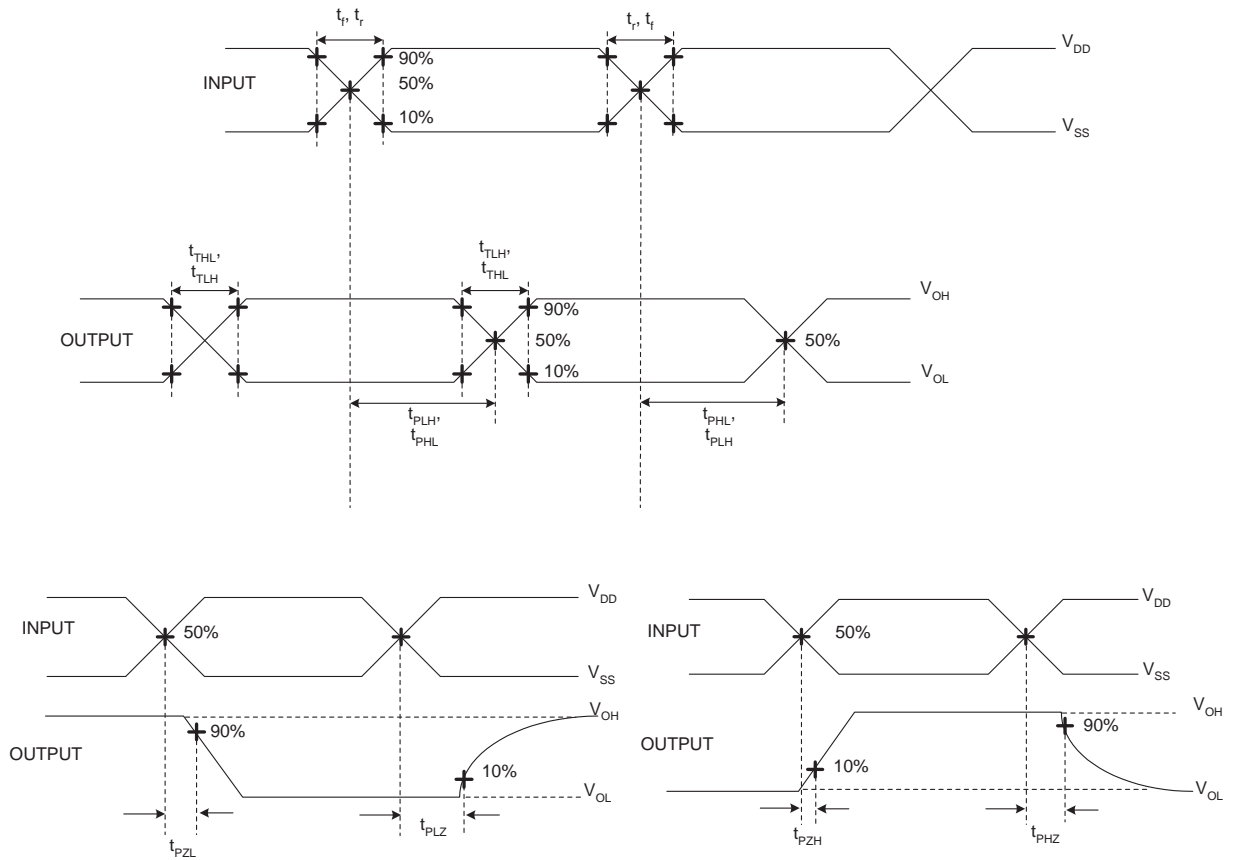
The pulse generator shall have the following characteristics:

$V_{GEN} = 0$ to V_{DD} ; $f = 500\text{kHz}$; t_r and $t_f \leq 15$ ns (10% to 90%); duty cycle = 50%. Output load capacitance $C_L = 50\text{pF} \pm 5\%$ including scope probe, wiring and stray capacitance without component in the test fixture.

Propagation delay and transition time shall be measured as follows:



| Parameter | RL | S1 | S2 |
|--------------------------------------|---------------|--------|--------|
| t_{PZH} | 1k Ω | Open | Closed |
| t_{PZL} | | Closed | Open |
| t_{PHZ} | | Open | Closed |
| t_{PLZ} | | Closed | Open |
| $t_{PHL}, t_{PLH}, t_{THL}, t_{TLH}$ | 200k Ω | Open | Closed |



2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb}=+22 \pm 3^{\circ}\text{C}$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|--|-----------|-------------------------|----------|------|---------|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Quiescent Current | I_{DD} | ± 0.15 | - | 1 | μA |
| Low Level Output Current 1 | I_{OL1} | $\pm 15\% (2)$ | 510 | - | μA |
| High Level Output Current 1 | I_{OH1} | $\pm 15\% (2)$ | -510 | - | μA |
| Output Leakage Current Third State, Low Level Applied | I_{OZL} | ± 60 | - | -400 | nA |
| Output Leakage Current Third State, High Level Applied | I_{OZH} | ± 60 | - | 400 | nA |
| Threshold Voltage N-Channel | V_{THN} | ± 0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | ± 0.3 | 0.7 | 3 | V |

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5

INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements .

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|-----------|-------------------------|----------|------|---------|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Functional Test 1 | - | - | - | - | - |
| Quiescent Current | I_{DD} | ± 0.15 | - | 1 | μA |
| Low Level Input Current | I_{IL} | - | - | -50 | nA |
| High Level Input Current | I_{IH} | - | - | 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | - | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | - | - | 500 | mV |
| High Level Output Voltage 1 | V_{OH1} | - | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | - | 4.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | $\pm 15\%$ (3) | 510 | - | μA |
| Low Level Output Current 2 | I_{OL2} | $\pm 15\%$ (3) | 3.4 | - | mA |
| High Level Output Current 1 | I_{OH1} | $\pm 15\%$ (3) | -510 | - | μA |
| High Level Output Current 2 | I_{OH2} | $\pm 15\%$ (3) | -3.4 | - | mA |
| Output Leakage Current Third State, Low Level Applied | I_{OZL} | ± 60 | - | -400 | nA |
| Output Leakage Current Third State, High Level Applied | I_{OZH} | ± 60 | - | 400 | nA |
| Threshold Voltage N-Channel | V_{THN} | ± 0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | ± 0.3 | 0.7 | 3 | V |

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|------------------------------|-----------|-----------------|-------|
| Ambient Temperature | T_{amb} | +125 (+0 -5) | °C |
| Outputs 1Qn, 2Qn | V_{OUT} | Open | V |
| Inputs 1R, 2R, 1OD, 2OD, 1Dn | V_{IN} | V_{SS} | V |
| Inputs 1STR, 2STR, 2Dn | V_{IN} | V_{DD} | V |
| Positive Supply Voltage | V_{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V_{SS} | 0 | V |
| Duration | t | 72 | Hours |

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|------------------------------|-----------|-----------------|-------|
| Ambient Temperature | T_{amb} | +125 (+0 -5) | °C |
| Outputs 1Qn, 2Qn | V_{OUT} | Open | V |
| Inputs 1R, 2R, 1OD, 2OD, 1Dn | V_{IN} | V_{DD} | V |
| Inputs 1STR, 2STR, 2Dn | V_{IN} | V_{SS} | V |
| Positive Supply Voltage | V_{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V_{SS} | 0 | V |
| Duration | t | 72 | Hours |

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

| Characteristics | Symbols | Test Conditions | Units |
|-----------------------------|--------------------------|------------------------------|-------|
| Ambient Temperature | T_{amb} | +125 (+0 -5) | °C |
| Outputs 1Qn, 2Qn | V_{OUT} | $V_{DD}/2$ | V |
| Inputs 1R, 2R | V_{IN} | V_{SS} | V |
| Inputs 1STR, 2STR | V_{IN} | V_{DD} | V |
| Inputs 1Dn, 2Dn | V_{IN} | V_{GEN1} | V |
| Inputs 1OD, 2OD | V_{IN} | V_{GEN2} | V |
| Pulse Voltage | V_{GEN} | 0V to V_{DD} | V |
| Pulse Frequency Square Wave | f_{GEN1} f_{GEN2} | 50k 25k 50% Duty Cycle | Hz |
| Positive Supply Voltage | V_{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V_{SS} | 0 | V |

NOTES:

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|--|---|
| <p>Deviations from Screening Tests - Chart F3</p> | <p>External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> <p>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.</p> |
| <p>Deviations from Qualification and Periodic Tests - Chart F4</p> | <p>External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> |
| <p>Deviations from High and Low Temperatures Electrical Measurements</p> | <p>High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p> |
| <p>Deviations from Room Temperature Electrical Measurements</p> | <p>All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p> |