INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS 32/40-BIT IEEE FLOATING POINT DIGITAL SIGNAL PROCESSOR, WITH THREE STATE OUTPUTS

BASED ON TYPE TSC21020F

ESCC Detail Specification No. 9512/002

Issue 3	June 2008

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DCR No.	CHANGE DESCRIPTION
415	Specification up issued to incorporate editorial and technical changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

951200201R

- Detail Specification Reference: 9512002
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	TSC21020F-20	MQFP-F256	G2	15	R [100kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification no. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.5	V	Notes 1, 2
Output Current	I_{OUT}	±50	mA	Note 3
Device Power Dissipation (Continuous)	P_D	3.4	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+265	^oC	Note 4
Junction Temperature	T_j	+165	^oC	
Thermal Resistance Junction to Case	$R_{th(j-c)}$	3	$^oC/W$	

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional for $4.5V \leq V_{DD} \leq 5.5V$.
2. V_{DD}+0.5V shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

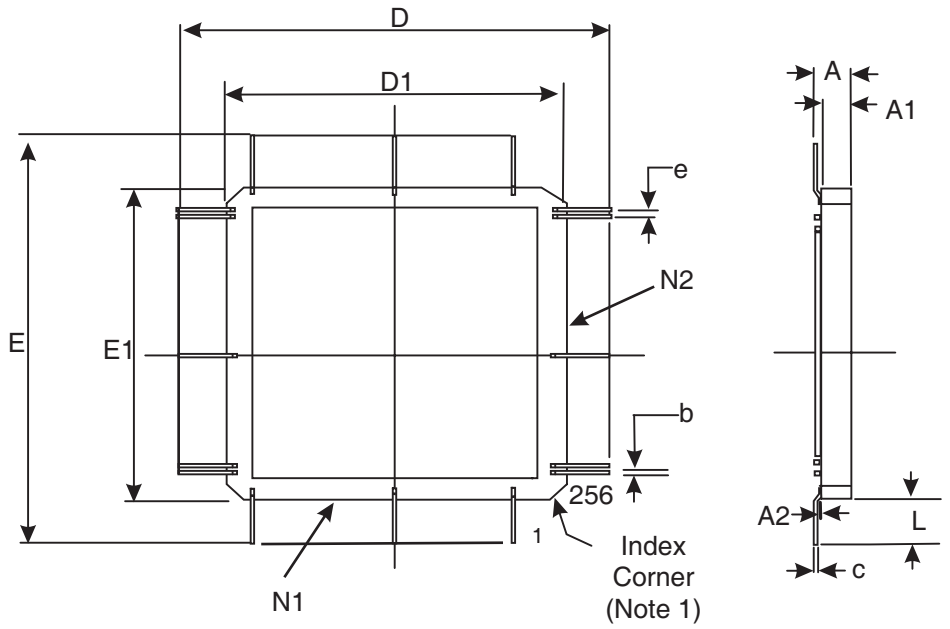
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Multilayer Quad Flat Package (MQFP-F256) - 256 Leads

BOTTOM VIEW

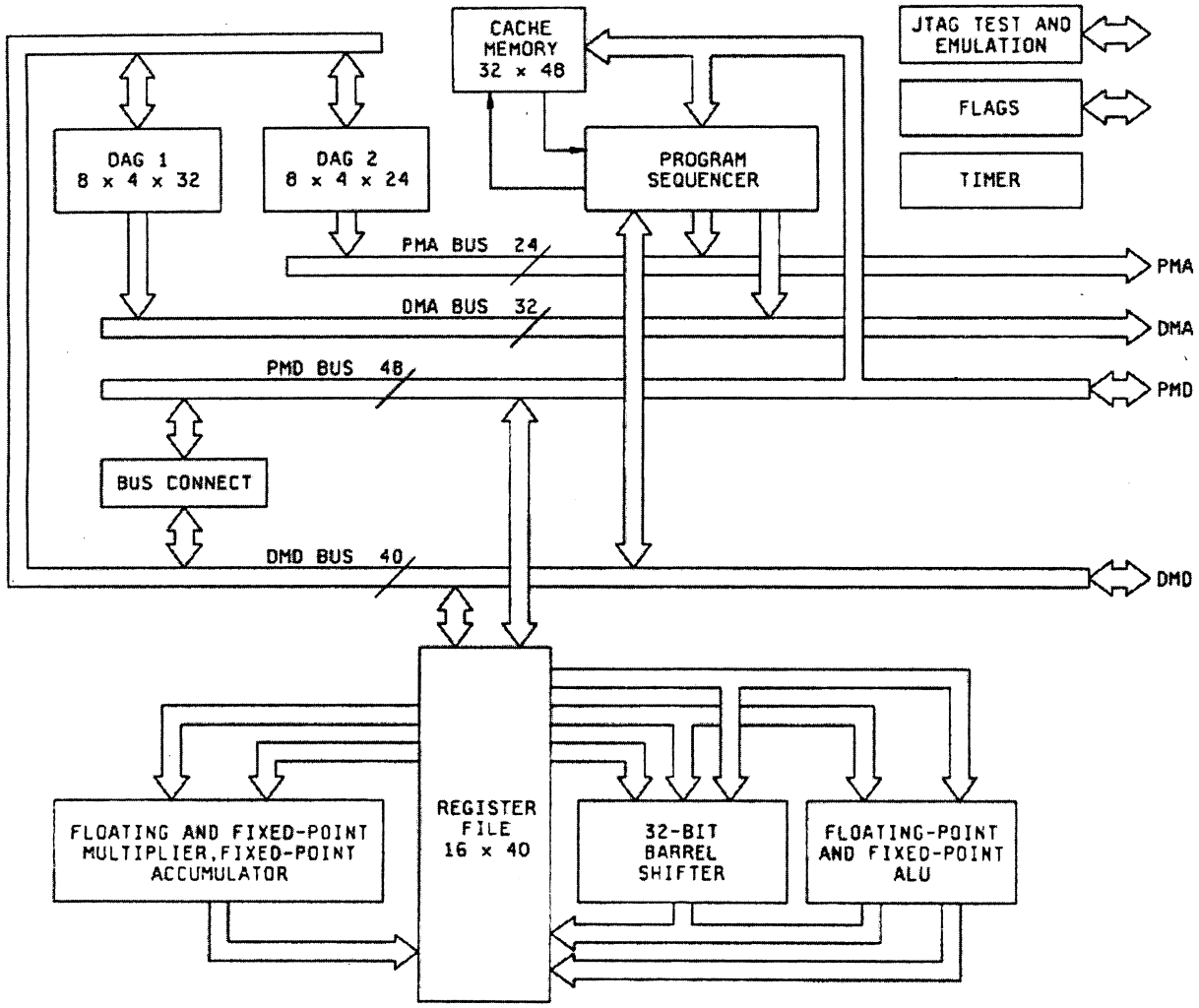


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.41	3.18	2
A1	2.06	2.56	
A2	0.05	0.36	2
b	0.15	0.25	2
c	0.1	0.2	2
D, E	53.23	55.74	
D1, E1	36.83	37.34	
e	0.508 BSC		3
L	8.2	9.2	2
N1, N2	64 Leads (per side)		

NOTES:

1. Index mark: a notch or lead 1 identification mark shall be located adjacent to lead 1.
2. All leads.
3. 252 places. The true position pin spacing is 0.508mm between centrelines. Each lead centreline shall be located within ±0.05mm of its true longitudinal position relative to the package centrelines.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Pin Name
1	IV_{SS}
2	IV_{DD}
3	DMD_{19}
4	DMD_{18}
5	DMD_{17}
6	DMD_{16}
7	EV_{SS}
8	DMD_{15}
9	DMD_{14}
10	DMD_{13}
11	DMD_{12}
12	EV_{DD}
13	DMD_{11}
14	DMD_{10}
15	DMD_{9}
16	DMD_{8}
17	IV_{SS}
18	IV_{DD}
19	EV_{SS}
20	DMD_{7}
21	DMD_{6}
22	DMD_{5}
23	DMD_{4}
24	EV_{DD}
25	DMD_{3}
26	DMD_{2}
27	DMD_{1}
28	DMD_{0}
29	EV_{SS}
30	PMD_{0}
31	PMD_{1}
32	PMD_{2}
33	IV_{SS}
34	IV_{DD}

Pin	Pin Name
35	PMD_3
36	EV_{DD}
37	PMD_4
38	PMD_5
39	PMD_6
40	PMD_7
41	EV_{SS}
42	PMD_8
43	PMD_9
44	PMD_{10}
45	PMD_{11}
46	EV_{DD}
47	PMD_{12}
48	PMD_{13}
49	IV_{SS}
50	IV_{DD}
51	PMD_{14}
52	PMD_{15}
53	EV_{SS}
54	PMD_{16}
55	PMD_{17}
56	PMD_{18}
57	PMD_{19}
58	EV_{DD}
59	PMD_{20}
60	PMD_{21}
61	PMD_{22}
62	PMD_{23}
63	EV_{SS}
64	PMD_{24}
65	IV_{SS}
66	IV_{DD}
67	PMD_{25}
68	PMD_{26}
69	PMD_{27}
70	EV_{DD}

Pin	Pin Name
71	PMD_{28}
72	PMD_{29}
73	PMD_{30}
74	PMD_{31}
75	EV_{SS}
76	PMD_{32}
77	PMD_{33}
78	PMD_{34}
79	PMD_{35}
80	EV_{DD}
81	IV_{SS}
82	IV_{DD}
83	PMD_{36}
84	PMD_{37}
85	PMD_{38}
86	PMD_{39}
87	EV_{SS}
88	PMD_{40}
89	PMD_{41}
90	PMD_{42}
91	PMD_{43}
92	EV_{DD}
93	PMD_{44}
94	PMD_{45}
95	PMD_{46}
96	PMD_{47}
97	IV_{SS}
98	IV_{DD}
99	EV_{SS}
100	$\overline{PMTS}$
101	$\overline{PMWR}$
102	PMACK
103	$\overline{PMRD}$
104	RCMP
105	EV_{DD}
106	$\overline{RESET}$

Pin	Pin Name
107	CLKIN
108	$\overline{DMRD}$
109	DMACK
110	$\overline{DMWR}$
111	EV_{DD}
112	$\overline{DMTS}$
113	IV_{SS}
114	IV_{DD}
115	TCLK
116	TMS
117	TDI
118	TDO
119	$\overline{TRST}$
120	PMPAGE
121	$\overline{PMS}_0$
122	$\overline{PMS}_1$
123	EV_{SS}
124	PMA_{23}
125	PMA_{22}
126	PMA_{21}
127	PMA_{20}
128	EV_{DD}
129	IV_{SS}
130	IV_{DD}
131	PMA_{19}
132	PMA_{18}
133	PMA_{17}
134	PMA_{16}
135	EV_{SS}
136	PMA_{15}
137	PMA_{14}
138	PMA_{13}
139	PMA_{12}
140	EV_{DD}
141	PMA_{11}
142	PMA_{10}

Pin	Pin Name
143	PMA_9
144	PMA_8
145	IV_{SS}
146	IV_{DD}
147	EV_{SS}
148	PMA_7
149	PMA_6
150	PMA_5
151	PMA_4
152	EV_{DD}
153	PMA_3
154	PMA_2
155	PMA_1
156	PMA_0
157	EV_{SS}
158	TIMEXP
159	EV_{DD}
160	EV_{SS}
161	IV_{SS}
162	IV_{DD}
163	$\overline{IRQ}_3$
164	$\overline{IRQ}_2$
165	$\overline{IRQ}_1$
166	$\overline{IRQ}_0$
167	EV_{DD}
168	$FLAG_0$
169	$FLAG_1$
170	$FLAG_2$
171	$FLAG_3$
172	EV_{SS}
173	DMA_0
174	DMA_1
175	DMA_2
176	DMA_3
177	IV_{SS}
178	IV_{DD}

Pin	Pin Name
179	EV_{DD}
180	DMA_4
181	DMA_5
182	DMA_6
183	DMA_7
184	EV_{SS}
185	DMA_8
186	DMA_9
187	DMA_{10}
188	DMA_{11}
189	EV_{DD}
190	DMA_{12}
191	DMA_{13}
192	DMA_{14}
193	IV_{SS}
194	IV_{DD}
195	DMA_{15}
196	EV_{SS}
197	DMA_{16}
198	DMA_{17}
199	DMA_{18}
200	DMA_{19}
201	EV_{DD}
202	DMA_{20}
203	DMA_{21}
204	DMA_{22}
205	DMA_{23}
206	EV_{SS}
207	DMA_{24}
208	DMA_{25}
209	IV_{SS}
210	IV_{DD}
211	DMA_{26}
212	DMA_{27}
213	EV_{DD}
214	DMA_{28}

Pin	Pin Name
215	DMA_{29}
216	DMA_{30}
217	DMA_{31}
218	EV_{SS}
219	DMPAGE
220	$\overline{BR}$
221	$\overline{BG}$
222	$\overline{DMS}_0$
223	$\overline{DMS}_1$
224	EV_{DD}
225	IV_{SS}
226	IV_{DD}
227	$\overline{DMS}_2$
228	$\overline{DMS}_3$
229	DMD_{39}
230	DMD_{38}
231	EV_{SS}
232	DMD_{37}
233	DMD_{36}
234	DMD_{35}
235	DMD_{34}
236	EV_{DD}
237	DMD_{33}
238	DMD_{32}
239	DMD_{31}
240	DMD_{30}
241	IV_{SS}
242	IV_{DD}
243	EV_{SS}
244	DMD_{29}
245	DMD_{28}
246	DMD_{27}
247	DMD_{26}
248	EV_{DD}
249	DMD_{25}
250	DMD_{24}

Pin	Pin Name
251	DMD_{23}
252	EV_{SS}
253	DMD_{22}
254	DMD_{21}
255	DMD_{20}
256	EV_{DD}

Pin Name	Type	Function
PMA_{23-0}	O	Program Memory Address. The processor outputs an address in program memory on these pins.
PMD_{47-0}	I/O	Program Memory Data. The processor inputs and outputs data and instructions on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 47-16 of the PMD bus.
$\overline{PMS}_{1-0}$	O	Program Memory Select lines. These pins are asserted as chip selects for the corresponding banks of program memory. Memory banks must be defined in the memory control registers. These pins are decoded program memory address lines and provide an early indication of a possible bus cycle.
$\overline{PMRD}$	O	Program Memory Read strobe. This pin is asserted when the processor reads from program memory.
$\overline{PMWR}$	O	Program Memory Write strobe. This pin is asserted when the processor writes to program memory.
PMACK	O	Program Memory Acknowledge. An external device asserts this input to add wait states to a memory access.
PMPAGE	O	Program Memory Page Boundary. The processor asserts this pin to signal that a program memory page boundary has been crossed. Memory pages must be defined in the memory control registers.
$\overline{PMTS}$	I/S	Program Memory Three-State Control. $\overline{PMTS}$ places the program memory address, data, selects, and strobes in a high-impedance state. If $\overline{PMTS}$ is asserted while a PM access is occurring, the processor will halt and the memory access will not be completed. PMACK must be asserted for at least one cycle when $\overline{PMTS}$ is asserted to allow any pending memory access to complete properly. $\overline{PMTS}$ should only be asserted (low) during an active memory access cycle.
DMA_{31-0}	O	Data Memory Address. The processor outputs an address in data memory on these pins.
DMD_{39-0}	I/O	Data Memory Data. The processor inputs and outputs data on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 39-8 of the DMD bus.

Pin Name	Type	Function
$\overline{DMS}_{3-0}$	O	Data Memory Select lines. These pins are asserted as chip selects for the corresponding banks of data memory. Memory banks must be defined in the memory control registers. These pins are decoded data memory address lines and provide an early indication of a possible bus cycle.
$\overline{DMRD}$	O	Data Memory Read strobe. This pin is asserted when the processor reads from data memory.
$\overline{DMWR}$	O	Data Memory Write strobe. This pin is asserted when the processor writes to data memory.
DMACK	I/S	Data Memory Acknowledge. An external device de-asserts this input to add wait states to a memory access.
DMPAGE	O	Data Memory Page Boundary. The processor asserts this pin to signal that a data memory page boundary has been crossed. Memory pages must be defined in the memory control registers.
$\overline{DMTS}$	I/S	Data Memory Three-State Control. $\overline{DMTS}$ places the data memory address, data, selects and strobes in a high-impedance state. If $\overline{DMTS}$ is asserted while a DM access is occurring, the processor will halt and the memory access will not be completed. DMACK must be asserted for at least one cycle when $\overline{DMTS}$ is de-asserted to allow any pending memory access to complete properly. $\overline{DMTS}$ should only be asserted (low) during an active memory access cycle.
CLKIN	I	External clock input to the processor. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{RESET}$	I/A	Sets the processor to a known state and begins execution at the program memory location specified by the hardware reset vector (address). This input must be asserted (low) at power-up.
$\overline{IRQ}_{3-0}$	I/A	Interrupt request lines; may be either edge triggered or level sensitive.
$FLAG_{3-0}$	I/O/A	External Flag. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{BR}$	I/A	Bus Request. Used by an external device to request control of the memory interface. When $\overline{BR}$ is asserted , the processor halts execution after completion of the current cycle, places all memory data, addresses, selects and strobes in a high impedance state, and asserts $\overline{BG}$. The processor continues normal operation when $\overline{BR}$ is released.
$\overline{BG}$	O	Bus Grant. Acknowledges a bus request ($\overline{BR}$), indicating that the external device may take control of the memory interface. $\overline{BG}$ is asserted (held low) until $\overline{BR}$ is released.
TIMEXP	O	Timer Expired. Asserted for four cycles when the value of the timer's 32-bit count register is decremented to zero.

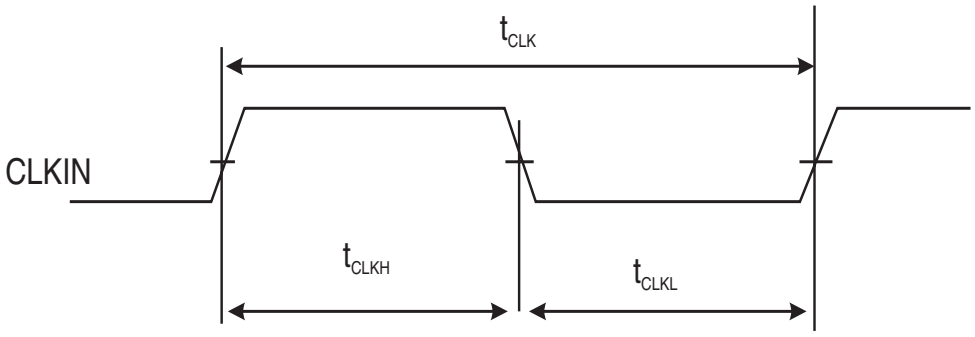
Pin Name	Type	Function
RCOMP	-	Not available. Can be set to any voltage level.
EV_{DD}	P	Power Supply (for output drivers); nominally +5Vdc (10 pins).
EV_{SS}	G	Power Supply return (for output drivers); (16 pins).
IV_{DD}	P	Power Supply (for internal circuitry); nominally + 5Vdc (4 pins).
IV_{SS}	G	Power Supply return (for internal circuitry); (7 pins).
TCLK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select. Used to control the test state machine. TMS has a 20kΩ internal pull-up resistor.
TDI	I/S	Test Data Input. Provides serial data for the boundary scan logic. TDI has a 20kΩ internal pull-up resistor.
TDO	O	Test Data Output. Serial scan output of the boundary scan path.
$\overline{TRST}$	I/A	Test Reset. Resets the test state machine. $\overline{TRST}$ must be asserted (pulled low) after power-up or held low for proper operation of the processor. $\overline{TRST}$ has a 20kΩ internal pull-up resistor.
NC	-	No Connect. No Connects are reserved pins that must be left open and unconnected.

NOTES:

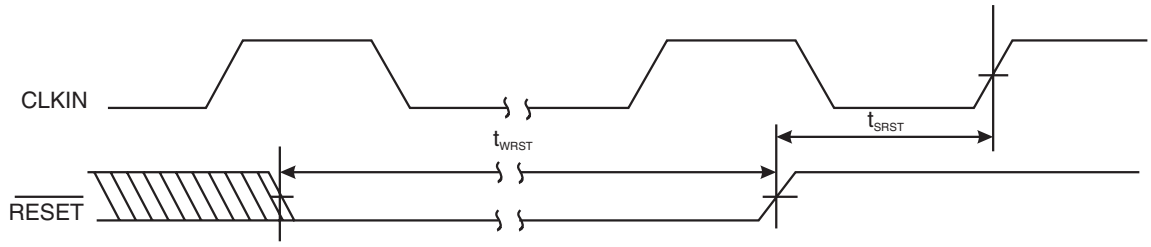
1. When groups of pins are identified with subscripts, e.g. PMD_{47-0}, the highest numbered pin is the most significant bit (in this case, PMD_{47}).
2. O = Output; I = Input; S = Synchronous; A = Asynchronous; P = Power Supply; G = Ground.
3. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCLK for TMS, TDI, and $\overline{TRST}$). Those that are asynchronous (A) can be asserted asynchronous to CLKIN.

1.10 TIMING DIAGRAMS

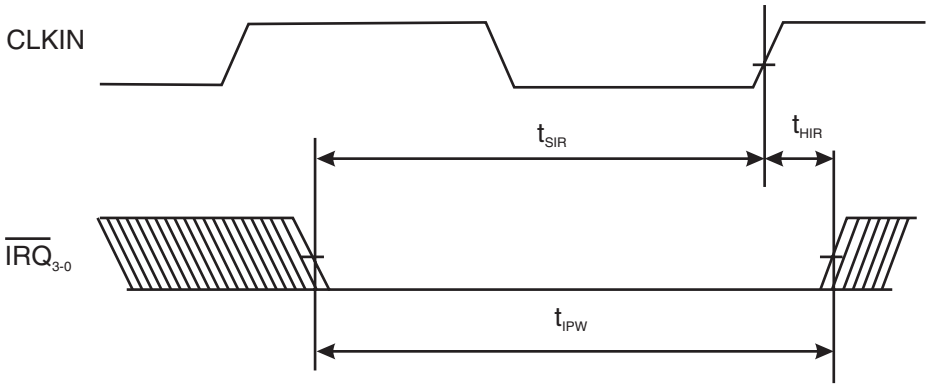
CLOCK TIMING



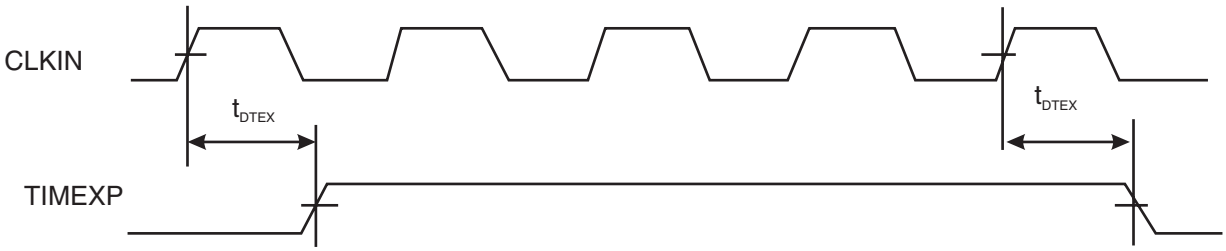
RESET TIMING



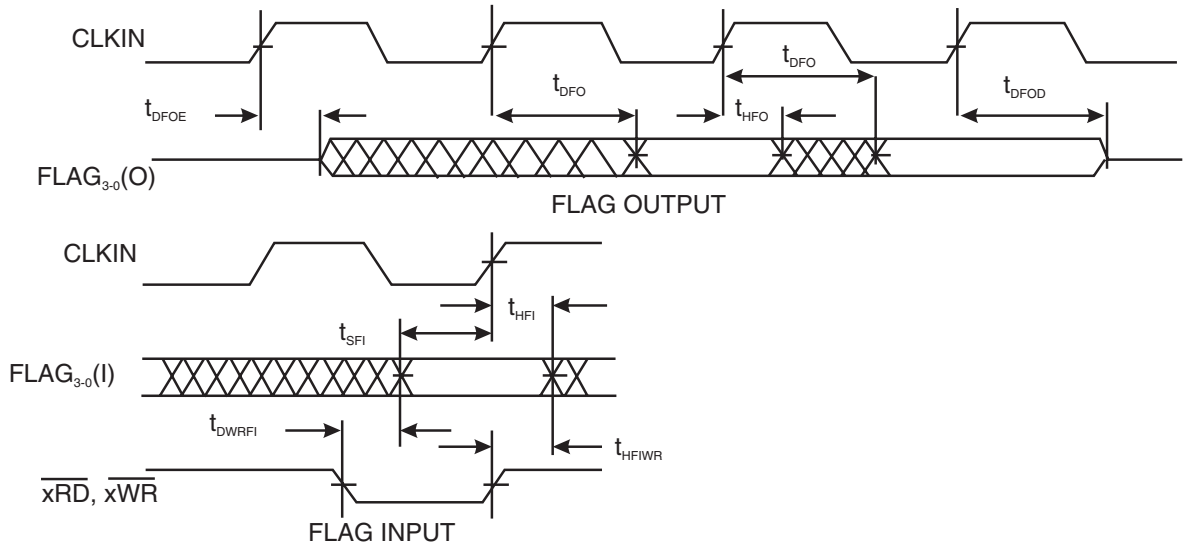
INTERRUPTS TIMING



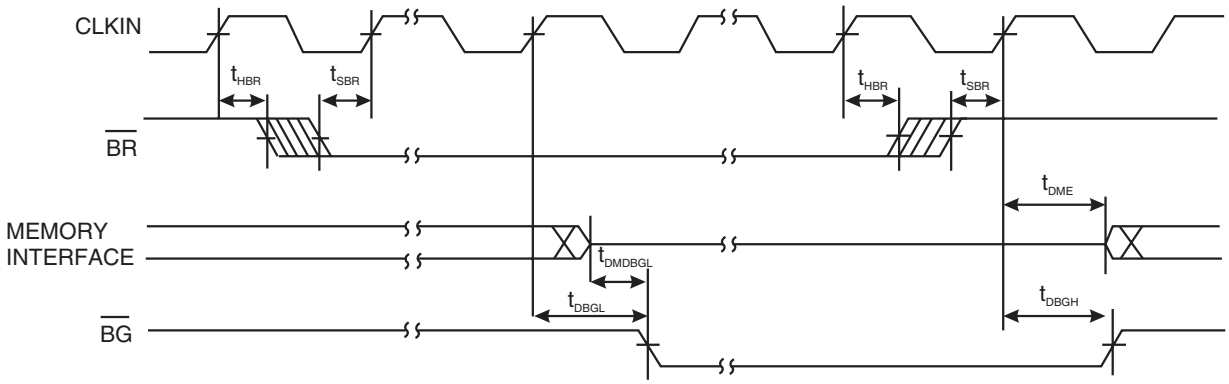
TIMER TIMING



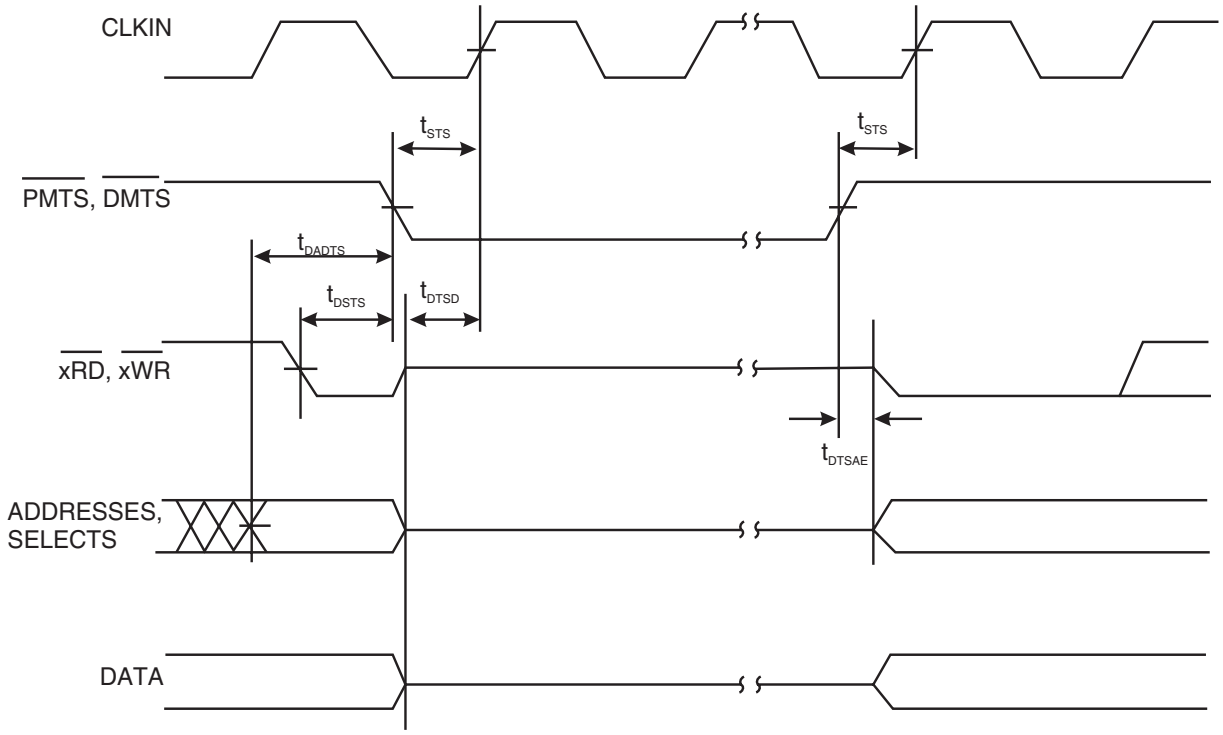
FLAG TIMING



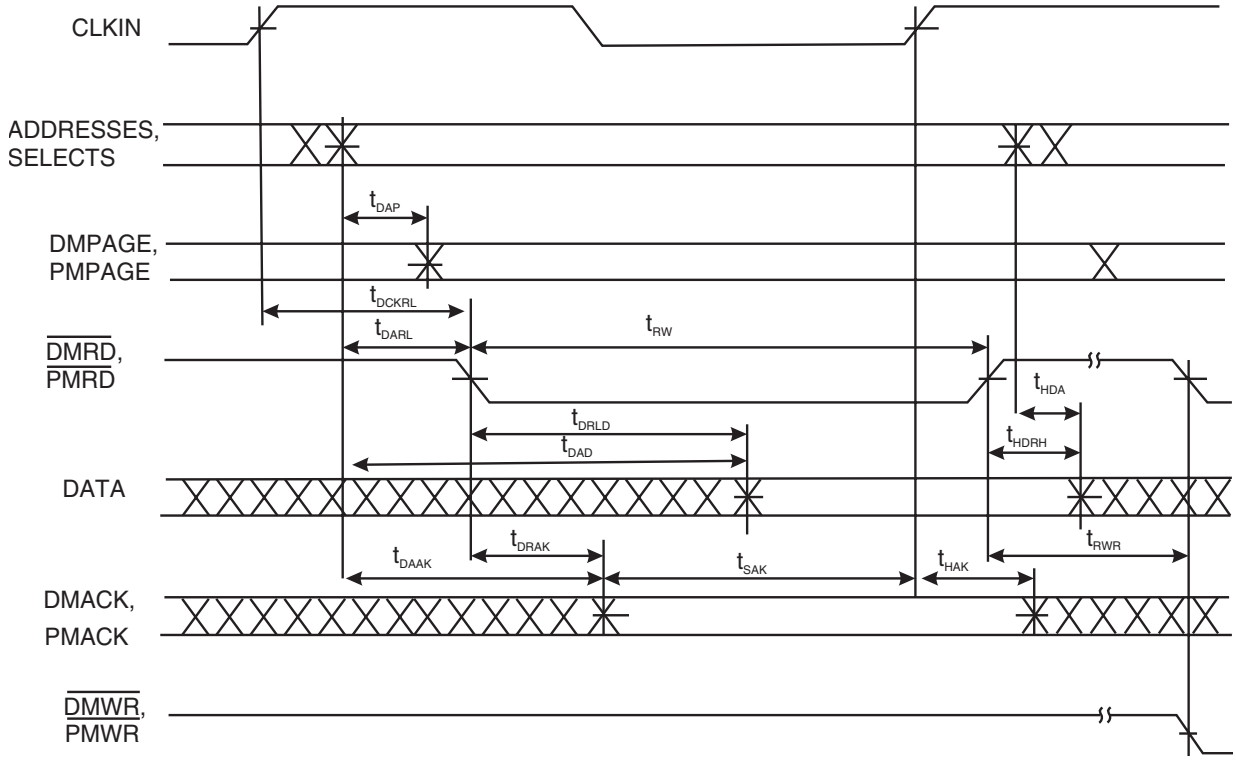
BUS REQUEST / BUS GRANT TIMING



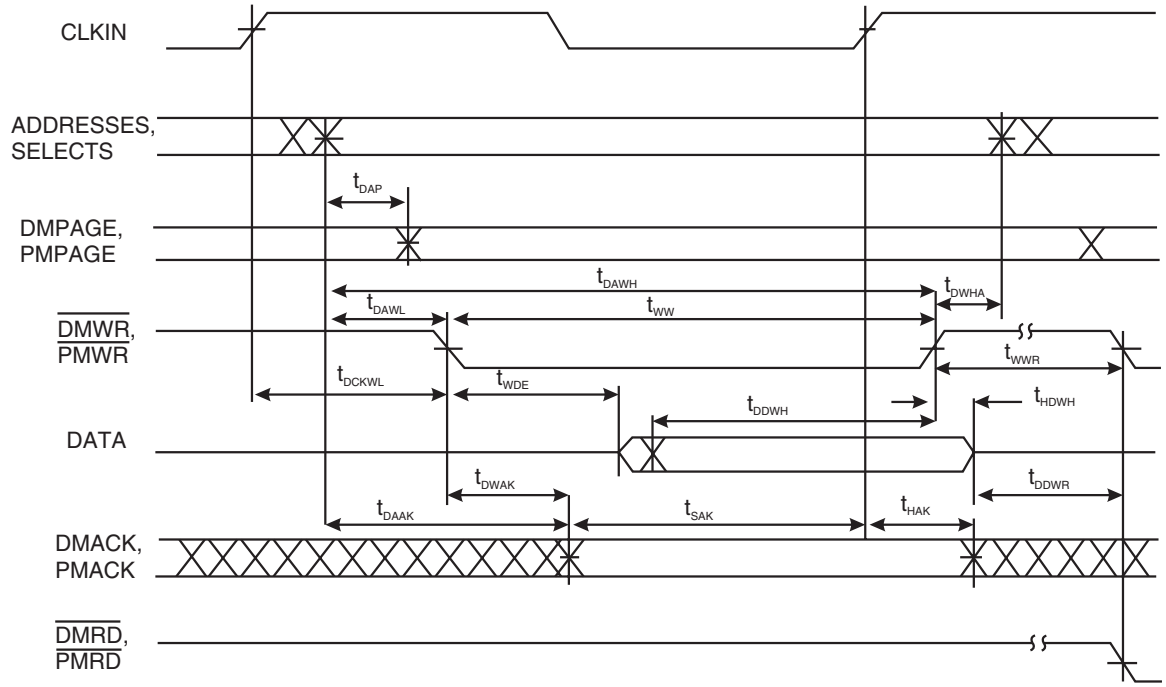
EXTERNAL MEMORY THREE-STATE CONTROL TIMING



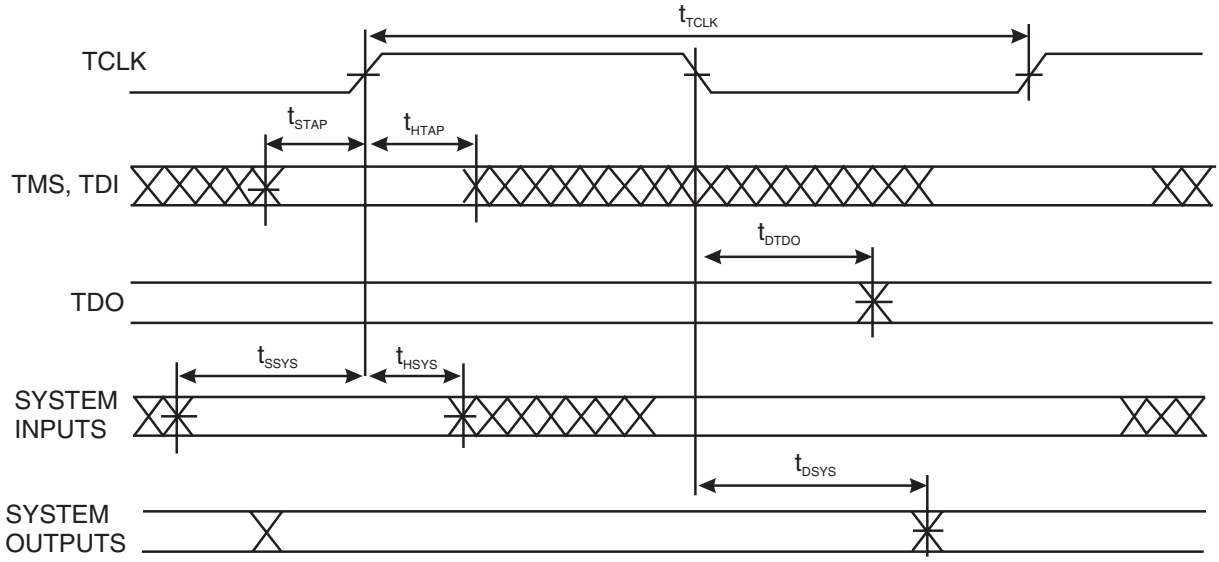
MEMORY READ TIMING



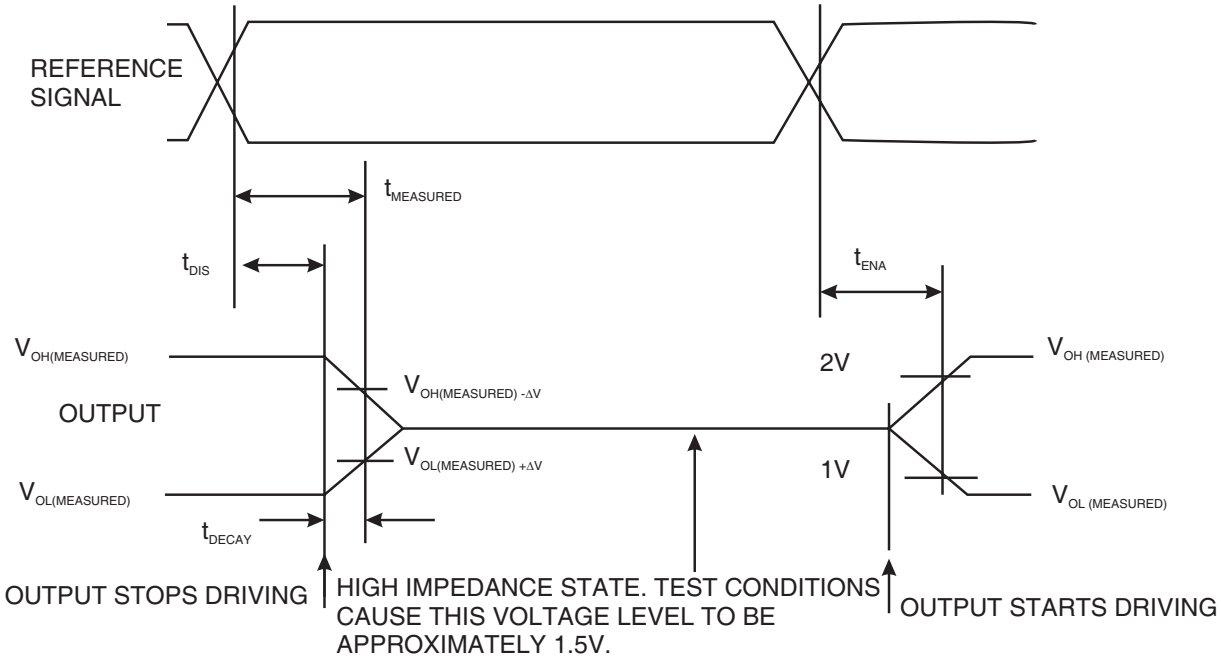
MEMORY WRITE TIMING



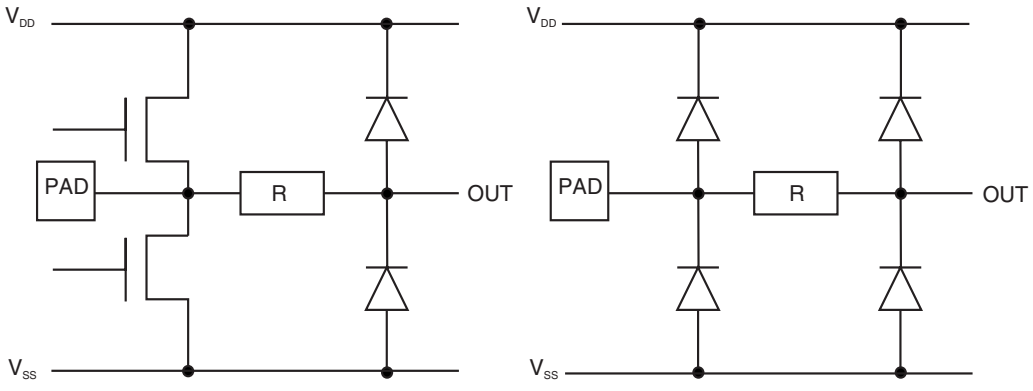
JTAG IEEE 1149.1 TEST ACCESS PORT TIMING



OUTPUT ENABLE/ DISABLE TIMING



1.11 PROTECTION NETWORKS



All Inputs/Outputs and all Outputs

All Inputs

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1 Basic Functional	-	3014	Verify Basic Functionality V_{IL}=0V, V_{IH}=3V f_{CLK}=20MHz V_{OL}≤1.45V, V_{OH}≥1.55V V_{DD}=4.5V, 5V and 5.5V V_{SS}=0V Note 2	-	-	-
Functional Test 2 Control Test	-	3014	Verify Control Functionality V_{IL}=0V, V_{IH}=3V f_{CLK}=20MHz V_{OL}≤1.45V, V_{OH}≥1.55V V_{DD}=4.5V, 5V and 5.5V V_{SS}=0V Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3 Complex Test	-	3014	Verify Complex Functionality V_{IL}=0V, V_{IH}=3V f_{CLK}=20MHz V_{OL}≤1.45V, V_{OH}≥1.55V V_{DD}=4.5V, 5V and 5.5V V_{SS}=0V Note 2	-	-	-
Functional Test 4 JTAG Test	-	3014	Verify JTAG Functionality V_{IL}=0V, V_{IH}=3V f_{CLK}=20MHz V_{OL}≤1.45V, V_{OH}≥1.55V V_{DD}=4.5V, 5V and 5.5V V_{SS}=0V Note 2	-	-	-
Internal Supply Current	I_{DDIN}	3005	V_{IL}=V_{ILC}=0.4V V_{IH}=2.4V, V_{IHCR}=3V t_{CLK}=50ns V_{DD}=5.5V V_{SS}=0V Note 3	-	430	mA
Idle Supply Current	I_{DDIDLE}	3005	V_{IN}=0V or V_{DD} V_{DD}=5.5V V_{SS}=0V Note 3	-	150	mA
Low Level Input Current 1	I_{IL1}	3009	V_{IN}=0V V_{DD}=5.5V V_{SS}=0V Note 4	-	-10	µA
Low Level Input Current 2	I_{IL2}	3009	V_{IN}=0V V_{DD}=5.5V V_{SS}=0V Note 5	-	-350	µA
High Level Input Current	I_{IH}	3010	V_{IN}=V_{DD} V_{DD}=5.5V V_{SS}=0V Notes 4, 5	-	10	µA
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3020	V_{OUT}=0V V_{DD}=5.5V V_{SS}=0V Note 6	-	-10	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	3021	V_{OUT}=V_{DD} V_{DD}=5.5V V_{SS}=0V Note 6	-	10	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Voltage	V_{OL}	3007	I_{OL}=4mA V_{DD}=4.5V V_{SS}=0V Note 7	-	400	mV
High Level Output Voltage	V_{OH}	3006	I_{OH}=-1mA V_{DD}=4.5V V_{SS}=0V Note 7	2.4	-	V
Low Level Input Voltage 1	V_{IL1}	-	V_{DD}=4.5V V_{SS}=0V Notes 8, 9, 11	-	800	mV
Low Level Input Voltage 2	V_{IL2}	-	V_{DD}=4.5V V_{SS}=0V Notes 10, 11	-	600	mV
High Level Input Voltage 1	V_{IH1}	-	V_{DD}=5.5V V_{SS}=0V Notes 8, 11	2	-	V
High Level Input Voltage 2	V_{IH2}	-	V_{DD}=5.5V V_{SS}=0V Notes 9, 10, 11	3	-	V
Input Capacitance	C_{IN}	3012	V_{IN}=2.5V V_{IN} (not under test) = 0V f=1MHz V_{DD}=V_{SS}=0V Note 12	-	10	pF
CLKIN Period (Clock Timing Diagram)	t_{CLK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	50	150	ns
CLKIN Width High (Clock Timing Diagram)	t_{CLKH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	10	-	ns
CLKIN Width Low (Clock Timing Diagram)	t_{CLKL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	10	-	ns
$\overline{\text{RESET}}$ Width Low (Reset Timing Diagram)	t_{WRST}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	200	-	ns
$\overline{\text{RESET}}$ Setup before CLKIN High (Reset Timing Diagram)	t_{SRST}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	29	50	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
$\overline{IRQ}_{3-0}$ Setup before CLKIN High (Interrupts Timing Diagram)	t_{SIR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	38	-	ns
$\overline{IRQ}_{3-0}$ Hold after CLKIN High (Interrupts Timing Diagram)	t_{HIR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
$\overline{IRQ}_{3-0}$ Pulse Width (Interrupts Timing Diagram)	t_{IPW}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	55	-	ns
CLKIN High to TIMEXP (Timer Timing Diagram)	t_{DTEX}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	24	ns
$FLAG_{3-0}$(I) Setup before CLKIN High (Flag Timing Diagram)	t_{SFI}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	19	-	ns
$FLAG_{3-0}$(I) Setup after CLKIN High (Flag Timing Diagram)	t_{HFI}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
$FLAG_{3-0}$(I) Delay from $\overline{xRD}$, $\overline{xWR}$ Low (Flag Timing Diagram)	t_{DWRFI}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	12	ns
$FLAG_{3-0}$(I) Delay from $\overline{xRD}$, $\overline{xWR}$ Deasserted (Flag Timing Diagram)	t_{HFIWR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
$FLAG_{3-0}$(O) Delay from CLKIN High (Flag Timing Diagram)	t_{DFO}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	24	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
$FLAG_{3-0}$(O) Hold after CLKIN High (Flag Timing Diagram)	t_{HFO}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	5	-	ns
CLKIN High to $FLAG_{3-0}$(O) Enable (Flag Timing Diagram)	t_{DFOE}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	1	-	ns
CLKIN High to $FLAG_{3-0}$(O) Disable (Flag Timing Diagram)	t_{DFOD}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	24	ns
$\overline{BR}$ Hold after CLKIN High (Bus Request/Bus Grant Timing Diagram)	t_{HBR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
$\overline{BR}$ Setup before CLKIN High (Bus Request/Bus Grant Timing Diagram)	t_{SBR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	18	-	ns
Memory Interface Disable to $\overline{BG}$ Low (Bus Request/Bus Grant Timing Diagram)	t_{DMDBGL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-2	-	ns
CLKIN High to Memory Interface Enable (Bus Request/Bus Grant Timing Diagram)	t_{DME}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	25	-	ns
CLKIN High to $\overline{BG}$ Low (Bus Request/Bus Grant Timing Diagram)	t_{DBGL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	22	ns
CLKIN High to $\overline{BG}$ High (Bus Request/Bus Grant Timing Diagram)	t_{DBGH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	22	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
$\overline{xTS}$ Setup before CLKIN High (External Memory Three-State Control Timing Diagram)	t_{STS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	14	50	ns
$\overline{xTS}$ Delay after Address, Select (External Memory Three-State Control Timing Diagram)	t_{DADTS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	28	ns
$\overline{xTS}$ Delay after $\overline{xRD}$, $\overline{xWR}$ Low (External Memory Three-State Control Timing Diagram)	t_{DSTS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	16	ns
Memory Interface Disable before CLKIN High (External Memory Three-State Control Timing Diagram)	t_{DTSD}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
$\overline{xTS}$ High to Address, Select Enable (External Memory Three-State Control Timing Diagram)	t_{DTSAE}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
Address, Select to Data Valid (Memory Read Timing Diagram)	t_{DAD}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	37	ns
$\overline{xRD}$ Low to Data Valid (Memory Read Timing Diagram)	t_{DRLD}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	24	ns
Data Hold from Address, Select (Memory Read Timing Diagram)	t_{HDA}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Data Hold from $\overline{xRD}$ High (Memory Read Timing Diagram)	t_{HDRH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-1	-	ns
xACK Delay from Address, Select (Memory Read Timing Diagram)	t_{DAAK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	27	ns
xACK Delay from $\overline{xRD}$ Low (Memory Read Timing Diagram)	t_{DRAK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	15	ns
xACK Setup before CLKIN High (Memory Read Timing Diagram)	t_{SAK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	14	-	ns
xACK Hold after CLKIN High (Memory Read Timing Diagram)	t_{HAK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
Address, Select to $\overline{xRD}$ Low (Memory Read Timing Diagram)	t_{DARL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	8	-	ns
xPAGE Delay from Address, Select (Memory Read Timing Diagram)	t_{DAP}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	1	ns
CLKIN High to $\overline{xRD}$ Low (Memory Read Timing Diagram)	t_{DCKRL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	16	26	ns
$\overline{xRD}$ Pulse Width (Memory Read Timing Diagram)	t_{RW}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	26	-	ns
$\overline{xRD}$ High to $\overline{xRD}$, $\overline{xWR}$ Low (Memory Read Timing Diagram)	t_{RWR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	17	-	ns
xACK Delay from $\overline{xWR}$ Low (Memory Write Timing Diagram)	t_{DWAK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	15	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Address, Select to $\overline{xWR}$ Deasserted (Memory Write Timing Diagram)	t_{DAWH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	37	-	ns
Address, Select to $\overline{xWR}$ Low (Memory Write Timing Diagram)	t_{DAWL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	11	-	ns
$\overline{xWR}$ Pulse Width (Memory Write Timing Diagram)	t_{WW}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	26	-	ns
Data Setup before $\overline{xWR}$ High (Memory Write Timing Diagram)	t_{DDWH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	23	-	ns
Address, Select Hold after $\overline{xWR}$ Deasserted (Memory Write Timing Diagram)	t_{DWHA}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	1	-	ns
Data Hold after $\overline{xWR}$ Deasserted (Memory Write Timing Diagram)	t_{HDWH}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
xPAGE Delay from Address, Select (Memory Write Timing Diagram)	t_{DAP}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	1	ns
CLKIN High to $\overline{xWR}$ Low (Memory Write Timing Diagram)	t_{DCKWL}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	16	26	ns
$\overline{xWR}$ High to $\overline{xWR}$ or $\overline{xRD}$ Low (Memory Write Timing Diagram)	t_{WWR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	17	-	ns
Data Disable before $\overline{xWR}$ or $\overline{xRD}$ Low (Memory Write Timing Diagram)	t_{DDWR}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	13	-	ns

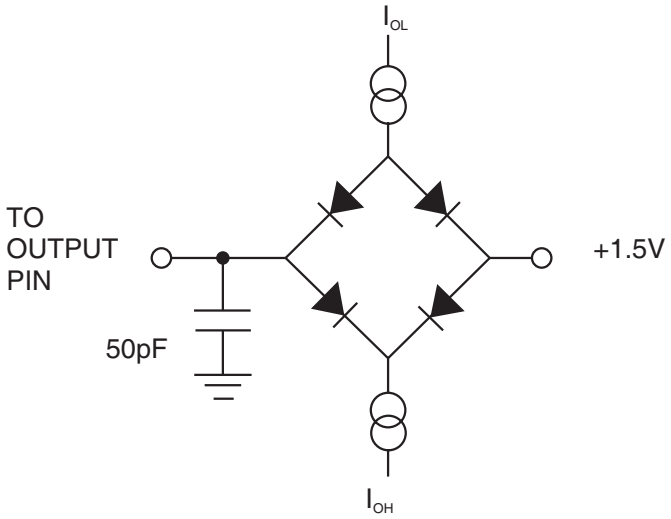
Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
$\overline{xWR}$ Low to Data Enabled (Memory Write Timing Diagram)	t_{WDE}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	0	-	ns
TCLK Period (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{TCLK}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	50	-	ns
TDI, TSM Setup before TCLK High (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{STAP}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	5	-	ns
TDI, TSM Hold after TCLK High (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{HTAP}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	6	-	ns
System Inputs Setup before TCLK High (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{SSYS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	7	-	ns
System Inputs Hold after TCLK High (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{HSYS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	9	-	ns
$\overline{TRST}$ Pulse Width (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{TRSTW}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	200	-	ns
TDO Delay from TCLK Low (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{DTDO}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	15	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
System Outputs Delay from TCLK Low (JTAG IEEE 1149.1 Test Access Port Timing Diagram)	t_{DSYS}	3003	f=20MHz V_{DD}=4.5V V_{SS}=0V Note 13	-	26	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed at each supply voltage with $t_r = t_f \leq 5$ns, Duty cycle 50% and with timings per specified limits. Unless otherwise specified, all timings per the timing diagrams specified herein shall be verified.
3. All IV_{DD} pins shall be tested.
4. The PMACK, $\overline{PMTS}$, DMACK, $\overline{DMTS}$, $\overline{IRQ}_{3-0}$, $\overline{BR}$, CLKIN, $\overline{RESET}$ and TCLK pins shall be tested.
5. The TMS, TDI and $\overline{TRST}$ pins shall be tested.
6. The PMA_{23-0}, PDM_{47-0}, $\overline{PMS}_{1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA_{31-0}, DMD_{39-0}, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE, $FLAG_{3-0}$ and TDO pins shall be tested.
7. The PMA_{23-0}, PDM_{47-0}, $\overline{PMS}_{1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA_{31-0}, DMD_{39-0}, $\overline{DMS}_{3-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE, $FLAG_{3-0}$, TIMEXP and $\overline{BG}$ pins shall be tested.
8. The PMD_{47-0}, PMACK, $\overline{PMTS}$, DMD_{39-0}, DMACK, $\overline{DMTS}$, $\overline{IRQ}_{3-0}$, $FLAG_{3-0}$, $\overline{BR}$, TMS and TDI pins shall be tested.
9. The $\overline{RESET}$ and $\overline{TRST}$ pins shall be tested.
10. The CLKIN and TCLK pins shall be tested.
11. Measurement shall be performed, on a go-no-go basis, during functional tests.
12. Guaranteed but not tested for all signal pins.
13. The timing characteristics shall be verfied on a go-no-go basis where the following shall apply:
    x = PM or DM.
    Address = PMA_{23-0}, DMA_{31-0}
    Data = PMD_{47-0}, DMD_{39-0}
    Select = $\overline{PMS}_{1-0}$, $\overline{DMS}_{3-0}$

    and the following output load shall be used:



2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125(+0-5)°C and T_{amb}=-55(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Internal Supply Current	I_{DDIN}	±43	-	430	mA
Idle Supply Current	I_{DDIDLE}	±15	-	150	mA
Low Level Input Current 1	I_{IL1}	±1	-	-10	µA
High Level Input Current	I_{IH}	±1	-	10	µA
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	±1	-	-10	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	±1	-	10	µA

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0-3)	°C
Inputs PMD_0 to PMD_{47}	V_{IN}	V_{DD}, V_{SS} per Note 1	V
Input CLKIN	V_{IN}	V_{GEN1} (Note 2)	V
Input $\overline{RESET}$	V_{IN}	V_{GEN2} (Note 2)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD} (Note 3)	V
Pulse Voltage	V_{GEN1}, V_{GEN2}	0 to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}, f_{GEN2}	1.6M 50 50± 15% Duty Cycle $t_r = t_f \leq 5$ns	Hz
Positive Supply Voltage IV_{DD}, EV_{DD}	V_{DD}	5(+0.5-0)	V
Negative Supply Voltage IV_{SS}, EV_{SS}	V_{SS}	0	V

NOTES:

1. The 48-bit (PMD_0 to PMD_{47}) input instruction code shall be configured as follows. Each input shall

be connected through a 4.7kΩ ±10% protection resistor.

Input	Condition	Input	Condition	Input	Condition	Input	Condition
PMD_0	V_{SS}	PMD_{12}	V_{SS}	PMD_{24}	V_{SS}	PMD_{36}	V_{DD}
PMD_1	V_{SS}	PMD_{13}	V_{DD}	PMD_{25}	V_{SS}	PMD_{37}	V_{DD}
PMD_2	V_{SS}	PMD_{14}	V_{DD}	PMD_{26}	V_{DD}	PMD_{38}	V_{SS}
PMD_3	V_{SS}	PMD_{15}	V_{DD}	PMD_{27}	V_{DD}	PMD_{39}	V_{SS}
PMD_4	V_{SS}	PMD_{16}	V_{SS}	PMD_{28}	V_{DD}	PMD_{40}	V_{SS}
PMD_5	V_{DD}	PMD_{17}	V_{SS}	PMD_{29}	V_{DD}	PMD_{41}	V_{SS}
PMD_6	V_{SS}	PMD_{18}	V_{SS}	PMD_{30}	V_{DD}	PMD_{42}	V_{SS}
PMD_7	V_{SS}	PMD_{19}	V_{DD}	PMD_{31}	V_{DD}	PMD_{43}	V_{SS}
PMD_8	V_{SS}	PMD_{20}	V_{DD}	PMD_{32}	V_{DD}	PMD_{44}	V_{DD}
PMD_9	V_{SS}	PMD_{21}	V_{SS}	PMD_{33}	V_{DD}	PMD_{45}	V_{DD}
PMD_{10}	V_{DD}	PMD_{22}	V_{DD}	PMD_{34}	V_{SS}	PMD_{46}	V_{SS}
PMD_{11}	V_{DD}	PMD_{23}	V_{DD}	PMD_{35}	V_{DD}	PMD_{47}	V_{SS}

2. CLKIN and RESET shall each be connected through a 1kΩ ±10% protection resistor.
3. All other inputs and outputs shall be connected through a 10kΩ ±10% protection resistor/load.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	°C
Inputs PMD_0 to PMD_{47}	V_{IN}	V_{SS} (Note 1)	V
Input CLKIN	V_{IN}	V_{GEN}	V
Input $\overline{RESET}$	V_{IN}	V_{DD} (Note 1, 2)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD} (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	7 50±15% Duty Cycle $t_r = t_f \leq 5ns$	MHz

Characteristics	Symbols	Test Conditions	Units
Positive Supply Voltage IV_{DD}, EV_{DD}	V_{DD}	5(+0.5-0)	V
Negative Supply Voltage IV_{DD}, EV_{DD}	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = Output Load = 4.7kΩ ±10%.
2. $\overline{\text{RESET}}$ is pulsed low (V_{SS}) for at least 200ns at power up then held at V_{DD}.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb}=22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in electrical measurements at Room Temperature.

The parameters to be measured during and on completion of radiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits		Units
		Min	Max	
Internal Supply Current	I_{DDIN}	-	450	mA
Idle Supply Current	I_{DDIDLE}	-	150	mA
Low Level Input Current 1	I_{IL1}	-	-10	µA
Low Level Input Current 2	I_{IL2}	-	-350	µA
High Level Input Current	I_{IH}	-	10	µA
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-	-10	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	10	µA
Low Level Output Voltage	V_{OL}	-	400	mV
High Level Output Voltage	V_{OH}	2.4	-	V