REQUIREMENTS FOR THE TECHNOLOGY FLOW QUALIFICATION OF FILM RESISTORS

ESCC Basic Specification No. 2544001

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1 PURPOSE

This specification provides additional information and requirements for the Qualification Approval of Film Resistors Technology Flows and Components and their inclusion on the ESCC Qualified Manufacturer's List (QML). It outlines the additional Film Resistors specific requirements for the definition of Technology Flow and its boundaries, the establishment of a Quality Management Programme, the preparation of a Process Capability and Reliability Assessment Programme, an Evaluation Test Programme and Qualification Test Programme, and the performance of an On-site Validation Audit.

This specification shall be read in conjunction with ESCC Basic Specification No. 25400.

This specification does not directly define detailed requirements for a resistor Manufacturer, but instead defines the points which the Manufacturer must address in his Quality Management Programme.

2 RELATED DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the Technology Flow certification.

2.1 APPLICABLE DOCUMENTS

(a) ESCC Basic Specification No. 25400, Requirements for the Technology Flow Qualification of Electronic Components for Space Application.
(b) ESCC Generic Specification No. 4001, Resistors, Fixed Film.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

4 INTRODUCTION

ESCC Technology Flow qualification is the status granted to a Manufacturer's specified Technology Flow after successful completion of an evaluation, certification and qualification programme as defined in ESCC Basic Specification No. 25400, the relevant parts of ESCC Generic Specification No. 4001 and this specification. It is also the status granted to any component type which is both:

- Manufactured using, and within the boundaries defined for, a qualified Technology Flow.
- Defined by, and meets the requirements of, ESCC Generic Specification No. 4001 and the relevant ESCC Detail Specification.

5 REQUIREMENTS

5.1 DEFINITION OF TECHNOLOGY FLOW BOUNDARIES

5.1.1 General

The Manufacturer shall define the Technology Flow for which certification and qualification is sought as required by ESCC Basic Specification No. 25400.

This Technology Flow definition shall also form the basis of a Process Identification Document (PID) to be produced by the Manufacturer which shall fulfil all of the requirements of ESCC Basic Specification No. 22700 in terms of content and configuration control.

This definition has to demonstrate that the Technology Flow and its corresponding boundaries represent a structured, properly controlled and monitored design methodology and manufacturing process for film resistors technologies.

To meet these requirements the definition should, as a minimum, address the areas listed in the following paragraphs at least to the extent detailed therein. The definition should cover all elements of the Technology Flow where a change could affect product performance and would therefore need to be reviewed by the Technology Review Board (TRB) before being introduced. Additional information should be supplied whenever necessitated by the particular nature of the technology under approval.

Within the definition of the Technology Flow, seven areas are of particular concern:

- The physical design and procedures which are closely related to the manufacturing process.
- The design system and procedures used to implement the circuit design methodology.
- The fabrication technologies and processes.
- The assembly processes.
- The package.
- Inspection and test requirements.
- Traceability.

These areas are addressed in the subsequent paragraphs.

5.1.2 Physical Design

The physical design is governed by a set of technology specific rules and parameters, commonly called 'Design Rules'. These rules define the construction and composition of all structures foreseen for the design and manufacture of a film resistor in a specific technology. The description of the physical design requires the definition of at least the following characteristics.

The layout design rule set which specifies the topology of all physical structures, including those for alignment and test purposes, and the substrates, in terms of:

- Function (e.g. conductor, contact, etc.).
- Shape (e.g. angles, etc.)
- Size (e.g. minimum/maximum, width/length/depth, etc.)
- Positioning (e.g. spacing between structures of equal or different nature).
- The thickness of all layers and constitutive elements.
- The resistor trimming rules (for laser and/or abrasive trimming).

The electrical rule and parameter set in terms of:

- Sheet resistivities of layers used for resistors.
- The current carrying capability of conductive layers.
- Breakdown voltages.

Other relevant parameters or restrictions not covered in the previous points like suitability to implement special circuit design techniques.

5.1.3 Design System

The design methodology is defined by the design system and all other procedures applied in the design of resistors. The design system comprises all software, basic design data and the hardware platform.

Technology Flow Qualification of a design system requires as a minimum:

1. The implementation of a configuration control guaranteeing the traceability of all software and data forming part of the system, and
2. The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documented and their application has to be evident.

At least the following items shall be covered in the PID:

(a) A general description of the design system representing:
  - The software structure of the system.
  - The design flow.

(b) A description of the hardware platform (e.g. work stations, etc.).

(c) The library of resistors shall be described at least in terms of the following relevant details:
  - The circuit symbol characterised by its name.
  - All relevant electrical characteristics and maximum ratings.
  - The detailed circuit.

The development process of the resistor library shall be described in terms of geometrical, functional, electrical and timing checks performed for verification.

(d) Software shall be described in terms of:
- The origin and version of the programme.
- A comprehensive description of its functional scope.
- The programming language and the amount of code.
- Definition of data formats and description languages.
- A description of the human interface with admitted or required interactivity and output format.
- All software serving simulation type purposes requires a detailed description of the underlying models and their parametric capability.

(e) A description of the configuration control system.
(f) A description of the quality assurance system.

5.1.4 Fabrication Processes

The fabrication processes to be covered by the description should include, but not be limited to, the following areas:

5.1.4.1 Materials

As a minimum the PID shall cover:

(a) The selection and approval of the material used.
(b) A list of fabrication materials and associated procurement specifications. This list shall include:
- Substrates.
- Conductor / Resistor materials.
- Photoresistive materials.
- Passivation, Glassivation and Assembly materials.
- Metallisation system.

(c) A list of incoming inspection procedures and other documents used to ensure the consistent quality of materials used.
(d) Procedures for traceability and control of limited shelf life items.

5.1.4.2 Fabrication Technologies and Processes

The manufacturer’s description of the basic technologies and processes used for the fabrication of the components shall at least cover:

- Type of Film technology (e.g. thin film, thick film, etc.)
- Physical location of fabrication line.
- Fabrication process sequence, flow and limits.
- Method of mask generation and identification.
- Curing / annealing temperature and duration.
- Resistor trimming processes.
- In-process controls & acceptance criteria.
- Sample plans (quantity and acceptance numbers).
- SPC implementation.
- Rework procedures.
- Lot formation.
- Cleanroom conditions.
- Handling and storage conditions.

5.1.4.3 Assembly Technologies and Processes

The assembly processes to be covered by the description should include, but not be limited to, the following areas:

- Substrate/Chip attach material, method and location.
- Wire bond/ Cap interconnect method.
- Seal technique (materials, sealing process and gas composition).
- Implementation procedure for internal visual inspection and other test methods.
- Assembly flow.
- Physical location of assembly operation.
- Scribing and resistor separation method (dicing of substrates).
- Resistors size.
- Periodic test and inspection procedures.
- Screening tests.
- Sample plans (quantity and acceptance numbers).
- Substrate/Chip back surface preparation.
- Contact geometry, spacing and metallisation.
- Device marking process.
- Lot formation.

5.1.5 Package

The package characteristics to be covered by the description should include, but not be limited to, the following areas:

- Vendor.
- Specification.
- Lot size.
- Incoming inspection.
- External dimensions.
- Cavity dimensions.
- Number of leads or terminals.
- Lead or terminal dimensions.
- Lead or terminal base material.
- Lead or terminal plating material.
- Body material.
- Body plating material.
- Body plating thickness.
- Substrate/Chip pad material.
- Substrate/Chip pad plating.
- Substrate/Chip pad plating thickness.
- Lid material.
- Lid plating materials.
- Lid plating thickness.
- Lid seal (preform) material.
- Lid glass seal material.
- Lid glass seal thickness.
- Lead glass seal material.
- Lead glass seal thickness.
- Leads or terminals spacing.
- Lead configuration.
- Maximum allowable Substrate/Chip size.
- Device marking process.
- Lead attachment.

5.1.6 Inspection and Test

The test facility characteristics to be covered by the description should include, but not be limited to, the following areas:

- Implementation procedures for external visual or other test methods.
- Testing flow.
- Physical location of test facility.
- Sample plans (quantity and acceptance numbers).
- Test procedures.
- Lot formation.

The Manufacturer shall describe inspection and test methods giving references to the documents specifying the methods. The following areas shall be covered as a minimum:

- Incoming inspection.
- In-process inspection.
- Substrate wafer acceptance testing.
- Precap inspection (if applicable).
- Screening and associated electrical tests.
- Qualification testing.
- Lot Validation testing or Periodic Testing.

5.1.7 Traceability

A traceability system must be defined which includes the maintenance of records which allow traceability from the device to a specific production lot.

At least the following points shall be addressed by such a traceability system:

- The use of purchase orders and specifications.
- The use of route sheets and travellers.
- The traceability of test vehicles.

5.2 QUALITY MANAGEMENT PROGRAMME

The following requirements, which are additional to the general requirements given in Section 6 of ESCC Basic Specification No. 25400, should be addressed in the Quality Management Programme for Film Resistors.

(a) Conversion of Customer Requirements (when applicable)
Mask generation procedure within the controlled design procedures.

Substrate wafer fabrication and assembly capabilities.

(b) Listing of Major Tests
Listing of major tests for which the ESCC Executive may request data to be submitted, including, where appropriate:
- Substrate wafer (lot) acceptance.
- Internal Visual.
- Preconditioning.
- Temperature/humidity testing.
- Temperature cycle.
- Burn-in.
- Life tests.

(c) Electrostatic discharge sensitivity programme

5.3 PARAMETRIC MONITORS, TEST VEHICLES

5.3.1 Parametric Monitors

The Manufacturer should have parametric monitor test structures to be used for measuring electrical characteristics of each Substrate wafer type in a specified technology. The parametric monitor test structures can be incorporated into the grid, within a device chip/substrate, as a dedicated drop-in chip/substrate or any combination thereof. Location of the parametric monitor test structures should be optimally positioned to allow for the determination of uniformity across the Substrate wafer.

The Manufacturer should establish and document reject limits and procedures for parametric measurements including which parameters will be routinely monitored and which will be included in the SPC programme. Documentation of the parametric monitor should also include parametric monitor test structure design and test procedure, including electrical measurements at temperature, if any and the relationship between the measured limits and those determined in the Manufacturer’s resistors, design and process rules. Alternative measurement techniques, such as in-line monitors are acceptable if properly documented. The following parameters are intended as a guideline to be used by the Manufacturer’s TRB in formulating suitable parametric monitors:

5.3.1.1 Sheet Resistance

Structures should be included to measure the sheet resistance of all conducting layers.

5.3.1.2 Temperature Coefficient

Structures should be included to measure Temperature Coefficient of all conducting layers.

5.3.2 Test Vehicles (TV) Programme

The Manufacturer should have a TV for the technology or process being considered for certification. A Manufacturer's standard evaluation component should be used to demonstrate fabrication process reliability for the technology.

Documentation procedures for the TV and standard production devices should be the same so that correlation can be made. The TV may be designed solely for its role as a quality and reliability monitoring vehicle or it may be a product intended for system use.

The TV should address the following requirements:

(a) Complexity
The TV should exercise the functionality of the process Technology Flow, be of a representative complexity.
(b) Functionality
Not applicable.
(c) Design
The TV should be designed to stress the design capabilities of the process. The architecture of the TV should be designed so that failures can be easily diagnosed.
(d) Fabrication
The TV should be processed on a Substrate wafer manufacturing line which is intended to be, or already is, a certified ESCC QML line.
(e) Packaging (if applicable)
The TV should be packaged in a package qualified in accordance with the requirements of the ESCC System.

Note that a different TV might be required whenever the design rules, the materials, the basic processes or the basic functionality of the technology differ.

5.4 PROCESS CAPABILITY AND RELIABILITY ASSESSMENT PLAN AND EVALUATION TEST PLAN

5.4.1 General

As part of evaluation the Manufacturer shall build test vehicles, and perform tests and analyses. These actions shall be designed to demonstrate, together with any existing information, the capabilities of the total manufacturing process with regard to quality, reliability and producibility and its suitability for producing space level components. The necessary activities shall be described in either a process capability and reliability assessment plan and/or an evaluation test plan which should cover all design, fabrication, assembly, test and control processes which comprise the total manufacturing process.

As a minimum the plans must generate sufficient information to allow for a process capability demonstration covering:

(a) Component Design.
(b) Substrate wafer fabrication.
(c) SPC or in-process monitoring programmes including parametric monitors and the TV.
(d) Substrate wafer acceptance.
(e) Assembly and packaging.

5.4.2 Design

In the plan(s), the Manufacturer should address the methodology for the following areas of design. The design procedure and tools should be controlled in such a manner that the ensuing resistor design performs only with limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electric, geometric and reliability).

5.4.2.1 Component Design

The plan(s) should address the information needed in the following areas of circuit design requirements and performance characteristics.

- Model verification
  It must be demonstrated that all models utilised in the design process are functional, predictable and accurate over the worst case temperature and electrical extremes.
- Layout verification
  It must be demonstrated that the automated or manual procedures routinely used for design, electrical and reliability rule checking are cover, as a minimum:

  (a) Design Rules Check: Geometric and physical.
  (b) Electrical Rules Check: Shorts, opens and connectivity.
  (c) Reliability Rules: Current density, Electrical fields and ESD.

5.4.3 Mask and Substrate Wafer Fabrication

The mask fabrication facility should be controlled such that an error free mask is produced from the resistors design database. This should include monitoring, controlling and reducing defect density.

The Manufacturer should identify a specific technology for the Substrate wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. The Substrate wafer manufacturing process should then be controlled with the following:

(a) In-line statistical control.
(b) A parametric monitor structure for measuring electrical parameters.

5.4.4 SPC and In-Process Monitoring Programme

The Manufacturer should have an in-process monitoring system to control key processing steps to ensure device yield, reliability.

The critical operations to be monitored should be determined by the Manufacturer based on his experience and knowledge of his processes. The resulting data should be analysed by appropriate SPC methods, when applicable.

The following should, as a minimum, be addressed for the substrate wafer fabrication process by the Manufacturer:

- Incoming mask and fabrication process materials.
- Equipment used for Substrate wafer fabrication.
- Metallisation deposition.
- Photolithography and resultant line width.
- Passivation process temperature and time.
- Annealing temperature and time.
- All reliability test data including the TV.
- Mask inspection.
- Parametric monitor test data.
- Substrate wafer acceptance data.
- Photoresistive processing, including rework procedures.
- Substrate wafer probe acceptance criteria.
- Rework.

5.4.5 Substrate Water Acceptance Plan

The Manufacturer shall have a Substrate wafer acceptance plan based on electrical and measurement of parametric monitors. This plan should utilise the parametric monitors and should include visual criteria, if applicable. The plan can be either a wafer by wafer acceptance plan or a Substrate wafer lot acceptance plan.

5.4.6 Assembly and Packaging

The Manufacturer should demonstrate the capability of the assembly and package processes by performing a qualification exercise on an actual product package.

5.4.6.1 Assembly Processes

The Manufacturer should list the assembly processes (chip/substrate attachment, wire bonding / cap insertion, sealing and marking) that are expected to be listed in the ESCC QML and used in ESCC QML resistors assembly and should then qualify these processes by the testing of fully assembled packages in accordance with appropriate tests for the assembly/packaging technology used. The assembly process related tests given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 4001, can be used by Manufacturers as a guide to suitable qualification tests. Sample sizes should be defined by the TRB.

5.4.6.2 Package Technology Styles

The Manufacturer should document how packages used in the manufacture of ESCC QML products are qualified. In particular, the Manufacturer should document his criteria for deciding which packages can be treated as similar and show how these are grouped together for qualification and change control purposes. Package technology style qualification test methodologies, vehicles and results should be available. Key package characteristics for which testing must be addressed on each ESCC QML package technology style are:

- Dimensions.
- Resistance to moisture.
- Susceptibility to corrosion.
- Lead/Termination integrity.
- Thermal resistance.
- Flammability.
- Outgassing.

The package technology related test given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 4001, can be used by Manufacturers as a guide to suitable testing. Sample sizes should be defined by the TRB.

5.4.7 TV Testing

As part of evaluation, as a minimum, the quantity of TV devices specified in the Process Capability and Reliability Assessment Programme or the Evaluation Test Programme is required randomly chosen from, an homogeneous Substrate wafer lot in the technology to be certified and from the fabrication facility to be certified. These Substrate wafer must have passed fabrication acceptance criteria. The number of TV device failures will serve as a qualification benchmark for the technology. Failure analysis should be performed on failed TVs to determine each failure category and action should be proposed and taken for correcting any problems found. The TV reliability data, including failure analysis results, should be prepared in a suitable form for review by the ESCC Executive.

5.5 ON-SITE VALIDATION AUDIT

5.5.1 General

The on-site audit by the ESCC Executive shall be performed in accordance with the requirements of ESCC Basic Specifications No. 20200 and No. 25400.

The on-site validation will be performed only after a satisfactory review of the Manufacturer's QM plan and self-validation results.

5.5.2 Technology Validation

A satisfactory review of the following areas during validation by the ESCC Executive, where applicable, is seen as critical for ESCC QML certification and should cover:

- Design procedures.
- Design review procedures.
- Software configuration and configuration management.
- Archival system.
- Mask inspection procedures TV and parametric monitor tests and data.
- Fabrication reworks procedures.
- SPC or In-process monitoring programmes.
- Design rule documentation.
- Clean room procedures.
- Substrate wafer traceability.
- Substrate wafer evaluation procedures.
- Assembly rework procedures.
- Chip/substrate attach procedures.
- Wire bonding / Cap insertion.
- Device traceability and travellers.
- Lot formation (Substrate wafer, device and inspection).
- Assembly area environmental control.
- Internal water vapour control programme.
- Electrostatic discharge control and testing.
- Visual inspection.
- Human contamination prevention procedures.
- Equipment calibration and maintenance.
- Training policy and procedures.
- Electrical test procedures.
- Screening procedures.
- Periodic testing procedures.
- Chip/substrate encapsulation/moulding.
- Qualification test plan.

5.6 QUALIFICATION TEST PLAN

5.6.1 Qualification Test Vehicles

The qualification test programme should define the relevant number of qualification test vehicles to cover the certified Technology Flow which the Manufacturer will produce on the certified manufacturing line. The qualification test vehicles should be of such complexity as to be representative of the ESCC QML resistors to be supplied by the Manufacturer. Each vehicle should operate and perform in compliance with the device specification, and should be manufactured in packages which are suitable for space use and which will not induce additional failures.

5.6.2 Qualification Test Plan

The qualification test plan should detail the test flow, test limits, test data to be measured, recorded and analysed, test sampling techniques and traceability records. As a baseline, the test flow should be based on the qualification testing specified in ESCC Generic Specification No. 4001 and the electrical measurements should be those given in the appropriate Detail Specification. The qualification test plan must be agreed and approved between the Manufacturer and the ESCC Executive.

5.6.3 Qualification Test Report

The Manufacturer should present to the ESCC Executive an analysis of the qualifying data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TV data monitoring is adequate and can be correlated to the process. The ESCC Executive should be notified of any improvements/changes to the certified ESCC QML Technology Flow as a result of evaluation of the qualification test results. The following data, if applicable, should be addressed and retained by the Manufacturer to support the results:

- Simulation results from the design process.
- Parametric monitor test data.
- Results of each subgroup test conducted, both initial and any resubmission.
- Number of devices tested and rejected.
- Failure mode and mechanism for each rejected device.
- Read and record variables data on all specified electrical parameter measurements.
- Where delta limits are specified, variable data, identified to the resistor serial number, should be provided for initial and final measurements.
- physical dimensions are checked, the actual dimensions of three randomly selected resistors should be recorded, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices has been approved.
- For bond/cap strength testing, the forces at the time of failure and the failure category, or the readings if a non-destructive method is implemented.
- For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.
- For lid torque strength testing, the forces at the time of failure or the actual torque if no failure occurs.
- For internal water vapour content readings, report of all gases found.

5.6.4 Qualification Test Failures

If any particular testing results are not successful, the Manufacturer should perform failure analysis and take any necessary corrective action after consultation with the ESCC Executive. The Manufacturer should notify the ESCC Executive of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

5.7 PROCUREMENT

Procurement of components manufactured within the boundaries of the qualified Technology Flow shall be in accordance with the requirements of ESCC Generic Specification No. 4001.