ELECTROSTATIC DISCHARGE SENSITIVITY TEST METHOD

ESCC Basic Specification No. 23800

Issue 2	February 2014

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
838	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1 SCOPE

1.1 GENERAL

This specification defines the basic requirements applicable to electrostatic susceptibility tests of electrostatic discharge sensitive (ESDS) components suitable for space application.

The electrostatic discharge sensitivity test method is considered to be destructive. Detailed requirements applicable to individual component types shall be specified in the relevant test plan and/or applicable ESCC Detail Specification.

1.2 PURPOSE

The purpose of this specification is to define the requirements for testing ESDS devices, including discrete semiconductors and integrated circuits, for definition of the electrostatic discharge susceptibility voltage range.

1.3 APPLICABILITY

The ESDS items subject to this specification are listed in Tables III-A, III-B and III-C

.

2 APPLICABLE DOCUMENTS

2.1 ESCC SPECIFICATIONS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of placing the purchase order or contract.

(a) ESCC Basic Specification No. 20600, Preservation, Packaging and Despatch of ESCC Electronic Components.
(b) ESCC Basic Specification No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.

2.2 OTHER (REFERENCE) DOCUMENTS

- DOD-HDBK-263, Military Handbook, Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).
- DOD-STD-1686, Appendix B, Electrostatic Discharge Control Programme for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) - Classification Testing.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. For the purpose of this specification, the following additional definitions shall be applicable:

- ESDS
  Electro Static Discharge Sensitive
- Critical failure path
  When the application of a test voltage to a given pin combination results in a failure on 2 consecutive similar components, that pin combination is a critical failure path.

4 CAUSES AND EFFECTS OF STATIC ELECTRICITY

4.1 NATURE OF STATIC ELECTRICITY

Static electricity is electrical charge at rest. The electrical charge is due to the transfer of electrons within a body (polarisation) or from one body to another (conductive charging). The transfer occurs due to interaction of charged bodies or uncharged bodies. The magnitude of the charge is primarily dependent on the size, shape, composition and electrical properties of the substances which make up the bodies.

Some substances readily give up electrons while others tend to accumulate excess electrons. A body having an excess of electrons is charged negatively; a body having an electron deficit is charged positively.

4.2 TYPICAL CHARGE SOURCES

Typical prime charge sources commonly encountered in a manufacturing facility are listed in Table I. These prime sources are essentially insulators and are typically synthetic materials. Electrostatic voltage levels generated with these insulators can be extremely high since they are not readily distributed over the entire surface of the substance or conducted to another contacting substance.

The conductivity of some insulating materials is increased by absorption of moisture under high humidity conditions onto the otherwise insulating surface, creating a slightly conductive humid layer which tends to distribute static charges over the material surface. The generation of 15000 Volts from common plastics in a typical manufacturing facility is usual.

TABLE I - TYPICAL PRIME CHARGE SOURCES

Object or Process	Material or Activity
Work Surfaces	- Waxed, painted or varnished surfaces - Common vinyl or plastics
Floors	- Sealed concrete - Waxed, finished wood - Common vinyl tile or sheeting
Clothes	- Common clean room smocks - Common synthetic personnel garments - Non-conductive shoes - Virgin cotton (1)
Chairs	- Finished wood - Vinyl - Fibreglass
Packaging and Handling	- Common plastic - bags, wraps, envelopes - Common bubble pack, foam - Common plastic trays, plastic tote boxes, vials, parts bins
Assembly, Cleaning, Test and Repair Areas	- Spray cleaners - Common plastic solder suckers - Solder irons with ungrounded tips - Solvent brushes (synthetic bristles) - Cleaning or drying by fluid or evaporation - Temperature chambers - Cryogenic sprays - Heat guns and blowers - Sand-blasting - Electrostatic copiers

NOTES
1. Virgin cotton can be a static source at low relative humidities such as below 30%.

4.3 TYPICAL ELECTROSTATIC VOLTAGE

Table II shows typical electrostatic voltages generated by personnel in a manufacturing facility.

TABLE II - TYPICAL ELECTROSTATIC VOLTAGES

Means of Static Generation	Electrostatic Voltages	
	10 to 20% Relative Humidity	65 to 90% Relative Humidity
Worker at bench	6000	100
Vinyl envelopes for work instructions	7000	600
Walking over vinyl floor	12000	250
Work chair padded with polyurethane foam	18000	1500
Common poly bag picked up from bench	20000	1200
Walking across carpet	35000	1500

4.4 ELECTROSTATIC DISCHARGE SENSITIVE COMPONENTS

Numerous components are susceptible to damage when ESD occurs across their terminals or when these components are exposed to electrostatic fields. ESDS components can be destroyed by an ESD when one pin is connected to a high voltage source and other pins are ungrounded.

A hard ground connection is not required to destroy an ESDS component. MOS large-scale integrated components in hermetic packages with non-conductive lids could be damaged for instance by spraying the lid with canned coolant despite there being no ground path connected to the component.

ESDS components installed in assemblies normally have their leads connected to a sufficient mass of conductive material such as printed wiring boards and wiring which may provide the required ground to result in damage from ESD. In such cases, however, the voltages required are normally higher than those needed when one or more pins or the component case is grounded. Components susceptible to ESD include:

- Microelectronic Components.
- Discrete Semiconductors.
- Film Resistors.
- Resistor Chips.
- Other Thick and Thin Film Components.
- Piezoelectric Crystals.

Known ESDS component types and their relative sensitivities are listed in Table III. component sensitivity is based upon 100pF, 1500Ω test circuit applying 1 discharge pulse. These sensitivity levels will vary for different test circuits and generally will be substantially less where multiple discharge pulses are applied.

TABLE III - LIST OF ESDS COMPONENTS

TABLE III-A - CLASS 1: SENSITIVITY RANGE 0 TO ≤1000 VOLTS

Metal Oxide Semiconductor (MOS) devices, including C, D, N, P, V and other MOS technology without protective circuitry, or protective circuitry having Class 1 sensitivity.
Surface Acoustic Wave (SAW) devices.
Operational Amplifiers (OP AMP) with unprotected MOS capacitors.
Junction Field Effect Transistors (JFET's).
Silicon Controlled Rectifiers (SCR's) with I_O <0.175 amperes at +100° Celsius (°C) ambient temperature.
Precision Voltage Regulator Microcircuits: Line or Load Voltage Regulation <0.5%.
Microwave and Ultra-High Frequency Semiconductors and Microcircuits: Frequency >1 gigahertz.
Thin Film Resistors (Type RN) with tolerance of ≤0.1%; power >0.05 watt.
Thin Film Resistors (Type RN) with tolerance of >0.1%; power ≤0.05 watt.
Large-Scale Integrated (LSI) Microcircuits, including microprocessors and memories without protective circuitry, or protective circuitry having Class 1 sensitivity. (Note: LSI devices usually have 2 to 3 layers of circuitry with metallisation cross-overs and small geometry active elements).
Hybrids utilising Class 1 parts.

TABLE III-B - CLASS 2: SENSITIVITY RANGE >1000 TO ≤4000 VOLTS

MOS devices or devices containing MOS constituents including C, D, N, P, V or other MOS technology with protective circuitry having Class 2 sensitivity.
Schottky diodes.
Precision Resistor Networks (Type RZ).
High Speed Emitter Coupled Logic (ECL) Microcircuits with propagation delay ≤1 nanosecond.
Transistor-Transistor Logic (TTL) Microcircuits (Schottky, low power, high speed, and standard).
Operational Amplifiers (OP AMP) with MOS capacitors with protective circuitry having Class 2 sensitivity.
LSI with input protection having Class 2 sensitivity.
Hybrids utilising Class 2 parts.

TABLE III-C - CLASS 3: SENSITIVITY RANGE >4000 TO ≤15000 VOLTS

Low Power Chopper Transistors.
Resistor Chips.
Small Signal Diodes with power ≤1 watt, excluding Zeners.
General Purpose Silicon Rectifier Diodes and Fast Recovery Diodes.
Low Power Silicon Transistors with power <5 watts at +25°C.
All other Microcircuits not included in Class 1 or Class 2.
Piezoelectric Crystals.
Hybrids utilising Class 3 parts.

4.5 FAILURE MECHANISMS

Various ESD failure mechanisms can occur within microelectronic and semiconductor devices. These failure mechanisms are power or voltage dependent as shown in Table IV.

TABLE IV- FAILURE MECHANISMS

Failure Mechanism	Power	Voltage
a. Thermal secondary breakdown	X	
b. Metallisation melt	X	
c. Dielectric breakdown		X
d. Gaseous arc discharge		X
e. Surface breakdown		X
f. Bulk breakdown	X	

All the above mentioned failure mechanisms can be observed on semiconductors and other components. Failure mechanisms (b) and (d) are evident for film resistors and failure mechanism (f) for piezoelectric crystals.

Besides these catastrophic failure mechanisms, unencapsulated chips and LSI MOS integrated circuits have exhibited temporary failure due to failure mechanism (d) from positive charges deposited on the chip as a by-product of gaseous arc discharge within the package between the lid and the substrate.

5 ELECTROSTATIC DISCHARGE TEST

5.1 GENERAL

The purpose of ESD testing is to determine the susceptibility of a component to damage from ESD by establishing a sensitivity Class in accordance with of this specification and ascertaining the minimum voltage at which critical path failure occurs.

ESD testing shall be performed ideally as part of the Evaluation Test Programme (ETP) for the component under examination.

Where an ETP has been completed without performance of an ESD Test, retrospective testing shall be performed on component types listed in Tables III-A, III-B and III-C of this specification if the sensitivity Class and the Minimum Critical Path Failure Voltage, as above, are unknown.

5.1.1 Human ESD Model

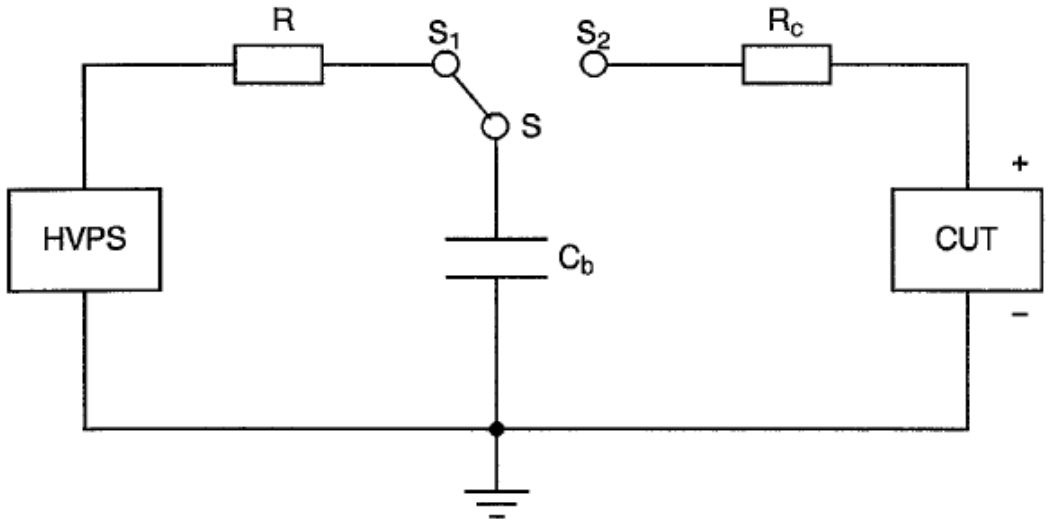
Human beings are main sources of ESD for damaging components. The test circuit used for ESD testing is therefore based upon a human discharge model. Electrostatic discharges generated by rubbing or separating materials are readily transmitted to a person's conductive humid skin causing that person to be charged. When a charged person handles, or comes in close proximity of, an ESDS component, this person can damage that component from direct discharge by touching the component or by subjecting the component to an electrostatic field. ESD from a person can be reasonably simulated for test purposes by means of the test circuit shown in Figure I.

Test voltages are measured across the capacitance. The capacitor shall be discharged through the series resistor into the component under test by maintaining the bounceless switch to the discharge position for a time no shorter than required to decay the capacitor voltage to less than 1% of the test voltage or 5 seconds, whichever is less. Power supply voltage shall be within a tolerance of ±5% of test voltage.

CAUTION NOTE

ESD testing should be considered to be destructive. Components subjected to ESD testing should not be used as deliverable hardware due to the possibility of component degradation or latent defects.

FIGURE I - HUMAN BODY MODEL TEST CIRCUIT



HVPS	=	High Voltage Power Supply 0 to 20000 Volts.
R	=	Current Limiting Resistor.
S	=	Bounceless High Voltage Switch.
S_1	=	Charge Position.
S_2	=	Discharge Position.
C_b	=	Source Body Capacitance 100pF ±5%.
R_c	=	Non-inductive Resistance 1.5kΩ ±5%.
CUT	=	Component Under Test.

5.2 ESD CLASSIFICATION PROCEDURE

5.2.1 Component Functional Test

The electrical parameters of a component, applicable to the component pin combination being tested (Table V) shall be measured and recorded prior to and after the performance of ESD testing.

5.2.2 Component Failure Definition

A component shall be considered failed when the component functional test performed after ESD testing indicates that one or more electrical parameters do not meet the limits of the applicable ESCC Detail Specification.

A failed component shall not be used in further testing since the failure could affect electrical parameters of other pin combinations.

5.2.3 Determination of Critical Failure Path

The critical failure path shall be determined according to Chart I using the pin combinations listed in Table V. In addition to the pin combinations of Table V, where metallisation cross-overs exist in microelectronic devices, the pin combinations which could result in puncture of the dielectric between these cross-overs should also be tested.

If the component's classification is unknown, start at Para. (a) below.

If the component is Class 1 and the intention is to reclassify the component as Class 2 or 3, start at Para. (d) below.

If the component is Class 2 and the intention is to reclassify the component as Class 3, start at Para. (e) below.

Class 1, Sensitivity Range: 0 to 1000 Volts

(a) Measure electrical parameters applicable to the pin combinations shown in Table V. With the test circuit of Figure I apply a test voltage of 1250 Volts to each pin combination shown in Table V.
Re-measure electrical parameters after testing each pin combination. Test until a failure occurs or until all pin combinations have been tested without a failure.
If a failure occurs, proceed to (b); if no failure occurs, proceed to (d).

(b) Repeat (a) for a second component using the same pin combination in which the first failure occurred, using the same voltage.
If a second failure occurs, the pin combination tested shall be designated as a critical path.

(c) Continue with (a), using a new component (or the component used for (b) if no failure occurs) for the remaining pin combinations to determine whether other critical paths exist.

Class 2, Sensitivity Range: 1000 to 4000 Volts

(d) Repeat (a) followed by (b) and (c) if applicable, for pin combinations that were not previously found to be critical paths, using 5000 Volts in place of 1250 Volts and a new component if necessary.

Class 3, Sensitivity Range: 4000 to 15000 Volts

(e) Repeat (d), but using 18750 Volts in place of 5000 Volts and a new component if necessary.

(f) Rank critical paths in ascending order of their voltage sensitivity as determined by (a) to (e).

(g) Proceed to the testing specified in Para. 5.2.4 if a critical path has been found.

5.2.4 ESD Classification Testing

The test procedure shall be in accordance with the Chart II using a sample size of 10 components.

The components shall be tested using the test circuit of Figure I for each critical path determined in Para. 5.2.3. Continue testing until 10 components have been tested or until 2 components have failed on the same critical path at a given voltage level. Start with the lowest voltage ranked critical path.

- If the critical path was determined in Para. 5.2.3(a) and (b), use 1000 Volts as the test voltage.
- If the critical path was determined in Para. 5.2.3(d), use 4000 Volts as the test voltage.
- If the critical path was determined in Para. 5.2.3(e), use 15000 Volts as the test voltage.

Using this procedure, components will be classified into ESD sensitivity class 1, 2 or 3 or unclassified if not more than 1 failure occurs for a given critical path.

5.2.5 Critical Path Failure Voltage Testing

When the classification procedure detailed in Para. 5.2.4 has been completed, the value of the Minimum Critical Path Failure Voltage shall be found for components which have been categorised into one of the three sensitivity classes. The test procedure shall be as given below, using components from Para. 5.2.4 on which no critical path failures have been found.

Using the test circuit in Figure I, the value shall be established by increasing the test voltage applied to the critical path under test from the minimum voltage for the class into which the failure falls, upwards, until such time as failure occurs.

The increase in voltage shall be made on a "stepped" basis until the value of the failure voltage has been determined. A "voltage step" shall be approximately 10% of the maximum test voltage for the class.

Where more than one critical path is to be tested for a component type, the lowest value measured shall be the Critical Path Failure Voltage.

5.2.6 ESD Warning

If an ESD classification is allocated to a component, the classification number and the minimum critical path failure voltage, as determined using Paras 5.2.3 and 5.2.5, shall be included into an ESD Warning paragraph to be inserted into Section 1 of the Detail Specification.

The warning paragraph shall take the following form:

1.x HANDLING PRECAUTIONS

These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, shipment and any handling.

These components are categorised as Class X with a Minimum Critical Path Failure Voltage of XXXXX Volts.

TABLE V- PIN COMBINATIONS FOR ESD TESTING

Component Types	Pin Combinations
All components	- All pins tied together (+) to top centre of case (-) - All pins tied together (-) to top centre of case (+)
Resistors	- Terminal (+) to terminal (-)
Diodes	- Anode (+) to cathode (-) - Anode (-) to cathode (+)
Transistors	- Emitter to base (1) - Base to collector (1)
Digital Microcircuits	- Input (+) to common (-) (2) - Output (-) to common (+) (2) - Input (+) to output (-) - V+ (-) to common (+)
Linear Microcircuits	- Input (+) to common (-) - Input (+) to input (-) - Output (-) to common (+) - V+ (-) to common (+)

MOS FET's and JFET's	- Gate to source (1) - Gate to drain (1)

NOTES

1. Both polarity (+) to (-) and (-) to (+).
2. Common

For NPN technology microcircuits, common is the most negative terminal (i.e. V- or GND). For PNP technology, common is GND.

CHART I - CRITICAL PATH DETERMINATION

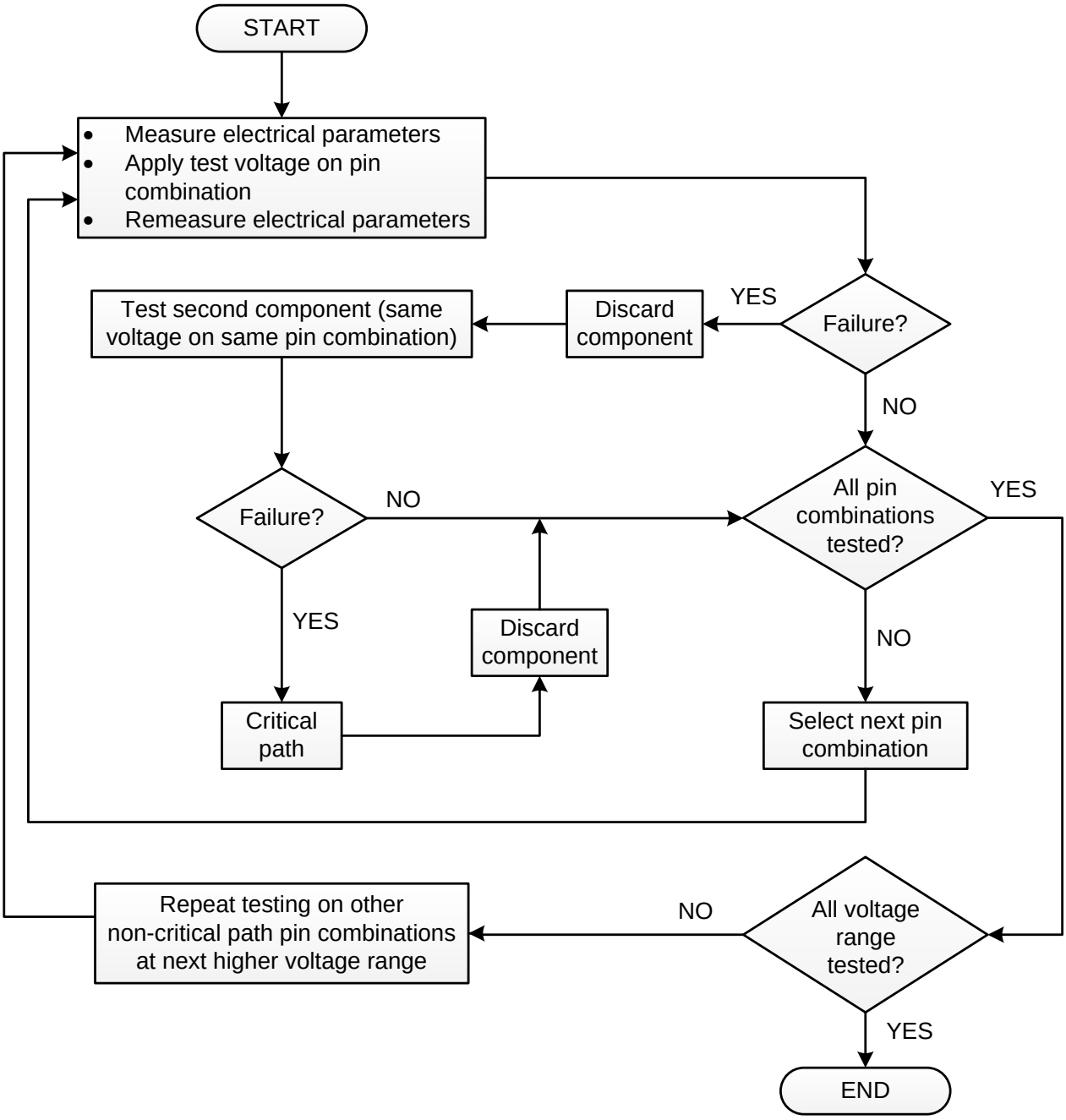


CHART II – CLASSIFICATION TESTING