INTERNAL VISUAL INSPECTION

OF DISCRETE NON-MICROWAVE

SEMICONDUCTORS

ESCC Basic Specification No. 2045000

ISSUE 1

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Pages 1 to 53

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SEMICONDUCTORS

ESA/SCC Basic Specification No. 2045000

space components
coordination group

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1. SCOPE

1.1 This specification, to be read in conjunction with ESA/SCC Basic Specification No. 20400, 'Internal Visual Inspection', contains additional requirements for Discrete Non-Microwave Semiconductor devices, which shall be applied to each device. It is divided into the following Paras:-

Para. 2 - General Requirements, Procedure and Definitions

Para. 3 - Detailed Requirements:

- 3.1 Magnification.
- 3.2 Bipolar Transistors, FET's and Diodes (Not Glass Encapsulated).
- 3.3 Diodes (Glass Encapsulated).

1.2 Para. 2 defines all terms used throughout this document and is common to Para. 3.

1.3 By referencing the index, specific detailed information may be extracted for each individual part type and inspection, as required.

2. GENERAL REQUIREMENTS

2.1 PROCEDURE

All header assemblies and packages shall be given a microscopic examination immediately prior to encapsulation in an area where the standard of cleanliness is not less than that of the assembly area.

All items shall be examined in such a manner that a minimum of handling and movement of the component is involved. Except for glass encapsulated devices (see Para. 3.3.1), the inspection shall be performed either perpendicular to the die surface, using vertically incident light for metallisation, oxide, diffusion and ball location defects, or within an angle of 30° from the perpendicular to the die surface for internal leads and package condition, using suitable illumination, with a monocular, binocular or stereo microscope.

2.2 DEFINITIONS

2.2.1 Scratch

A scratch is any tear, discontinuity of tooling mark in or on the metallisation, detected at the specified magnification, whether or not the bare semiconductor material and /or the oxide is exposed.

2.2.2 Crack (see Figure II)

A crack is a fracture that extends through the thickness of the die.

2.2.3 Chip-out (See Figure II)

A chip-out is any section of the die which has broken away from the main body of the die.

2.2.4 Void (See Figure III)

(a) A void is any region in the metallisation, not caused by a scratch, where bare semiconductor material or oxide is visible within the design areas of the metallisation.

(b) In the case of die-mounting, a void is the absence of die attach material in the defined areas.

(c) In the case of glassivation, a void is the absence of glassivation over any active circuit area of the die.

2.2.5 Contact Window

A contact window is an opening in the dielectric (normally oxide), usually covered by metallisation where electrical contact is made with an underlying layer.

2.2.6 Bonding Pad

A bonding pad is that part of the metallisation where an electrical connection to the package terminal is to be made.

2.2.7 Excess Metallisation (see Figure IV)

Excess metallisation is metallisation extending beyond the normal designed pattern, or in isolated islands, caused by smearing or defecting photo-engraving.

2.2.8 Pinhole

A pinhole is a small hole which exposes underlying material.

2.2.9 Die

Individual pieces of semiconductor wafer in which a transistor or diode is contained. Some examples of die terminology are given in Figure I.

2.2.10 Bond-Off

A bond made in the process of clearing the bonding tool following an unsuccessful bond attempt.

2.2.11 Rebonding

A second bonding made between two pads, or a pad and a bonding terminal, to replace the original bonded wire, which has either been removed, leaving the welded portion of the bond attached to the pad or bonding terminal, or which failed to adhere at the first bonding attempt.

2.2.12 Crazing

The presence of minute cracks in the glassivation.

2.2.13 Active Surface Area

Any area where electrical contact may be made to the n or p regions of the die. Where a chip contains a number of devices i.e. built-in redundancy, the term active area shall only refer to the devices which are bonded.

2.2.14 Passivation

Silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the depositing of any metal.

2.2.15 Glassivation

The top layer(s) of transparent insulation material which cover(s) the active circuit area including metallisation, but excluding bond pads.

2.2.16 Foreign Matter

Any semiconductor materials, metal particles, carbonised particles or other extraneous organic or inorganic materials which should not be present.

2.2.17 Conductive Foreign Matter

Any substance which appears opaque under all conditions of lighting and magnification used in routine visual inspections.

FIGURE I - DIE TERMINOLOGY

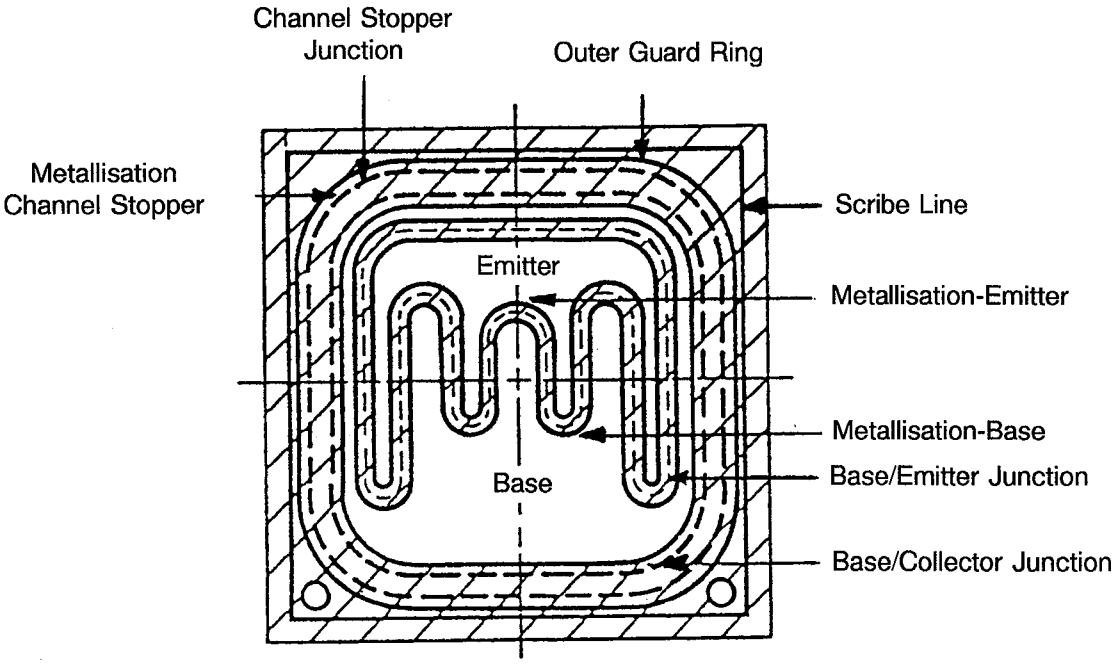
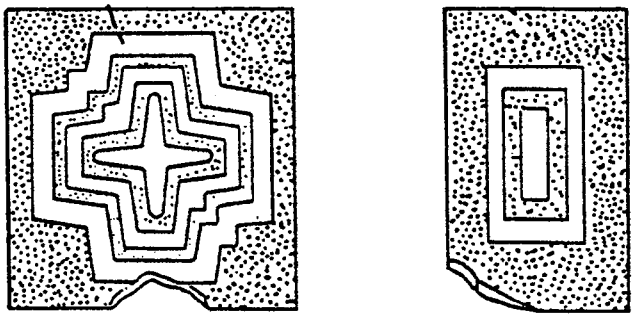
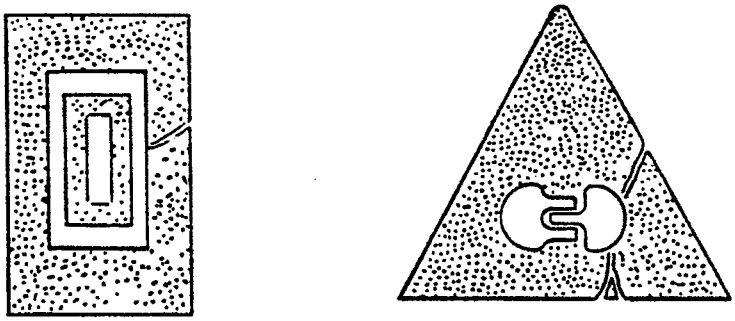


FIGURE II - CHIPPED AND CRACKED DIE



Chipped Die



Cracked Die

FIGURE III - VOIDS

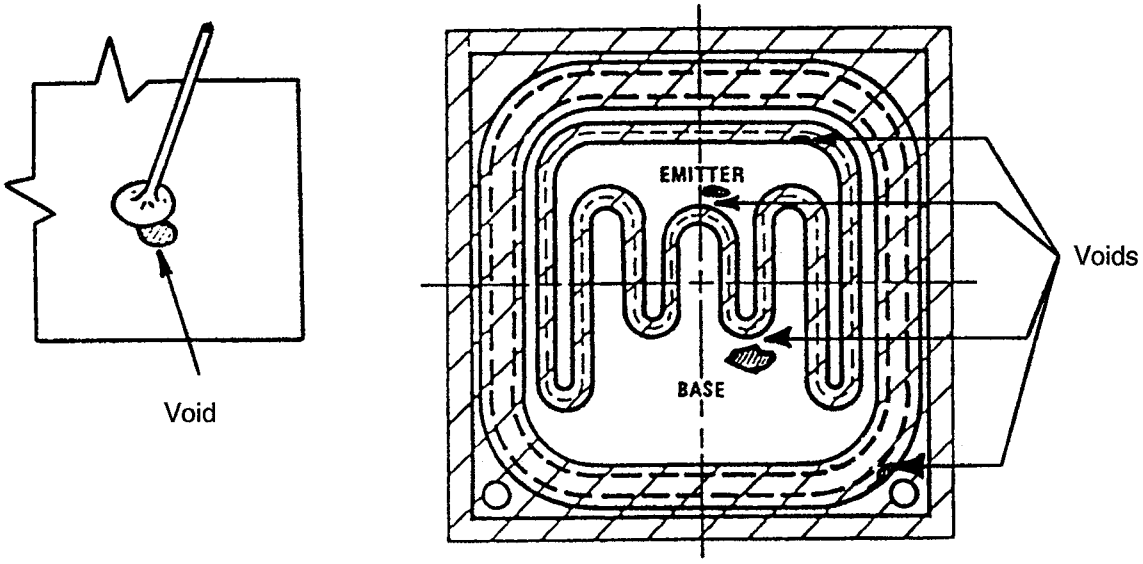
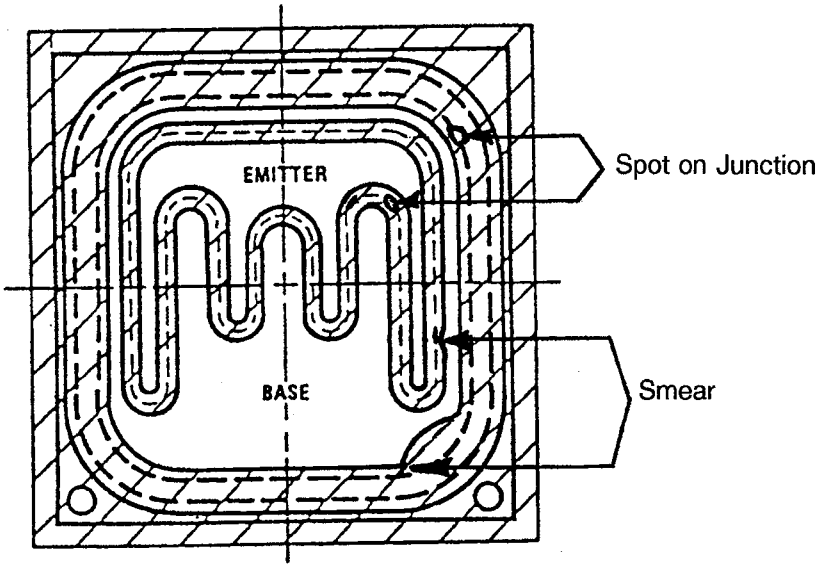


FIGURE IV - SPOTS AND SMEARS



3. DETAILED REQUIREMENTS

3.1 MAGNIFICATION

The magnification shall be as follows:-

	MINIMUM	MAXIMUM
Metallisation Defects	100	120
Oxide and Diffusion Defects	100	120
Scribing and Die Defects	100	120
Bonds and Internal Leads	30	50
Glassivation Defects	100	200
Package Condition	30	50

N.B.
For the purpose of clarification only, specific defects may be subjected to a scrutiny at increased magnification.

3.2 BIPOLAR TRANSISTORS, FET's AND DIODES (NOT GLASS ENCAPSULATED)

3.2.1 General

A unit shall be rejected if it exhibits one or more of the defects listed in any of the paragraphs detailed in Para. 3.2. Where applicable, drawings are included to provide additional explanatory material.

3.2.2 Mechanical Die Defects

3.2.2.1 General

Less than 2.5µm of passivation visible between active metallisation or between isolation/diffusion channel bond periphery and the edge of the die. Excluded from this criterion are metallisation and bonds associated with peripheral ground metallisation, metallised (inactive) scribe lines and bonding pads grounded to the die.

3.2.2.2 Chip-outs or Offset Scribe Lines/Breaks (see Figure V)

(a) Portions of the active area of another die attached or unattached.

(b) A chip-out in the active circuit area, or extending from the scribe line in the active area.

(c) A chip-out or offset scribe lines/breaks into the non-active circuit area. The minimum acceptable distance between any metallised area involved in the electrical operation of the device and edge of the fault shall be 5.0µm.

(d) On any edge of the die, a chip-out or series of chip-outs where length, or aggregate length is greater than 25% of the die edge.

(e) Any chip-out that extends to within 25µm of a junction.

(f) Chip-outs meeting the annular channel stopper, isolation or guard ring.

3.2.2.3 Cracks (see Figure VI)

(a) A crack in the active circuit area, or extending from the scribe line in the active area.

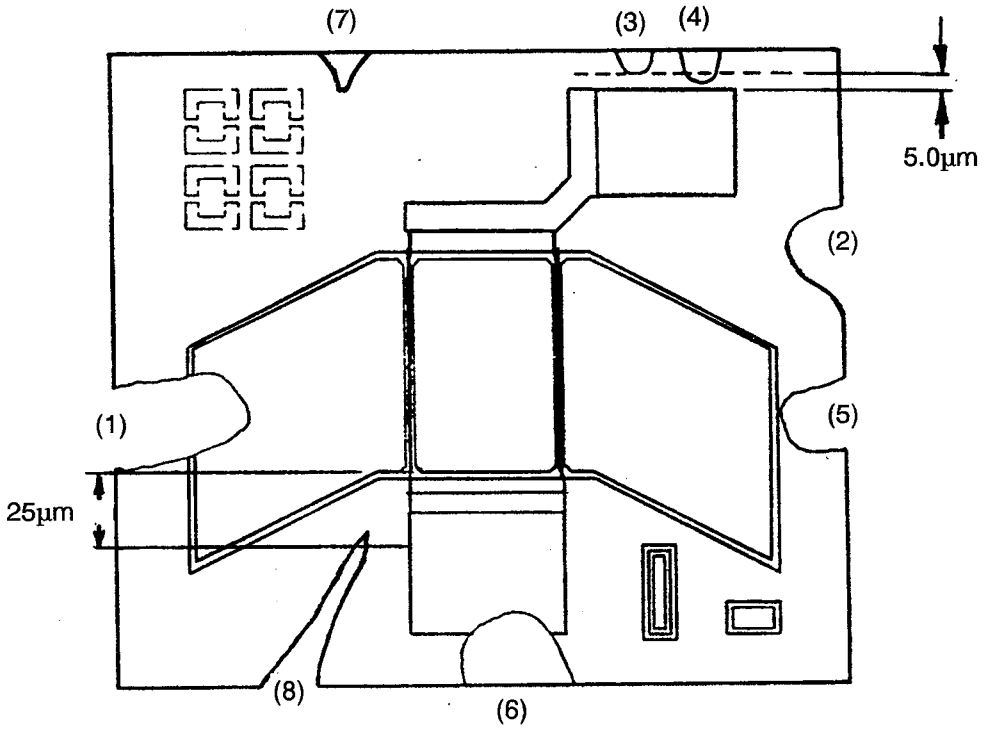
(b) a crack in the non-active circuit area which exceeds 25µm in length, measured from the inside edge of the scribe grid or die edge that points towards active metallisation or the circuit area.

(c) A crack in the non-active circuit area which exceeds 100µm in length or comes closer than 6.0µm to any active metallisation, bonding pad or other active portion of the die.

(d) Cracks meeting the annular channel stopper, isolation or guard ring.

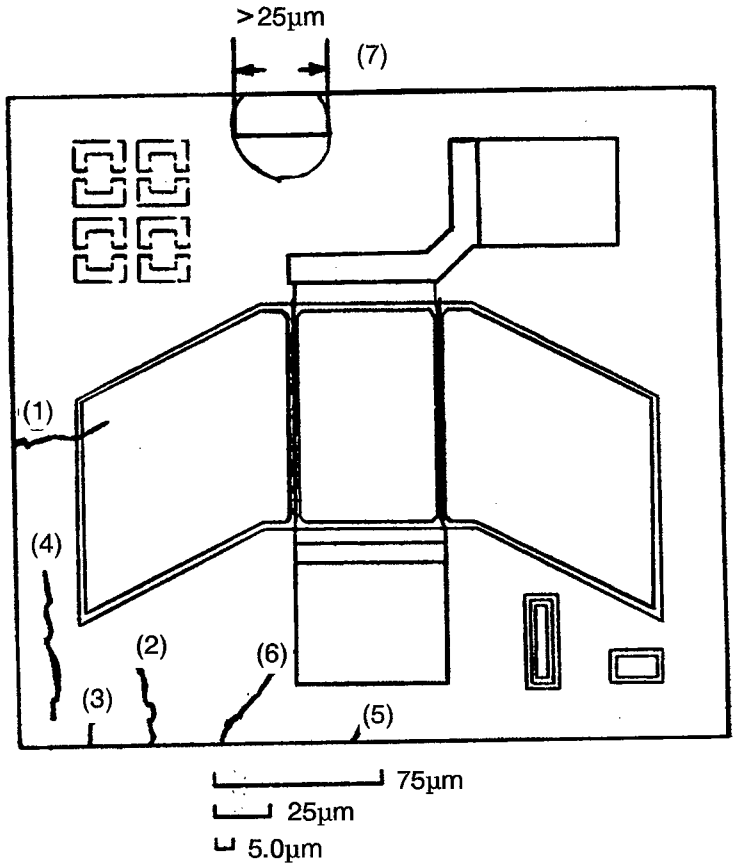
(e) Semicircular crack, i.e. undetached chip-out terminating at the die edge whose chord is equal or greater than 25µm.

FIGURE V - CHIP-OUTS OR OFFSET SCRIBE LINES/BREAKS (3.2.2.2)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.2.2(b)	Chip-out into active area
2	X		3.2.2.2(c)	Separation >5.0µm
3	X		3.2.2.2(c)	Separation ≥5.0µm
4		X	3.2.2.2(c)	Separation <5.0µm
5		X	3.2.2.2(c)	Separation <5.0µm
6		X	3.2.2.2(c)	Chip-out into non-active area but into metallisation
7	X		3.2.2.2(c)	Chip-out into non-active area
2 + 5		X	3.2.2.2(d)	Aggregate Length >25%
8		X	3.2.2.2(e)	Separation <25µm

FIGURE VI - CRACKS (3.2.2.3)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.2.3(a)	Crack in circuit area
2		X	3.2.2.3(b)	Crack in non-active circuit area pointing towards active circuit area >25µm
3	X		3.2.2.3(c)	Crack in non-active circuit area <100µm long
4		X	3.2.2.3(c)	Crack in non-active circuit area >100µm long
5	X		3.2.2.3(c)	Crack >6.0µm separation from metallisation
6		X	3.2.2.3(c)	Crack <6.0µm from metallisation involved in device operation
7		X	3.2.2.3(e)	Chord of undetached chip-out >25µm

3.2.3 Metallisation Defects

3.2.3.1 General (see Figure VII)

(a) Evidence of metallisation corrosion. Metallisation having any discoloured localised area shall be closely examined and shall be rejected unless it is demonstrated to be caused by a harmless defect.

(b) Evidence of metallisation lifting, peeling or blistering.

(c) Scratches in the metallisation which expose underlying material, leaving less than 75% of the original width undisturbed except as follows:

- Scratches that sever the metallisation of the innermost metallised guard ring;
- Scratches in devices having a lobed or fingerd configuration that reduce the width or length of the lobe or finger by more than 25%;
- Scratches in the bonding region and/or fillet area reducing the area of metallisation by more than 25%.

(d) Scratches in the metallisation which do not expose the underlying material, leaving less than 50% of the original width undisturbed.

(e) Voids in the metallisation which expose underlying material, leaving less than 75% of the original width undisturbed except as follows:

- Voids in the bonding region and/or fillet area reducing the area of metallisation by more than 25%;
- Voids that encompass or touch any bond;
- Voids that sever the metallisation of the innermost metallised guard ring;
- Voids in devices having a lobed or fingered configuration that reduce the width or length of the lobe or finger by more than 25%.

(f) Contact window that has less than 75% of its area covered by continuous metallisation.

(g) Metallisation path not intended to cover a contact window and which is separated from the window by less than 2.5µm, or half of the design separation (whichever is the greater).

(h) Metallisation overlaps departing from the design.

(i) The minimum acceptable separation between two metallisation areas shall be 50% of the design width or 25µm, whichever is the smaller, and shall not be less than 2.5µm minimum separation at any point, whether caused by smears, photolithographic defects or other defects. This excludes gate/source, gate/gate and gate/drain in a FET.

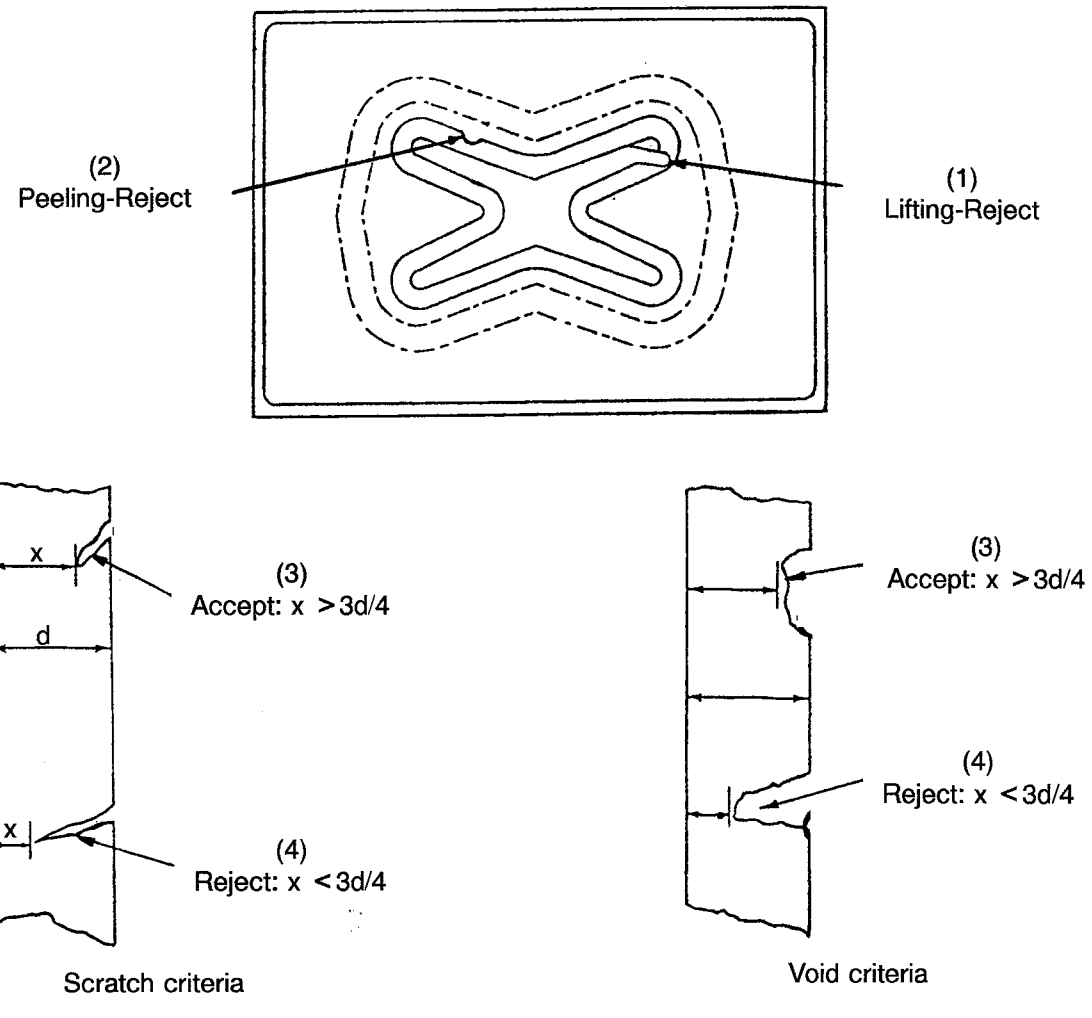
(j) Aluminium whisker longer than half of the shortest distance between two unglassivated areas.

(k) Aluminium whisker longer than half of the shortest distance between two metallised areas on unglassivated devices.

(l) Aluminium whisker longer than half a wire diameter.

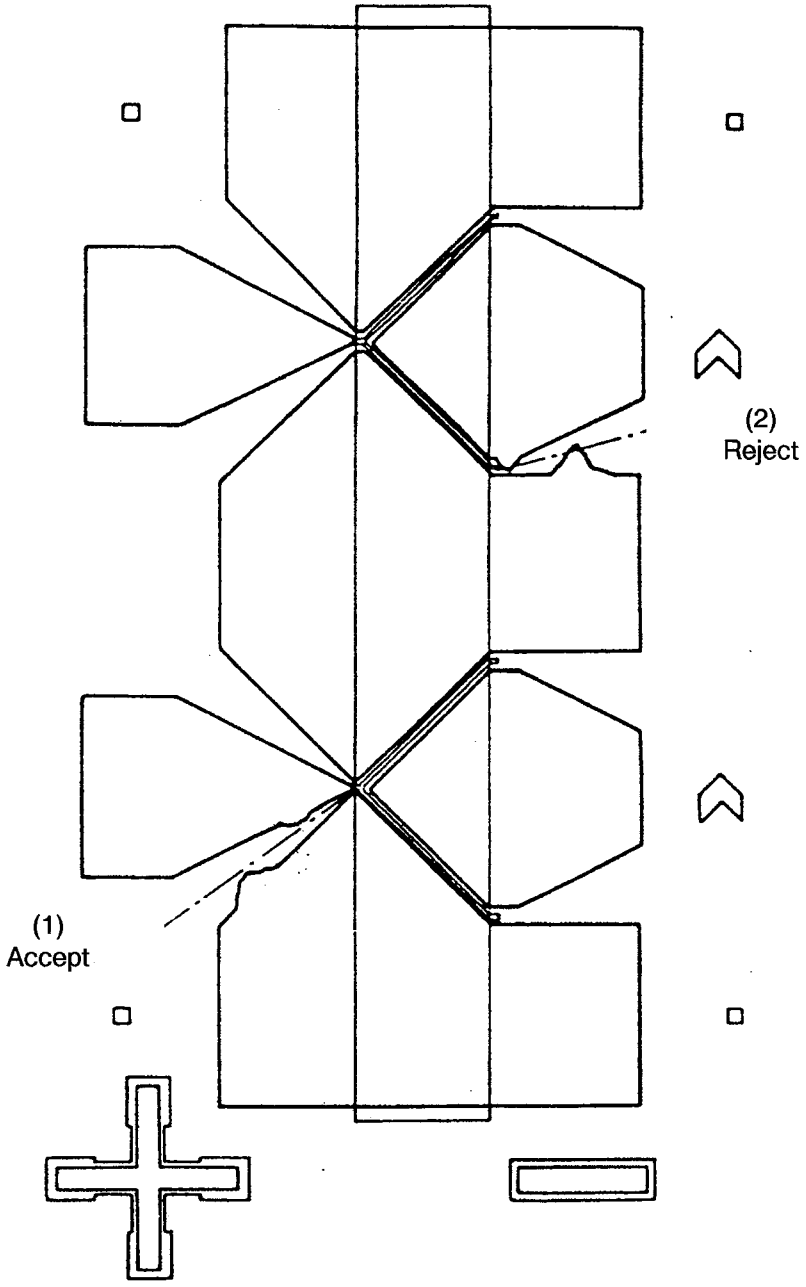
N.B.
Additional defects which are specific to FET's are given in Para. 3.2.3.2.

FIGURE VII - GENERAL METALLISATION DEFECTS (3.2.3.1)



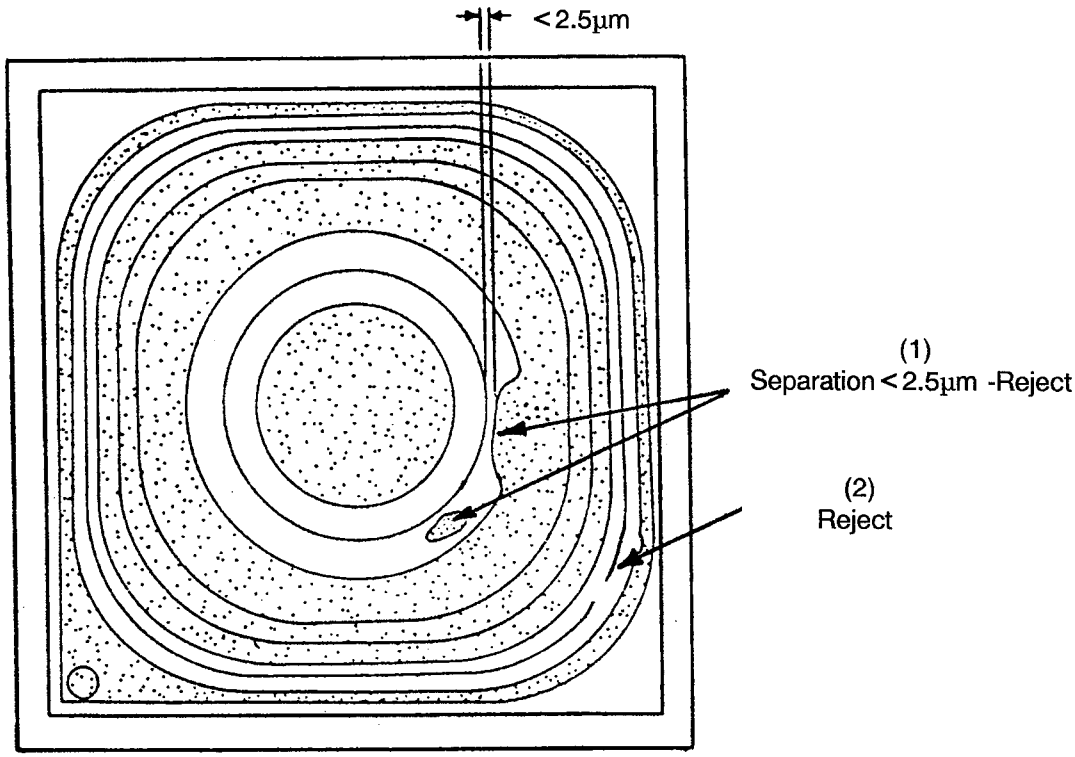
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.3.1(b)	Metallisation lifting
2		X	3.2.3.1(b)	Metallisation peeling
3	X		3.2.3.1(d)	x >3d/4
4		X	3.2.3.1(d)	x <3d/4
5		X	3.2.3.1(g)	Separation <2.5µm

FIGURE VII - GENERAL METALLISATION DEFECTS (3.2.3.1) (CONTINUED)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.3.1(k)	Separation >50% design
2		X	3.2.3.1(k)	Separation <50% design

FIGURE VII - GENERAL METALLISATION DEFECTS (3.2.3.1) (CONTINUED)



FAULT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X	3.2.3.1(i)	Separation <2.5µm
2	X	3.2.3.1(e)	Innermost guard ring severed

3.2.3.2 FET's (see Figure VIII)

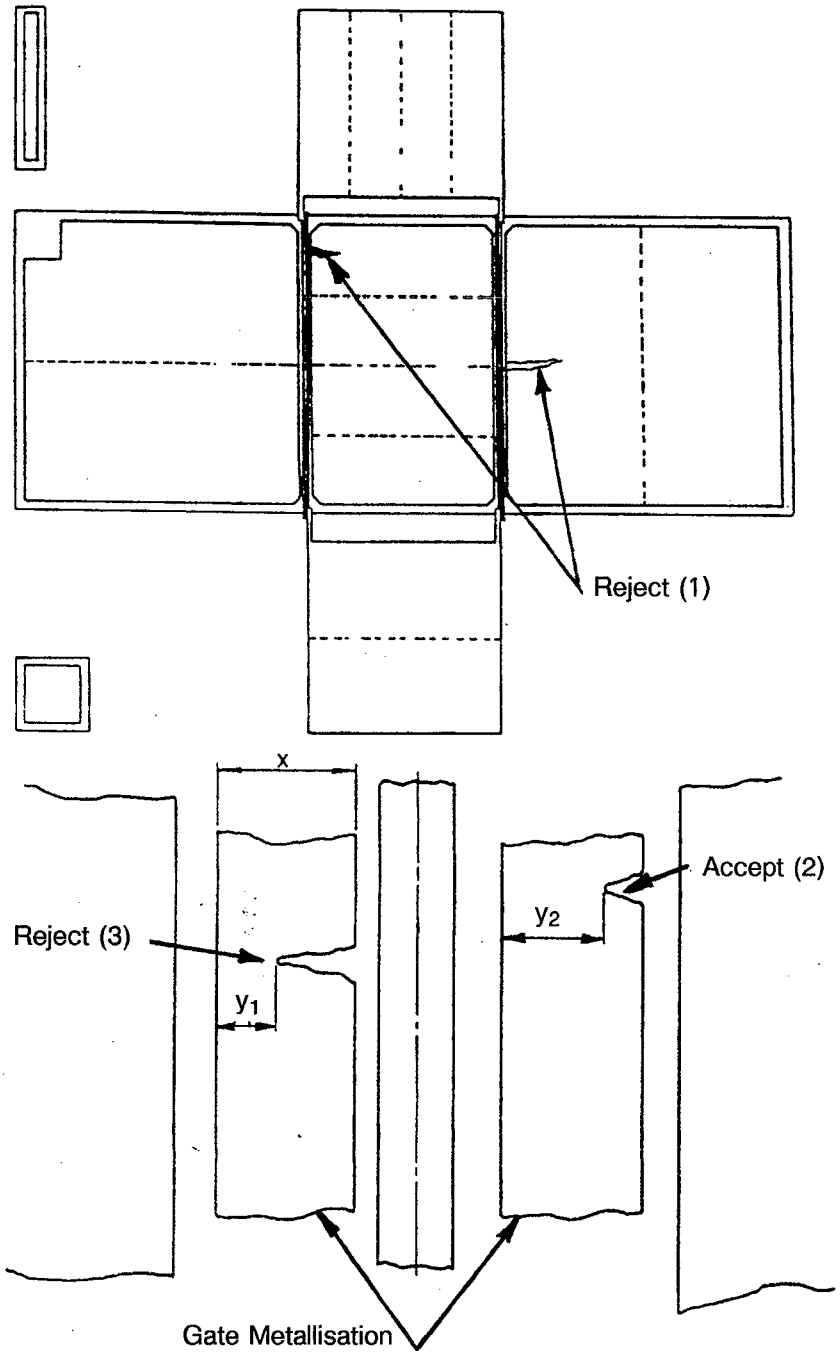
(a) Scratches in the metallisation which start at the gate channel edge/scratches on the gate metallisation, not including the pad area.

(b) Necking of the gate metallisation. The minimum acceptable width of remaining metallisation shall be 75%.

(c) The localised metallisation defects which reduce gate/source, gate/gate and gate/drain separations shall not exceed 25% of the actual design separation.

(d) Excess metal on the gate shall not increase the gate length by more than 25%.

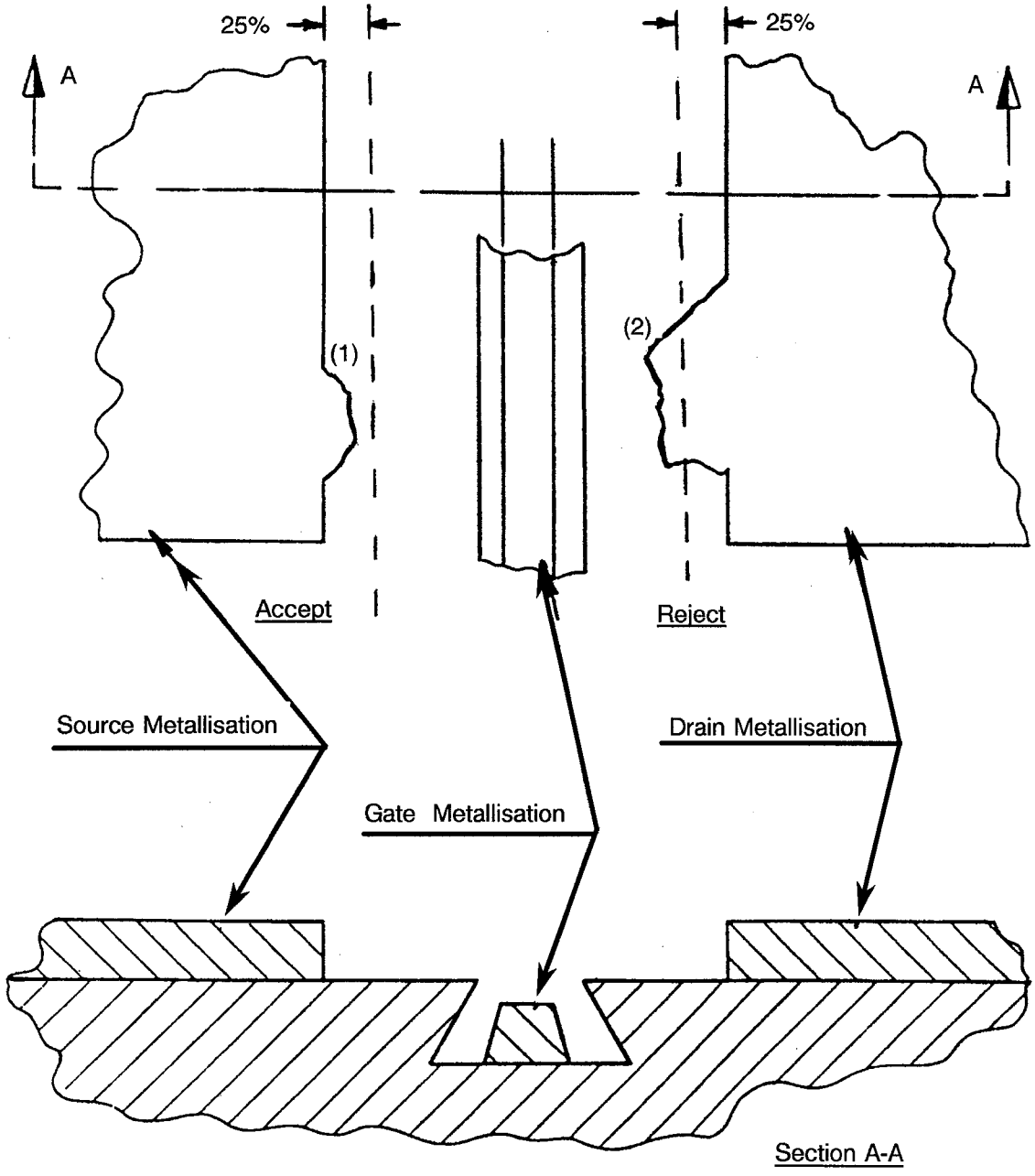
FIGURE VIII - METALLISATION DEFECTS (FET's) (3.2.3.2)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.3.2(a)	Scratch starts at Gate Channel Edge
2	X		3.2.3.2(b)	$\frac{y_2}{x} > 0.75$
3		X	3.2.3.2(b)	$\frac{y_1}{x} < 0.75$

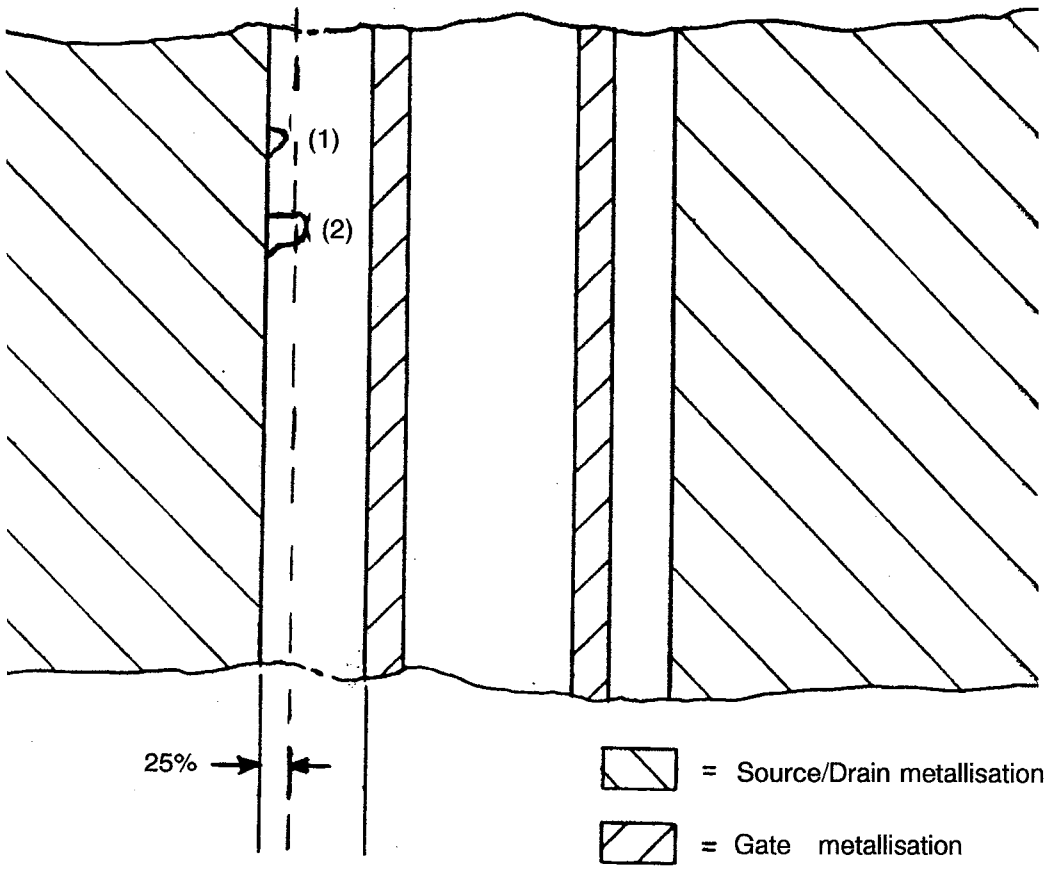
FIGURE VIII - METALLISATION DEFECTS (FET's) (3.2.3.2) (CONTINUED)

Ideal Gate Alignment



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.3.2(c)	Localised separation >25%
2		X	3.2.3.1(c)	Localised separation <25%

FIGURE VIII - METALLISATION DEFECTS (FET's) (3.2.3.2) (CONTINUED)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.3.2(c)	≤25% reduction in separation
2		X	3.2.3.2(c)	>25% reduction in separation

3.2.4 Oxide and Diffusion Faults (see Figure IX)

(a) A diffusion area that appears to be discontinuous.

(b) A diffusion fault that allows bridging between any two diffused areas, any two metallisation areas or any combination thereof not intended by design.

(c) A contact window in a diffused area which unintentionally extends across a junction into an undiffused area or another diffused area.

(d) An oxide fault, including pinholes, that exposes bare semiconductor material and allows bridging between any two diffused areas or a combination thereof not intended by design.

(e) Pinholes on any junction or active circuit area.

(f) Bare semiconductor material areas not covered by oxide and exposing or touching any metallisation.

(g) An absence of oxide, visible at the edge and continuing under the metallisation, such as to cause an apparent short between the metal and the underlying material. (Double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the bare semiconductor material).

(h) An active junction area which is not covered by oxide (except by design) or exhibiting oxide cracking.

(i) More than two fringe undercuttings present on any junction.

(j) Areas of undercutting which exhibit other than normal oxide colour differentiation.

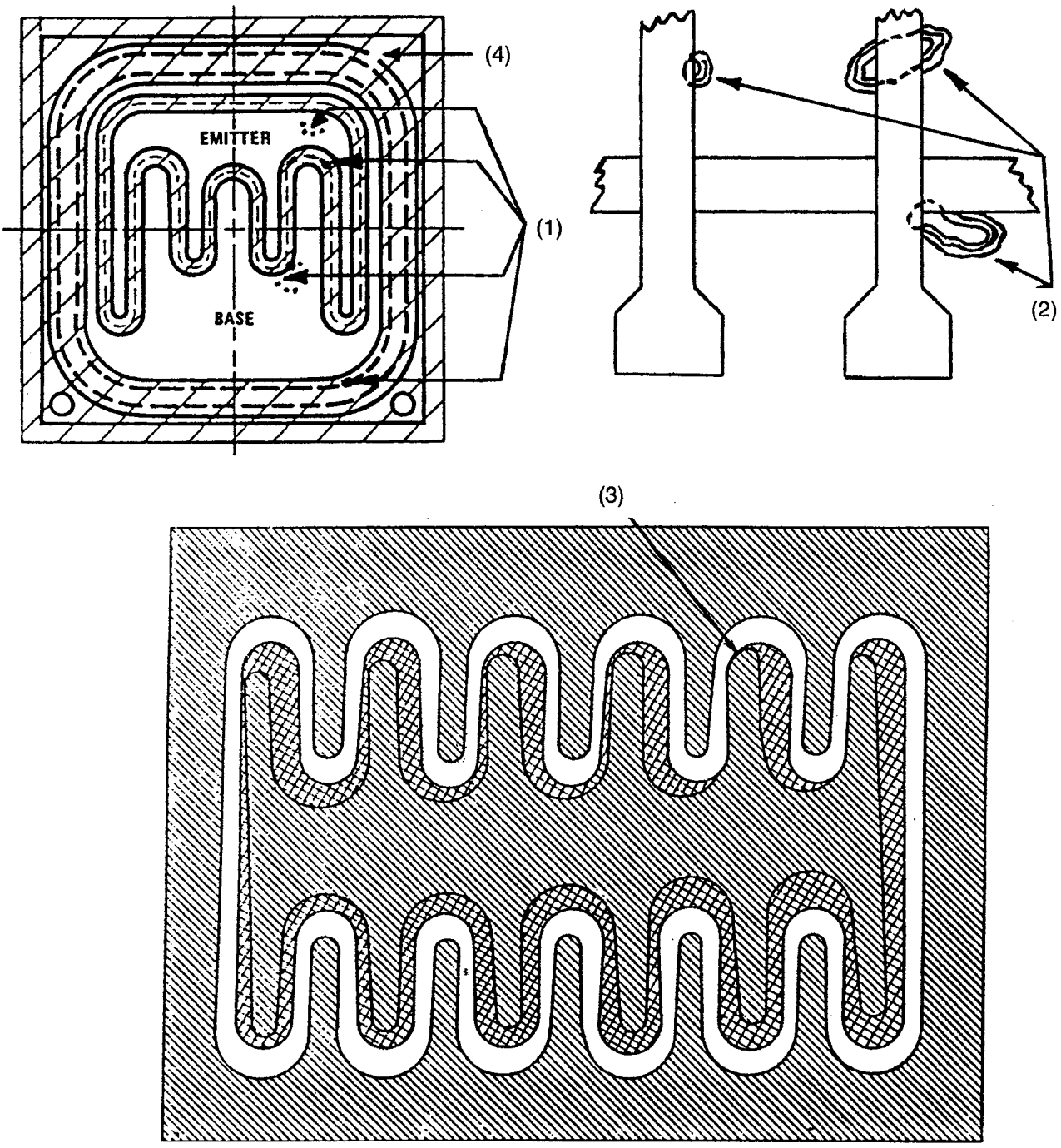
(k) A depression or irregularity which is not part of the design pattern and is completely covered by metallisation.

(l) Any misalignment such that a continuous oxide colour cannot be seen.

(m) A break in continuity of the Annular Stopper, Isolation or Guard Ring.

(n) Evidence of over-etching.

FIGURE IX- OXIDE AND DIFFUSION FAULTS (3.2.4)



FAULT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X	3.2.4(e)	Pinholes on Junction/Active Circuit Area
2	X	3.2.4(g)	Absence of Oxide
3	X	3.2.4(l)	Misalignment causing Non-Continuous Oxide Colour
4	X	3.2.4(m)	Continuity Break in Annular Stopper

3.2.5 Die Mounting Defects (see Figure X and Note 1)

(a) Portions of the active area of another die attached or unattached.

(b) Die mounted such that it is not flat against the bottom of the package within 10°.

(c) Die mounted such that it is not properly orientated according to the drawing.

(d) Die geometry or dimensions not in accordance with the applicable assembly drawing of the device.

(e) Die attach material at the edge of the die exceeding the height of the die, except for unprotected MESA devices where the die attached material shall not exceed the height of the lower etch limit.

(f) Pinnacles in the flow area higher than one half of the height of the die.

(g) Die attach material anywhere outside the main attachment area or on the surface of the die.

(h) Slag or crumbly die attache material visible around the die or on the header.

(i) Voids in the fillet greater than 20% on any side of the die.

(j) Minimum die mounting material around the visible perimeter of the die shall not be less than 75%.

(k) Balling of the die mounting material which does not exhibit a fillet when viewed from above.

(l) Unmelted preform.

(m) Preforms that overlap onto any insulation material.

(n) Preforms that are not firmly attached to the package.

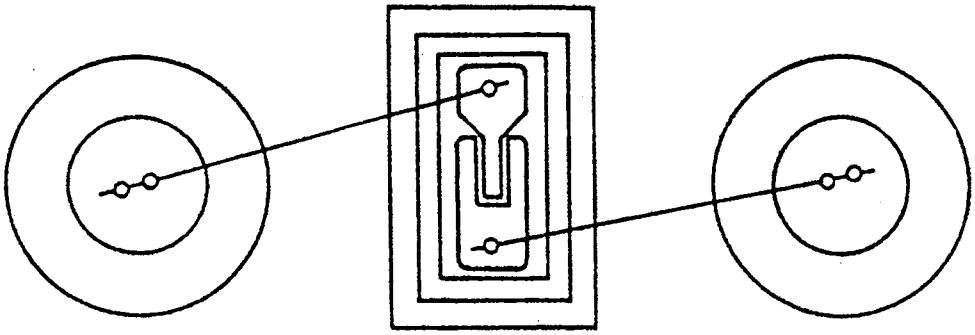
(o) Foreign material or rough surface holding the die off the header.

(p) Die bonded over post glass.

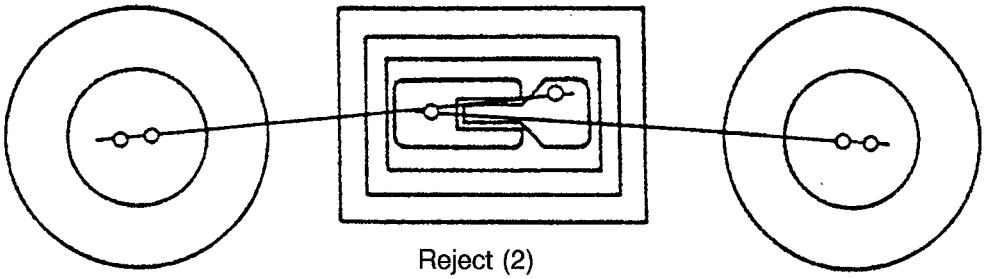
NOTES

1. For die mounting defects, the angle may be increased above the 30° range set in Para. 2.1 up to the maximum compatible with safe handling.

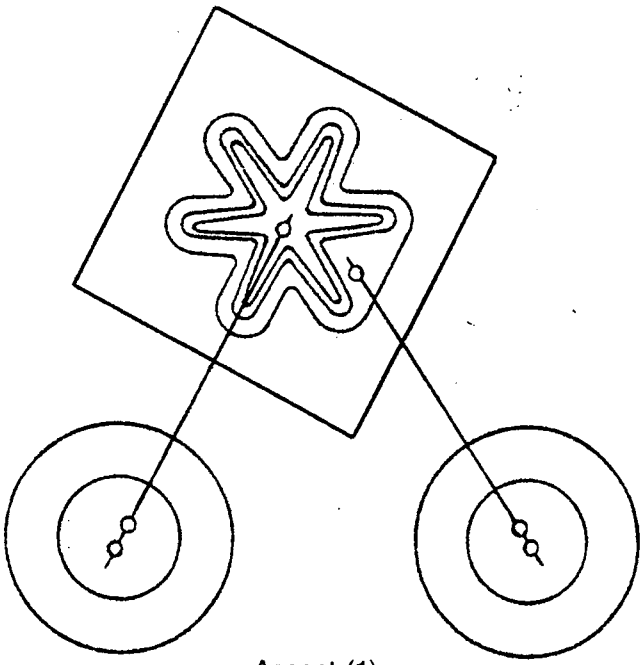
FIGURE X- DIE MOUNTING DEFECTS (3.2.5)



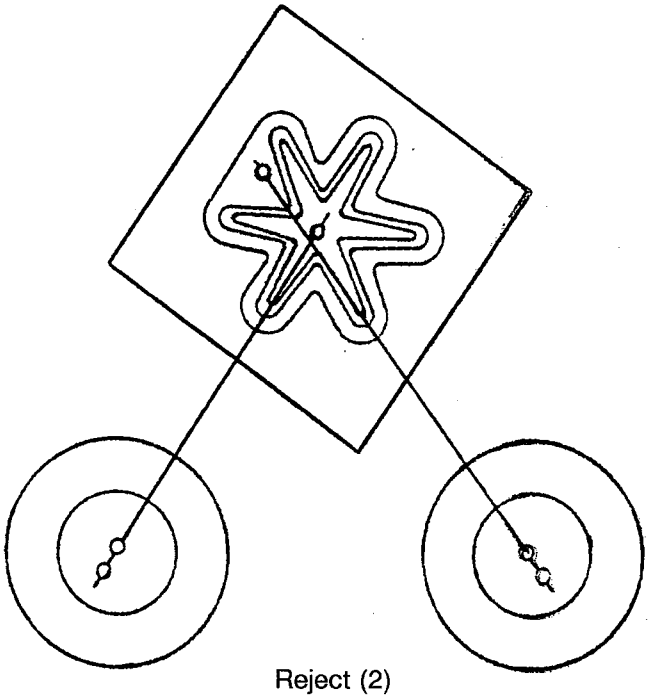
Accept (1)



Reject (2)



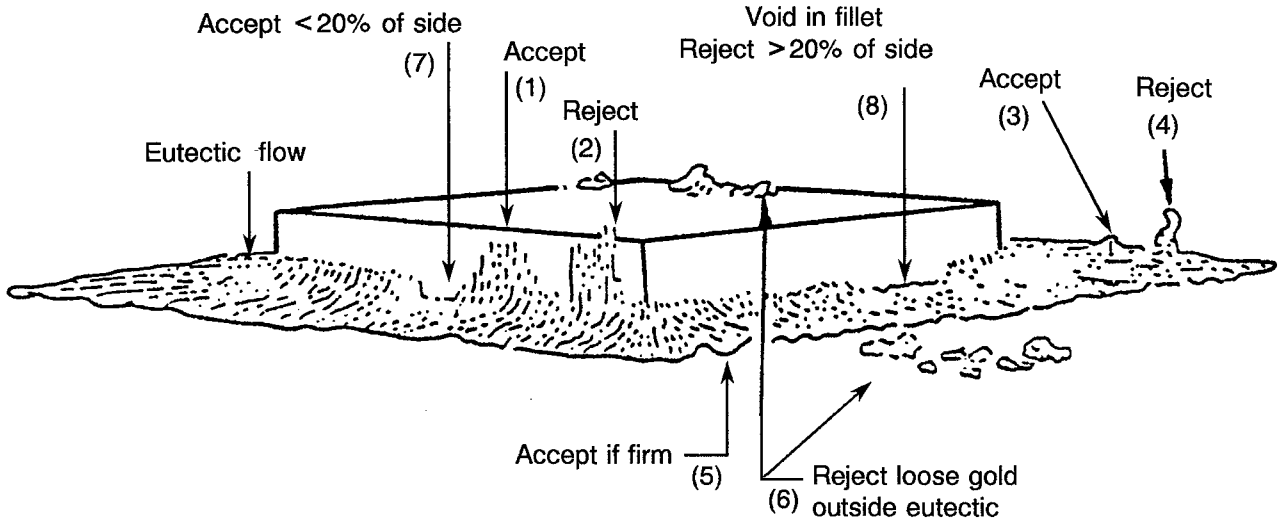
Accept (1)

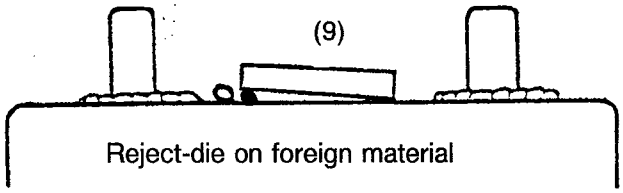


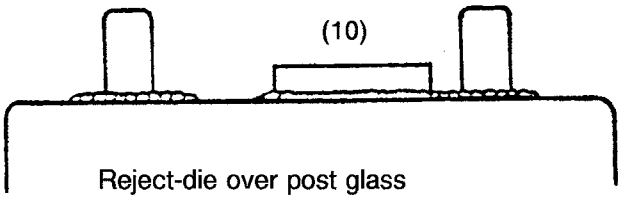
Reject (2)

FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.5(c)	Correct Orientation
2		X	3.2.5(c)	Incorrect Orientation - Wires Crossing

FIGURE X- DIE MOUNTING DEFECTS (3.2.5) (CONTINUED)







FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.5(e)	Not exceeding die height
2		X	3.2.5(e)	Exceeding die height
3	X		3.2.5(f)	<1/2 die height
4		X	3.2.5(f)	>1/2 die height
5	X		3.2.5(g)	Accept if firm
6		X	3.2.5(g)	Outside eutectic
7	X		3.2.5(i)	<20% of side
8		X	3.2.5(i)	>20% of side
9		X	3.2.5(o)	Die on foreign material
10		X	3.2.5(p)	Die over post glass

3.2.6 Header Defects (see Figure XI)

(a) Any glass, die or other material greater than 25µm in its greater dimension which adheres to the flange or the side of the header; or of lesser dimension but which would impair sealing.

(b) A solder preform on the flange which still resembles a preform.

(c) Header posts bent more than 10°.

(d) Metal shavings on the flange or side of the header longer than the width of the flange.

(e) Bent or deformed flanges.

(f) Metallic particle on the top of the header which is greater in any dimension than the minimum distance between a junction line and the metallisation of the particular device, and is not firmly attached to the header. There shall not be a prevalence of smaller particles.

(g) Non-metallic substance of similar dimension on top of the header or the glass seal, or a prevalence of smaller particles.

(h) Cracked or chipped glass seals. Meniscus chip-outs must not exceed 0.2mm in any dimension.

(i) Non-uniformity of finish of lead or pillar, particularly at the glass seal.

(j) Nicks or bulges in the wire diameter outside stated lead tolerances.

(k) Bubbles, or an area of adjacent or interconnecting bubbles in the seal area larger than 12.5% of the seal area or which are more than one half of the distance between the pin and body or pin and pin.

(l) Foreign particles enclosed in the glass seal.

(m) Eccentricity of lead not passing through the centre of glass to metal seal greater than 10% of the seal diameter.

(n) Lead tilted by more than 5° from normal to seal body.

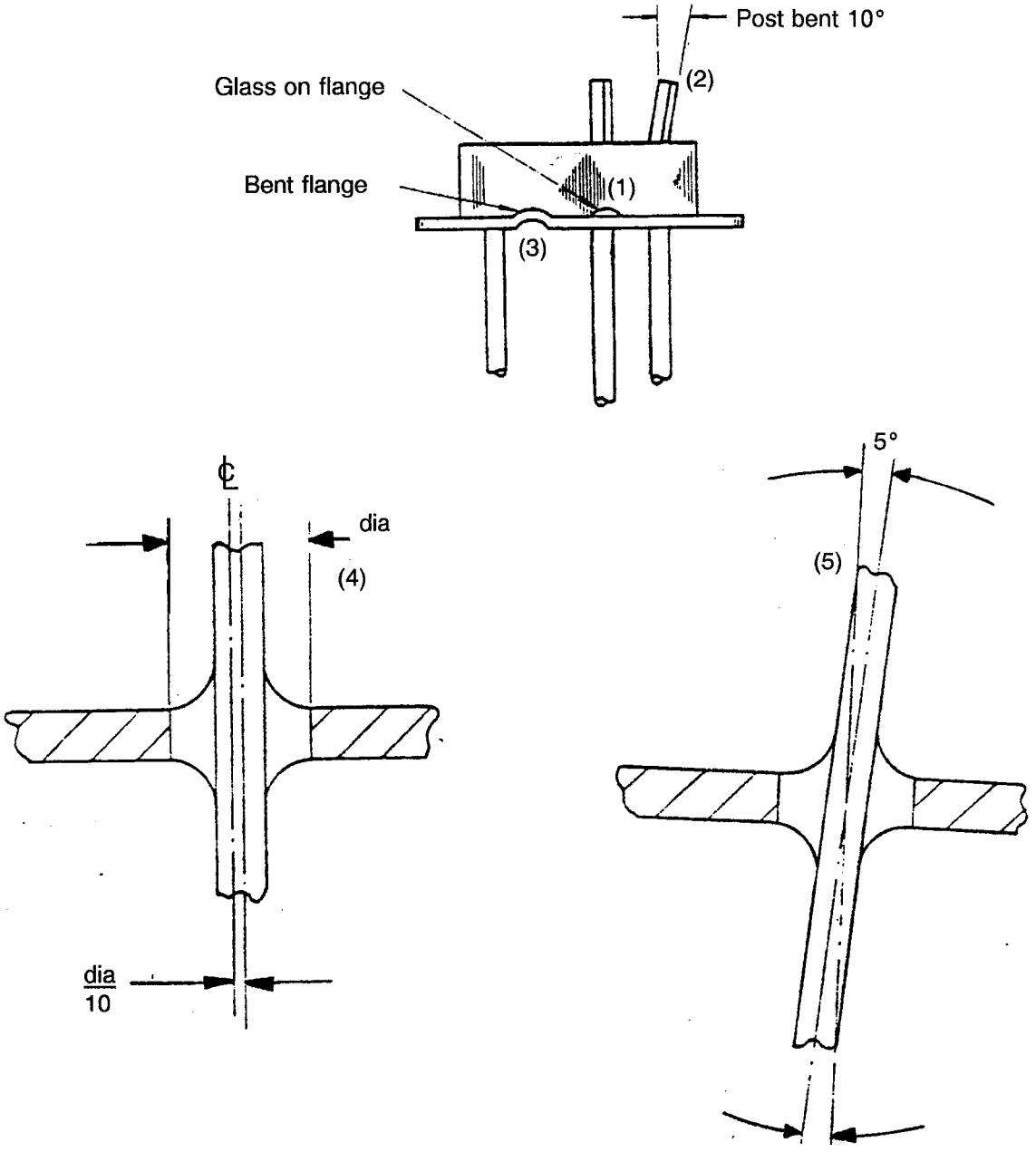
(o) Blistering, flaking or cracking of gold or nickel plating.

(p) Die or part of a die on the flange or on the side of the header.

(q) Grease, varnish, ink or similar stain on the flange or the side of the header.

(r) Plating or die attach material overlapping the seals.

FIGURE XI- HEADER DEFECTS (3.2.6)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.6(a)	Glass >25μm in dimension
2	X		3.2.6(c)	Post bent ≤10%
3		X	3.2.6(e)	Bent Flange
4	X		3.2.6(m)	Eccentricity ≤10%
5	X		3.2.6(n)	Tilt ≤5°

3.2.7 Wire Bonding

3.2.7.1 General

Wire bonding operations shall be carried out such that when "up-bonding" (bonding from the die up to the post) or "down-bonding" (bonding from the die down to the post), the wire is carried from the bond in a smooth trajectory without mechanical stress. In particular, care should be taken to avoid situations where the tool leaves the made bond vertically (or horizontally) and then resets the wire to a new angle resulting in a crack at the wire-bond "heel".

NOTES

1. Extra lead wire anywhere in the package as a result of a bond-off shall be cause for rejection.

3.2.7.2 Deformed Wire (see Figure XII)

(a) Wire twisted more than 360° from pad bond to pillar bond.

(b) Any nicks, crimps, twisting, scratching, scoring or other deformity which reduces the wire diameter by more than 25%.

(c) Any wire exhibiting a sharp kink with an interior angle of 90° or less or twisted to the extent that stress marks show.

3.2.7.3 Bowed Wire (see Figure XIII)

(a) Wire less than 125µm diameter bowed more than 7 wire diameters.

(b) Wire greater than 125µm diameter bowed more than 3 wire diameters.

3.2.7.4 Up-Bonding (see Figure XIV)

(a) Wire not travelling in a smooth upward arc from the pad bond to the edge of the die and clearing the edge by 75µm.

(b) Wire rising more than 500µm above the top of the pillar or the top of the die (whichever is the highest).

(c) Wire sagging below a line parallel to the top of the header and 75µm above the top of the die.

NOTES

1. For "Metallic TO254/7 or similar type" header, wire is allowed to travel in a "S" shape within one plane without any visible stress.

3.2.7.5 Down-Bonding (see Figure XV)

(a) Wire not travelling in a smooth arc from the bond to the edge of the die and clearing the edge by 25µm for an upward arc, 75µm for a downward arc;

Wire sagging below a line parallel to the top of the header and 75µm above the top of the header and 75µm above the top of the die.

(b) For ultrasonic bonding

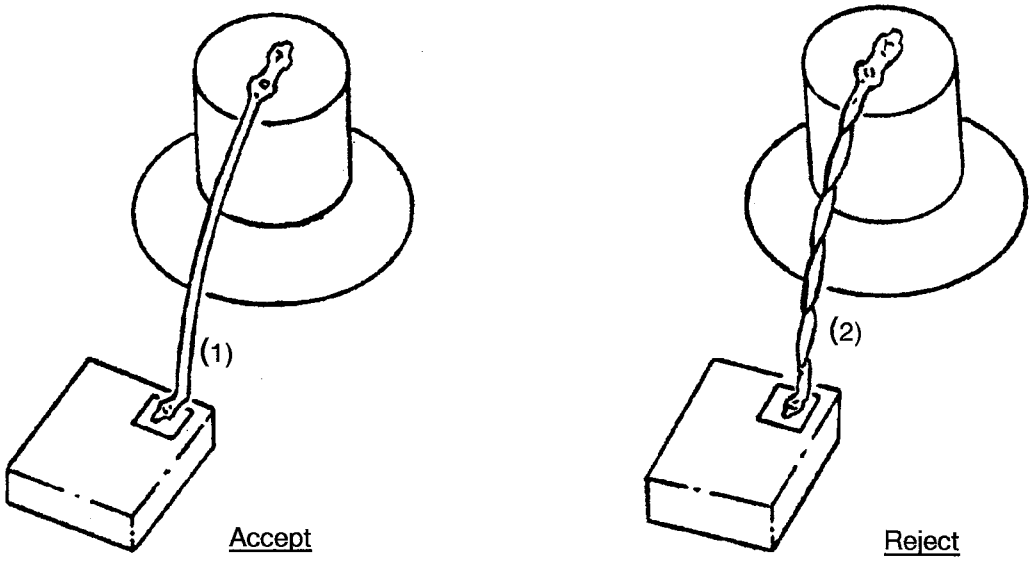
Wire equal to or less than 75µm diameter, rising more than 250µm or 7 wire diameters, whichever is the less, above the top of the die;

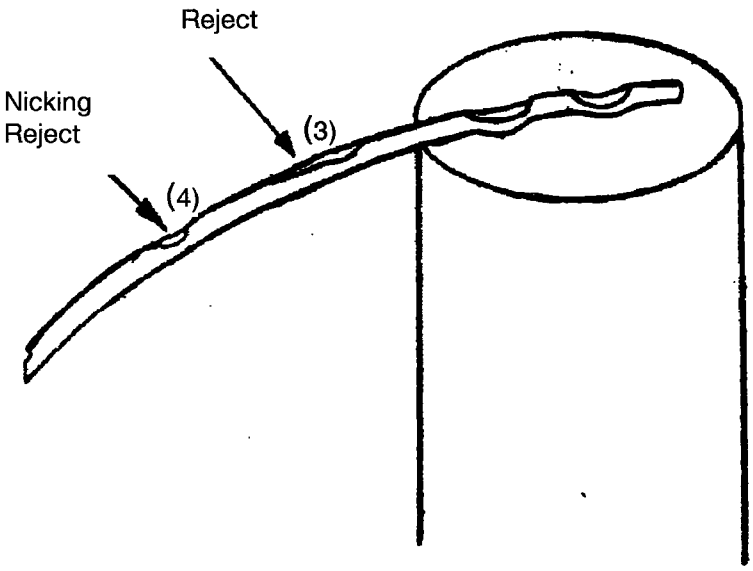
Wire greater than 75µm diameter, rising more than 3 wire diameters above the top of the die.

(c) For gold ball bonding

Gold wire rising more than 10 wire diameters above the top of the die.

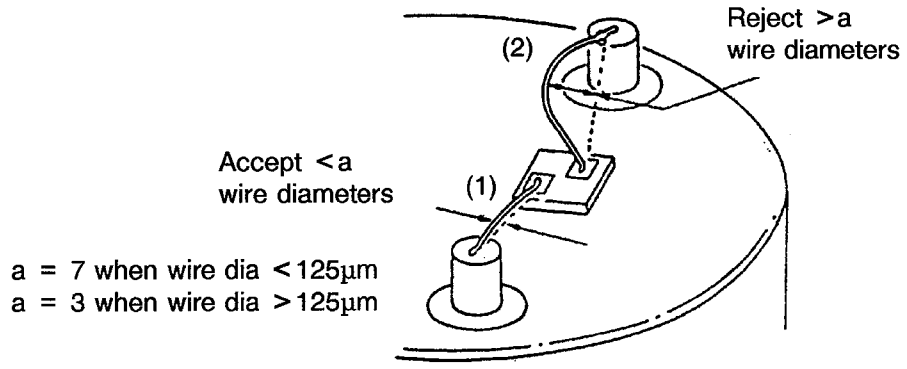
FIGURE XII - DEFORMED WIRE (3.2.7.2)





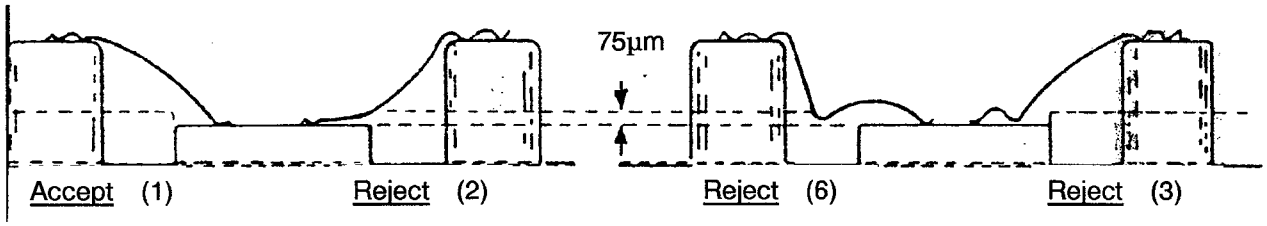
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.7.2(a)	No Twist
2		X	3.2.7.2(a)	360° Twist
3		X	3.2.7.2(b)	Scratch reduces diameter >25%
4		X	3.2.7.2(b)	Nick reduces diameter >25%
5	X		3.2.7.2(c)	Kink interior angle >90°

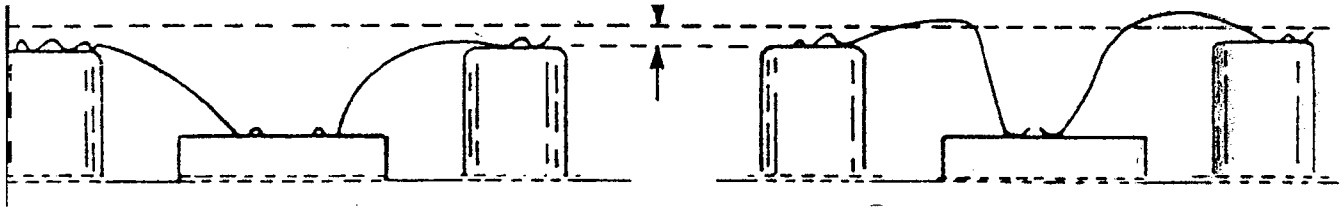
FIGURE XIII - BOWED WIRE (3.2.7.3)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.7.3(a,b)	a< 7 or 3 wire diameters
2		X	3.2.7.3(a,b)	a> 7 or 3 wire diameters

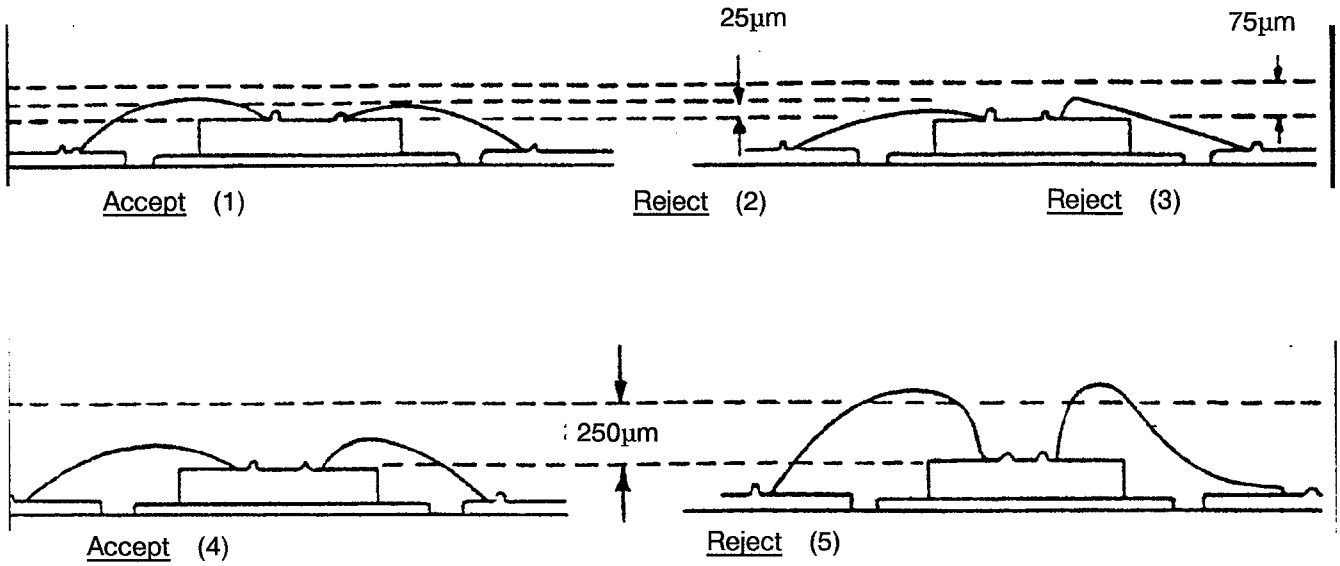
FIGURE XIV - UP-BONDING (3.2.7.4)

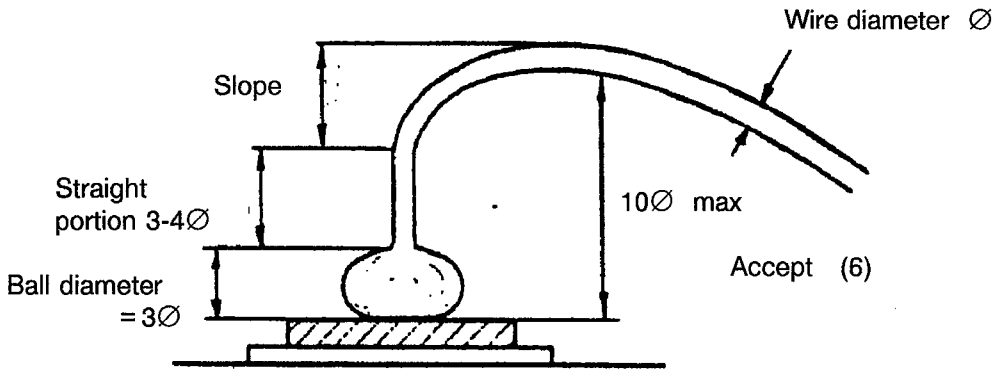




FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.7.4(a)	Proper arc and clearance
2		X	3.2.7.4(a)	Clearance <75µm
3		X	3.2.7.4(a)	Not rising in upward arc
4	X		3.2.7.4(b)	Rises <500µm above the pillar
5		X	3.2.7.4(b)	Rises >500µm above the pillar
6		X	3.2.7.4(c)	Sags below 75µm line

FIGURE XV - DOWN-BONDING (3.2.7.5)





FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.7.5(a)	Proper arc and clearance
2		X	3.2.7.5(a)	Clearance <25µm in upward arc
3		X	3.2.7.5(a)	Clearance <75µm in downward arc
4	X		3.2.7.5(b)	Proper arc and clearance
5		X	3.2.7.5(b)	>250µm above top of die
6	X		3.2.7.5(c)	<10 wire diameters above top of die

3.2.8 Wire and Bond Defects

3.2.8.1 General (see Figure XVI)

(a) Black or purple plague or other corrosion around the bond perimeter or on the metallisation.

(b) Bonds on the package post which are not completely within the boundaries of the package post.

(c) Missing or broken bonds/wires.

(d) Tearing at the junction of the wire and the bond. This criteria does not apply to tool marks without any tearing.

(e) Wire or wires not in accordance with the device bonding diagram.

(f) A bond placed on top of an existing bond.

(g) Any evidence of repair of metallisation by bridging with a bond or the addition of a bonding wire or ribbon.

(h) Bond or wire bond tails that extend over and make contact with any metallisation not covered by glassivation other than bonding pad metallisation.

(i) For bonds on the die bonding pad, the minimum percentage of bond within the unglassivated bonding pad area shall be:

- Where the bond area is smaller than the bonding wire, 50%. (However the bond must cover the entire area of the bond pad).
- Where the bond pad is larger than the bond, 75%.

(j) Lifted bonds.

(k) Excessive loops, bows or sags in any wires such that they could short to another wire, to another pad or any other package post, to the die or could touch any portion of the package.

(l) Bond wires fragments or bond pad metal detached from the bond or pad.

(m) Bond wires which do not clear the die edge by at least 25µm.

(n) Bonds placed such that the wire exiting from the bond crosses over (when viewed from above) or is less than 2 wire diameters or 150µm whichever is the less from another wire, unglassivated operating metallisation, unpassivated die area, or any portion of the package (including the plane of the lid), with the exception of common connections and pigtails. Within a 150µm spherical radial distance from the perimeter of the bond on the die surface the separation may be 25µm.

(o) Periphery of a bond overlapping an adjacent junction.

(p) Wire bond tails exceeding 2 wire diameters in length at the pad or half a post diameter at the post, or extra pigtails or no pigtail at the pad.

(q) Bonds located where any portion of the bond is placed on an area containing die preform mounting material.

(r) For aluminium wires greater than 50µm diameter, the bond width shall not be less than the diameter of the wire.

3.2.8.2 Gold Ball Bonds (see Figure XVII)

(a) Less than two thirds of the ball in contact with the pad.

(b) Wire terminating on the perimeter of the ball when viewed from above.

(c) Wire of which the diameter at the ball is reduced by more than 25%.

(d) Ball diameter, viewed from above, less than twice the wire diameter or more than four times the wire diameter.

(e) Ball height, viewed from the side, less than one wire diameter or more than twice the wire diameter.

(f) Wire centre exit not within the boundaries of the bonding pad.

(g) Wire not within 10° of the perpendicular to the surface of the chip for a distance greater than 12.5µm before bending towards the package post or other terminating point.

3.2.8.3 Ultrasonic and Thermocompression Crescent/Wedge Bonds (see Figure XVIII)

(a) Pad bond torn in the bond area or behind the bond.

(b) Nicks in the side of the bond or holes in the centre of the bond.

(c) Needle impression area lifted more than 25%.

(d) If the bond is smaller than the pad area, at least 75% of the needle impression of the pad bond must be bonded to the metallisation.

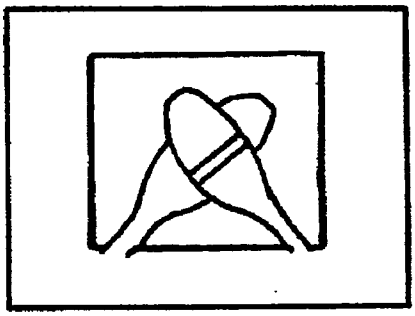
(e) If the bond is larger than the pad area, less than 50% of the needle impression of the pad bond appearing on the area of the pad.

(f) Crescent bond width less than 1.2 or more than 5 wire diameters or length less than 0.5 or more than 3 wire diameters.

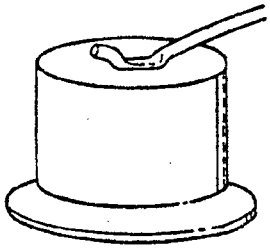
(g) Crescent bonds where the bond impression does not cover the entire width of the wire.

(h) Wedge bond width less than 1.2 or more than 3 wire diameters or length less than 1.5 or more than 5 wire diameters.

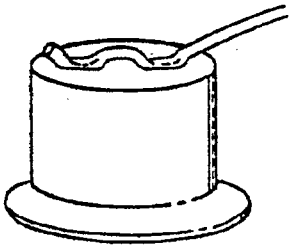
FIGURE XVI - GENERAL WIRE AND BOND DEFECTS (3.2.8.1)



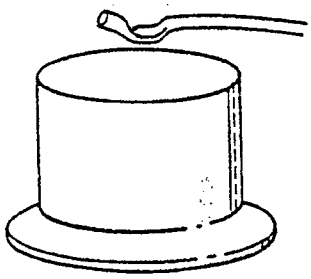
Reject (1)



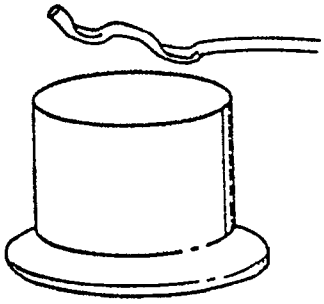
Accept (2)



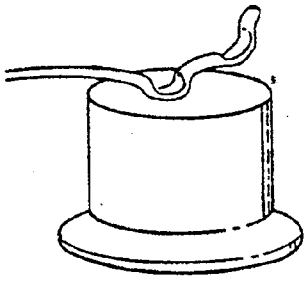
Accept (2)



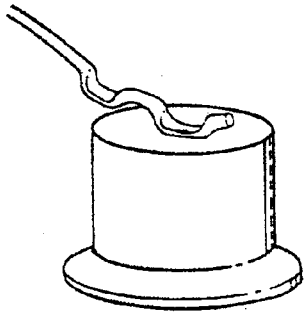
Reject (3)



Reject (3)



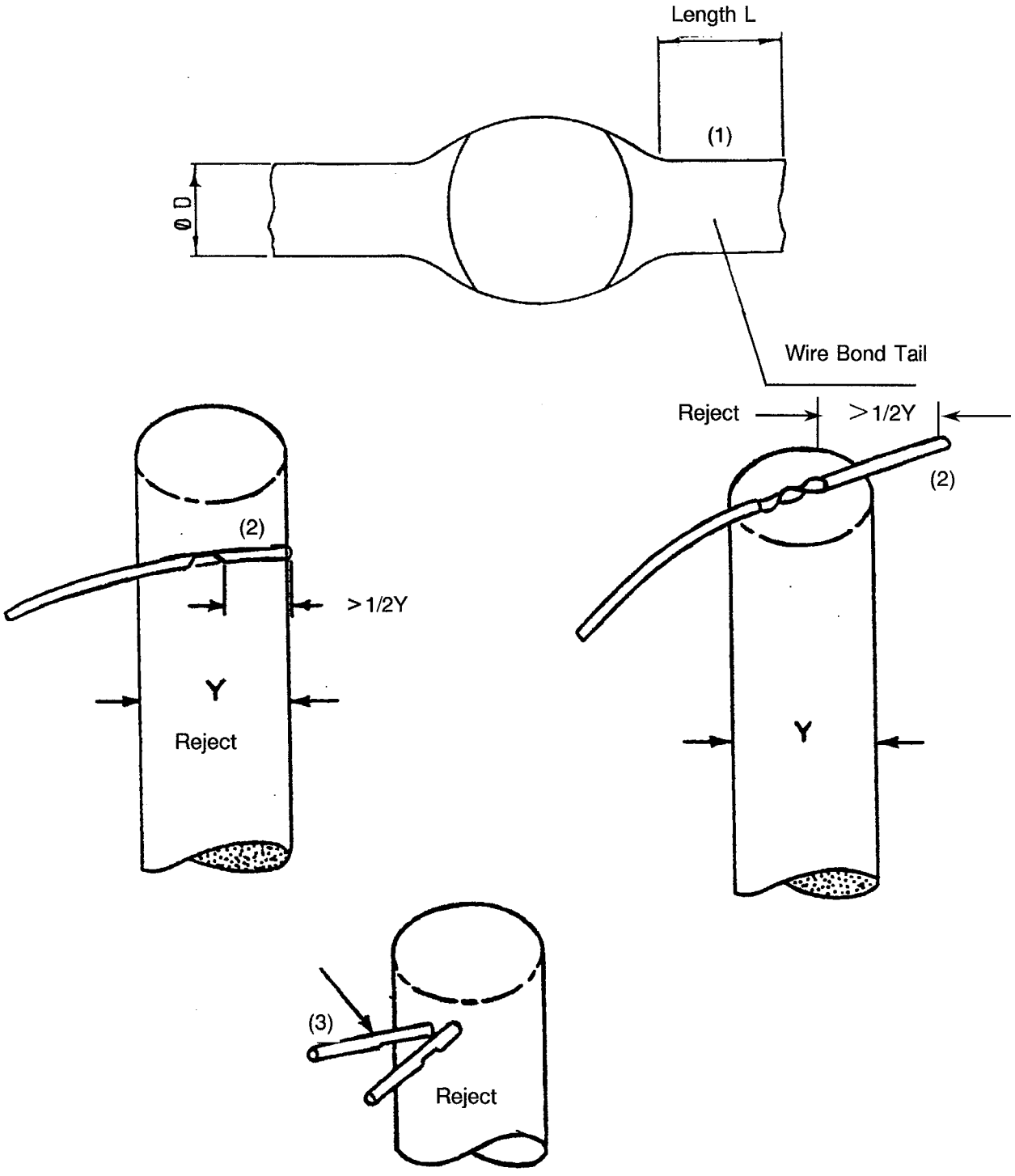
Reject (3)



Reject (3)

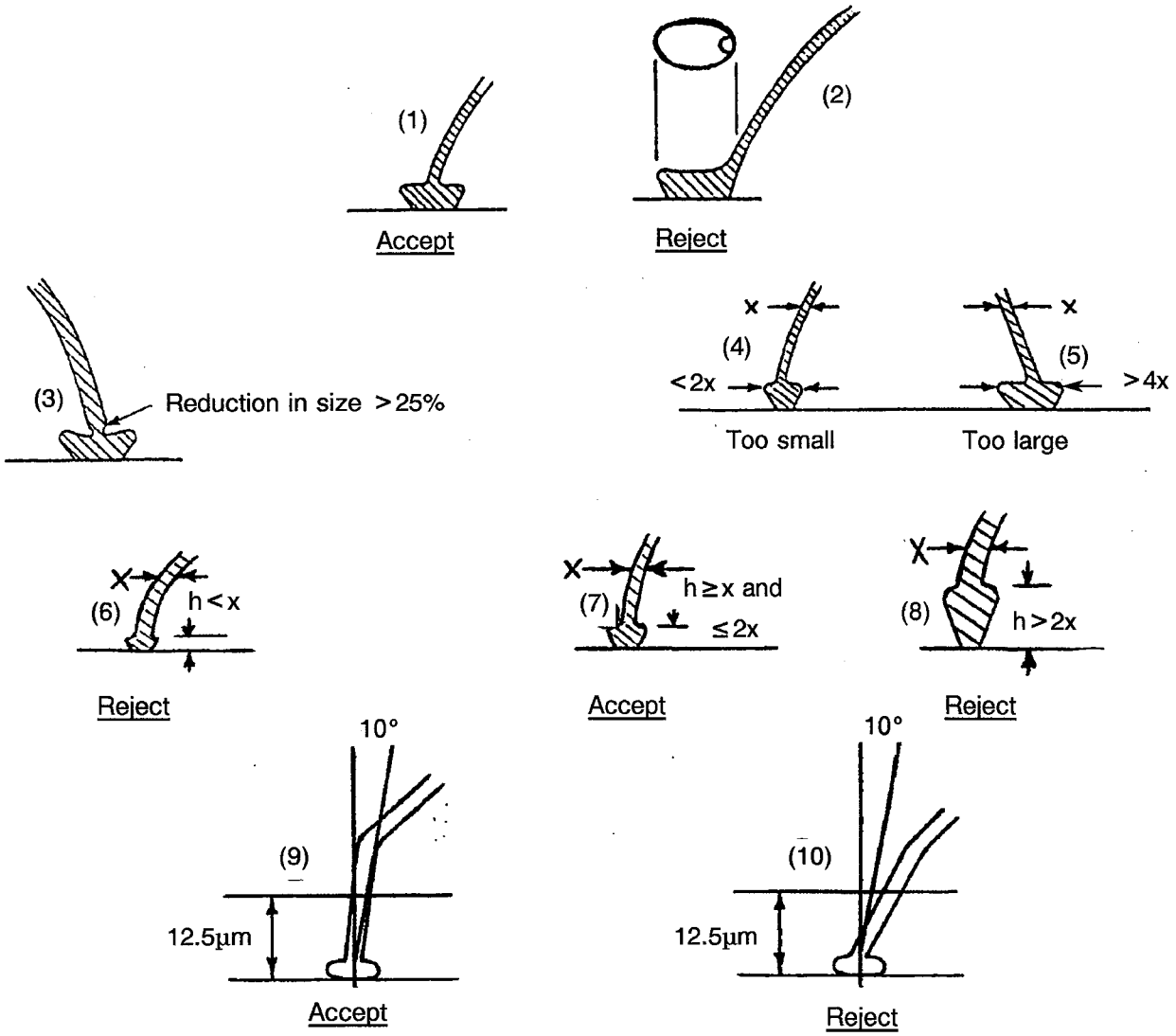
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.2.8.1(f)	Bond or another bond
2	X		3.2.8.1(j)	Correct bonds
3		X	3.2.8.1(j)	Lifted bonds

FIGURE XVI - GENERAL WIRE AND BOND DEFECTS (3.2.8.1) (CONTINUED)



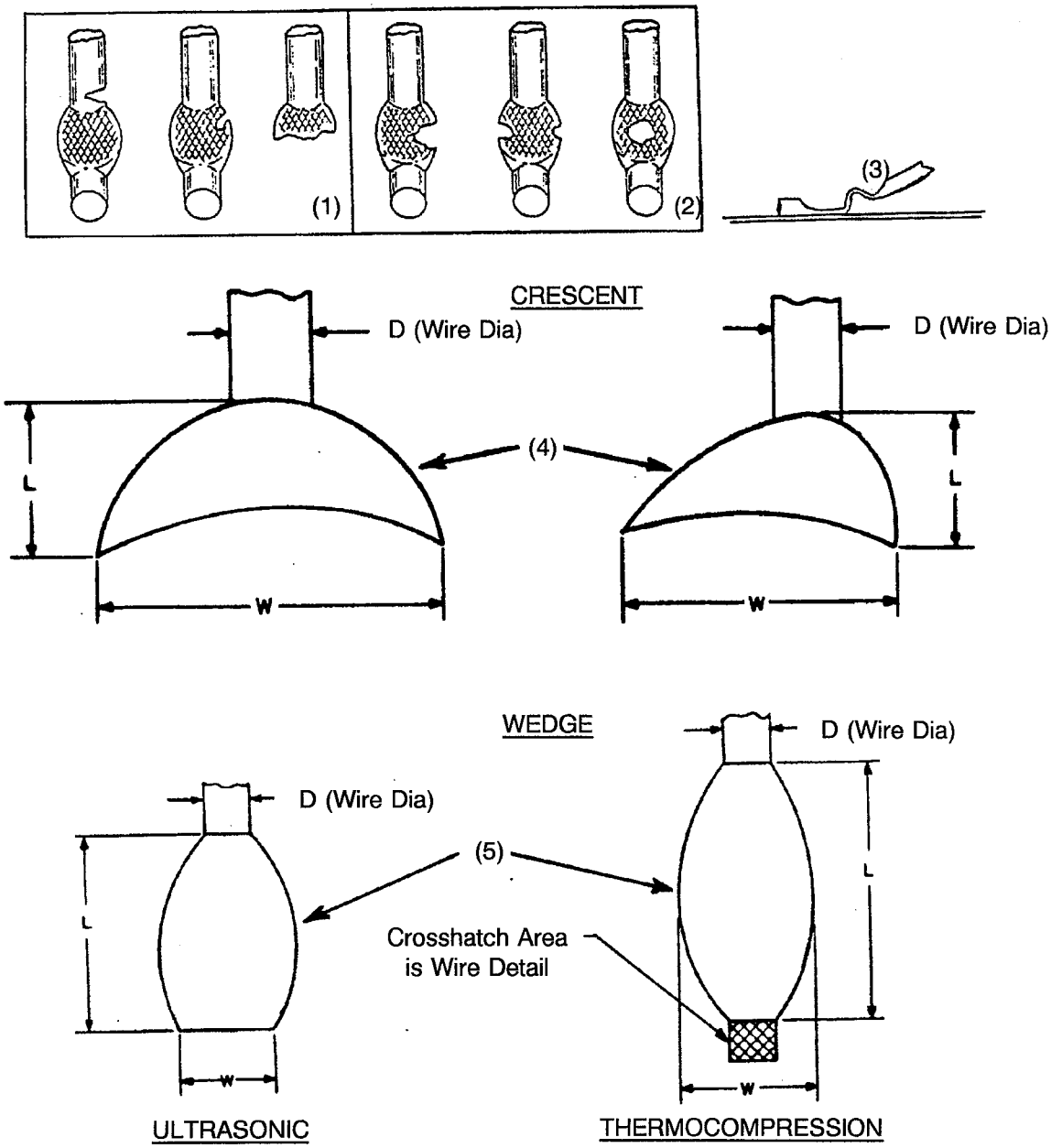
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.8.1(p)	Tail <2 wire diameters
2		X	3.2.8.1(p)	Tail >1/2 post diameters
3		X	3.2.8.1(p)	Extra pigtail

FIGURE XVII - GOLD BALL BONDS (3.2.8.2)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.2.8.2(b)	Correct termination
2		X	3.2.8.2(b)	Perimeter termination
3		X	3.2.8.2(c)	Reduction >25%
4		X	3.2.8.2(d)	<2 x wire diameter
5		X	3.2.8.2(d)	>4 x wire diameter
6		X	3.2.8.2(e)	Height <1 x wire diameter
7	X		3.2.8.2(e)	Correct height
8		X	3.2.8.2(e)	Height >2 x wire diameter
9	X		3.2.8.2(g)	Wire ≤10° to perpendicular
10		X	3.2.8.2(g)	Wire >10° to perpendicular

FIGURE XVIII - ULTRASONIC AND THERMOCOMPRESSION CRESCENT/WEDGE BONDS (3.2.8.3)



FAULT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X	3.2.8.3(a)	Pad bond torn in or behind bond area
2	X	3.2.8.3(b)	Nicks in side or centre of bond
3	X	3.2.8.3(c)	Needle impression area lifted >25%
4	X	3.2.8.3(f)	Width <1.2 or >5 x wire diameter Length <0.5 or >3 x wire diameter
5	X	3.2.8.3(h)	Width <1.2 or >3 x wire diameter Length <1.5 or >5 x wire diameter

3.2.8.4 Pillar/Post Bonds (see Figure XIX)

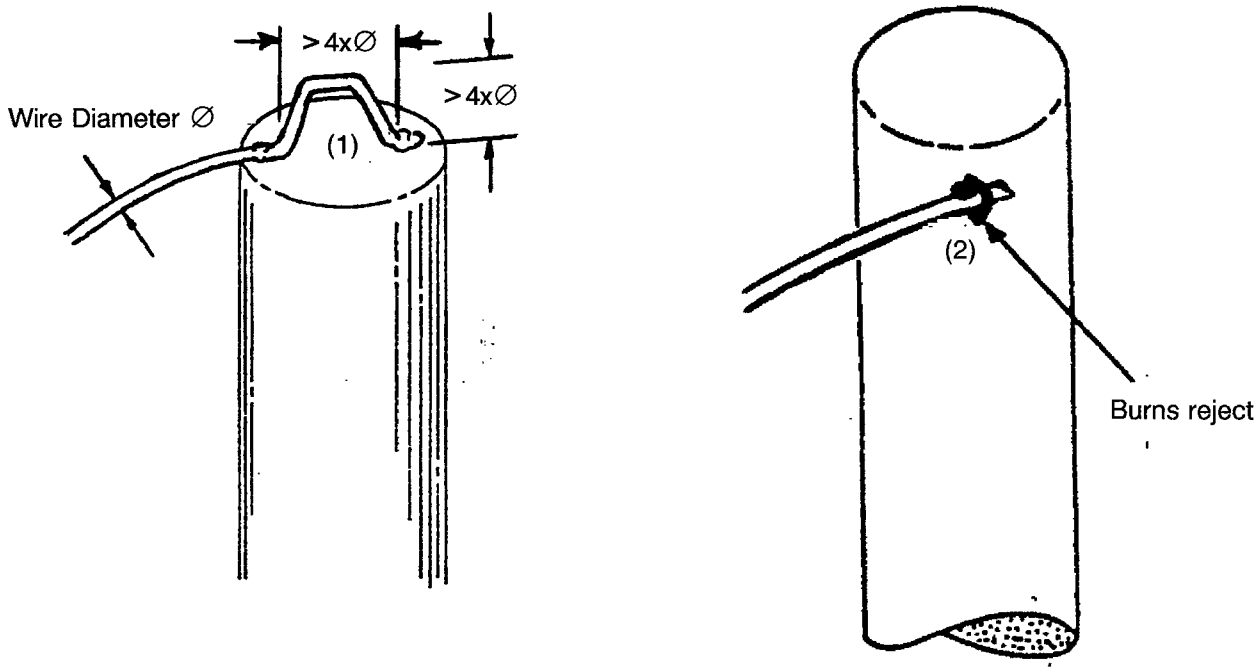
The criteria for ultrasonic and thermocompression wedge bonds shall apply and in addition:-

(a) First pillar bond not clear of the edge of the pillar.

(b) A bow or loop between double bonds greater than 4 x wire diameters.

(c) Excessive lead burn at lead/post weld.

FIGURE XIX - PILLAR/POST BONDS (3.2.8.4)



FAULT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X	3.2.8.4(b)	Bow or loop >4 x wire diameters
2	X	3.2.8.4(c)	Excessive lead burn

3.2.9 Rebonds

(a) Rebonding onto the die shall only be permitted where the bond pad area has been designed to accomodate a rebond (but see (b) below).

The second bond shall be at a point near to the metallisation exit. There shall be no residual bond material between the rebond and the exiting metallisation.

(b) Rebonds are permitted only if the original bonding has not removed bond pad material.

(c) At least 50% of the attachment area of a rebond shall be placed on undisturbed metal (excluding probe marks that do not expose underlying material).

(d) Only one rebond shall be permitted at one bonding pad or bonding terminal location.

(e) The total number of rebonds shall be limited to a maximum of 10% (to the nearest whole number) of the total number of bonds on the device.

One rebond can always be permitted with the provision that the conditions specified in (a), (b) and (c) above are satisfied.

3.2.10 Glassivation Defects (when applicable)

(a) Glass crazing that prevents the detection of the visual criteria contained below.

(b) Any glassivation which has delaminated. Lifting or peeling of the glassivation may be excluded from the above when it does not extend more than 25µm from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallisation leading from those pads.

(c) Two or more adjacent active metallisation pads which are not covered by glassivation, except by design.

(d) Unglassivated areas at the edge of a bonding pad which expose semiconductor material.

(e) Glassivation which covers more than 25% of the design bonding pad area.

3.2.11 Visual Condition of the Package of the Device

3.2.11.1 Foreign Matter

Foreign matter shall be considered to be attached when it cannot be removed with a soft camel hair brush, or a gas blow of dry nitrogen at 140KN/m^2 gauge applied for a minimum of three seconds from a distance of 50mm. In the case of the gas blow, the nozzle used shall not be less than 1.0mm in diameter.

N.B.
Tweezers or other instruments shall not be used to remove particles from the die surface.

3.2.11.2 Defects

(a) Attached foreign matter greater than 25µm in any dimension on the surface of the die or within the package.

(b) Loosely attached foreign particles (conductive particles which are attached by less than one half of their largest dimension) which are present on the surface of the die that are large enough to bridge the narrowest unglassivated active circuit element spacing.

(c) Embedded foreign particles on the die that bridge two or more metallisation paths or semiconductor junctions, or any combination of metallisation or junction.

(d) Liquid droplets, chemical stains or photoresist on the die surface that bridge any combinations of unglassivated metal or bare semiconductor material.

(e) Grease, varnish, ink or similar stain greater than 25µm in the greater dimension anywhere on the die, or bridging two areas of metallisation.

(f) Ink on the die surface that covers more than 25% of a bonding pad area, or that bridges any combination of unglassivated metallisation or bare semiconductor material, except for unused cells.

3.3 DIODES (GLASS ENCAPSULATED)

3.3.1 General

A unit shall be rejected if it exhibits one or more of the defects listed in any of the paragraphs detailed in Para. 3.3. Where applicable, drawings are included to provide additional explanatory material.

N.B.
Inspection of these devices shall be carried out after final seal, but prior to painting with opaque material, at an angle to the principal axis that is convenient for assessment of the feature under examination.

3.3.2 Mechanical Die Defects

3.3.2.1 General (see Figure XX)

The distance between oxide or metallisation and the edge of the chip shall not be less than 6.0µm. Excluded from this criterion are areas of metallisation or oxide which have the same potential as those areas to which a short circuit is possible.

3.3.2.2 Chip-outs or Offset Scribe Lines/Breaks (see Figure XX)

(a) A chip-out into the oxide or metallisation, or which comes within 6.0µm of the oxide.

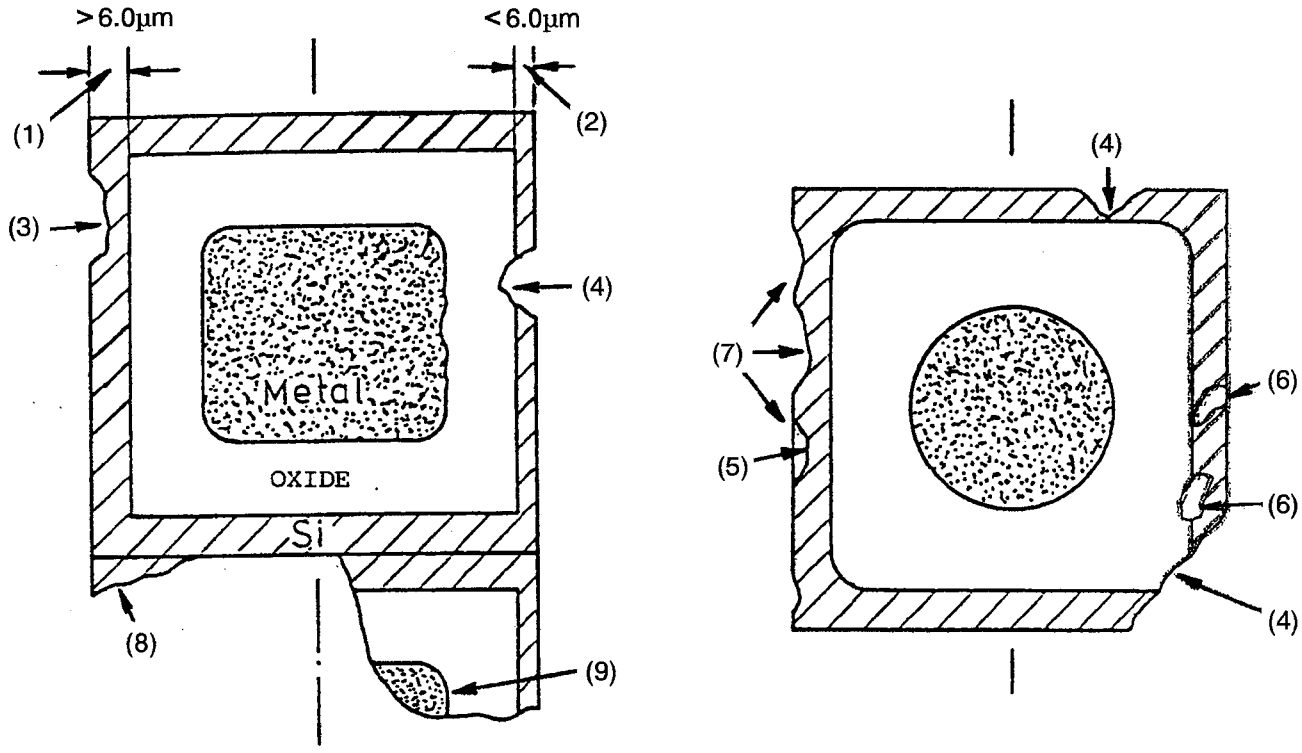
(b) Shell style chip-outs in the substrate going into the oxide or metallisation, or which come within 6.0µm of the oxide.

(c) A chip-out in the active circuit area, or extending from the scribe line in the active area.

(d) On any edge of the die, a chip-out or series of chip-outs where length, or aggregate length is greater than 25% of the die edge.

(e) Die having attached portions of another die which contains metallisation.

FIGURE XX - CHIP-OUTS OR OFFSET SCRIBE LINES/BREAKS (3.3.2.2)



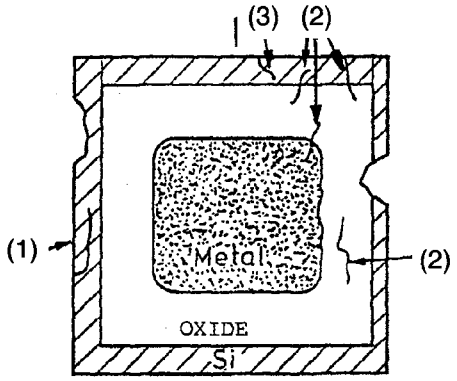
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.2.1	Edge of chip >6.0µm to metallisation
2		X	3.3.2.1	Edge of chip <6.0µm to metallisation
3	X		3.3.2.2(a)	Chip-out not into oxide
4		X	3.3.2.2(a)	Chip-out into oxide or within 6.0µm of oxide
5	X		3.3.2.2(b)	Chip-out not into oxide
6		X	3.3.2.2(b)	Chip-out into oxide or within 6.0µm of oxide
7		X	3.3.2.2(d)	Aggregate length >25%
8	X		3.3.2.2(e)	Attached die without metallisation
9		X	3.3.2.2(e)	Attached die with metallisation

3.3.2.3 Cracks (see Figure XXI)

(a) A crack in the oxide or metallisation.

(b) A crack in the substrate which is within 6.0μm of the oxide.

FIGURE XXI - CRACKS (3.3.2.3)

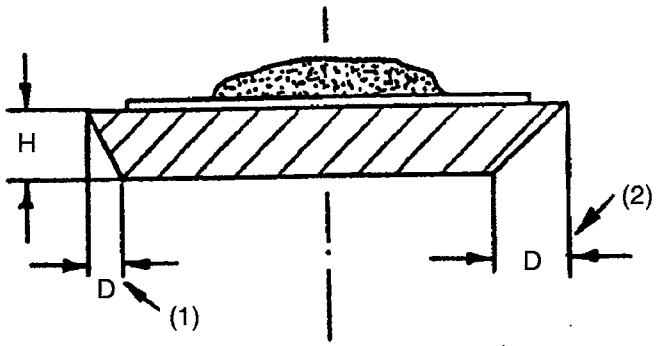


FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.2.3(a)	Crack not into metallisation
2		X	3.3.2.3(a)	Crack in oxide or metallisation
3		X	3.3.2.3(b)	Crack < 6.0μm to oxide

3.3.2.4 Overhangs (see Figure XXII)

The overhang between upper and lower edges of the silicon must not exceed the thickness of the silicon chip.

FIGURE XXII - OVERHANGS (3.3.2.4)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.2.4	Overhang D < H
2		X	3.3.2.4	Overhang D > H

3.3.3 Metallisation Defects (see Figure XXIII)

(a) Evidence of metallisation corrosion. Metallisation having any discoloured localised area shall be closely examined and shall be rejected unless it is demonstrated to be caused by a harmless effect.

(b) Evidence of metallisation lifting, peeling or blistering.

(c) Scratches or voids in the metallisation which expose underlying material.

(d) Bumps, bubbles or stubs exceeding metallisation thickness by greater than 50%.

(e) Cavities in the metallisation of dimension exceeding 25% of the metallisation side-length.

(f) Excessive contact material which reduces the design separation to the edge of the oxide area by more than 50%.

(g) Voids in the metallisation of dimension exceeding 10% of the metallisation side-length.

(h) Misplacement of a contact area which reduces the design separation to the edge of the oxide area by greater than 50%.

3.3.4 Oxide and Diffusion Faults (see Figure XXIV)

(a) A diffusion area that appears to be discontinuous.

(b) A diffusion fault that allows bridging between any two diffused areas, any two metallisation areas or any combination thereof not intended by design.

(c) An oxide fault, including pinholes, that exposes bare semiconductor material and allows bridging between any two diffused areas or a combination thereof not intended by design.

(d) Bare semiconductor material areas not covered by oxide and exposing or touching any metallisation.

(e) An absence of oxide, visible at the edge and continuing under the metallisation, such as to cause an apparent short between the metal and the underlying material. (Double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the bare semiconductor materials).

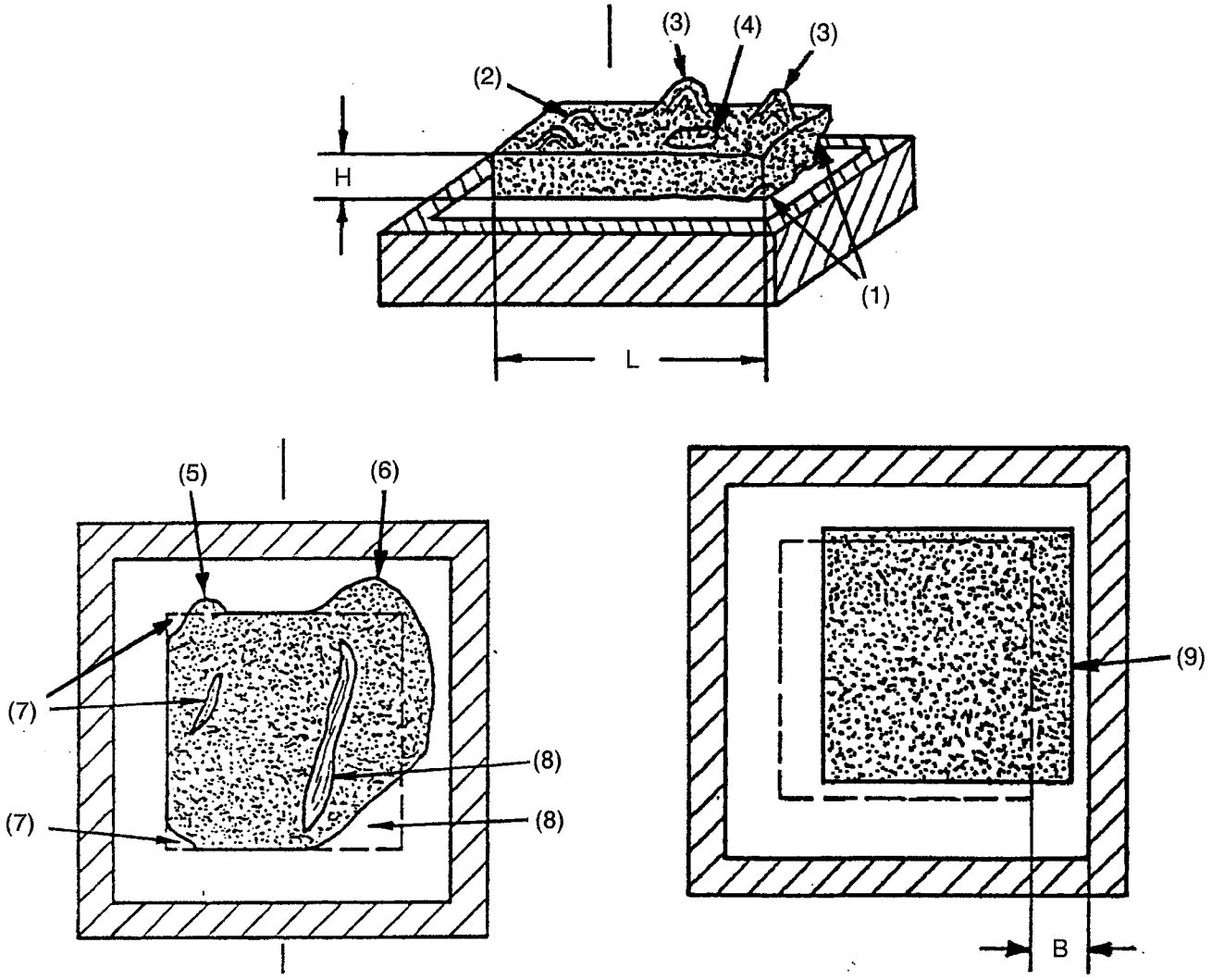
(f) Areas of undercutting which exhibit other than normal oxide colour differentiation.

(g) A depression or irregularity which is not part of the design pattern and which is completely covered by metallisation.

(h) Evidence of over-etching.

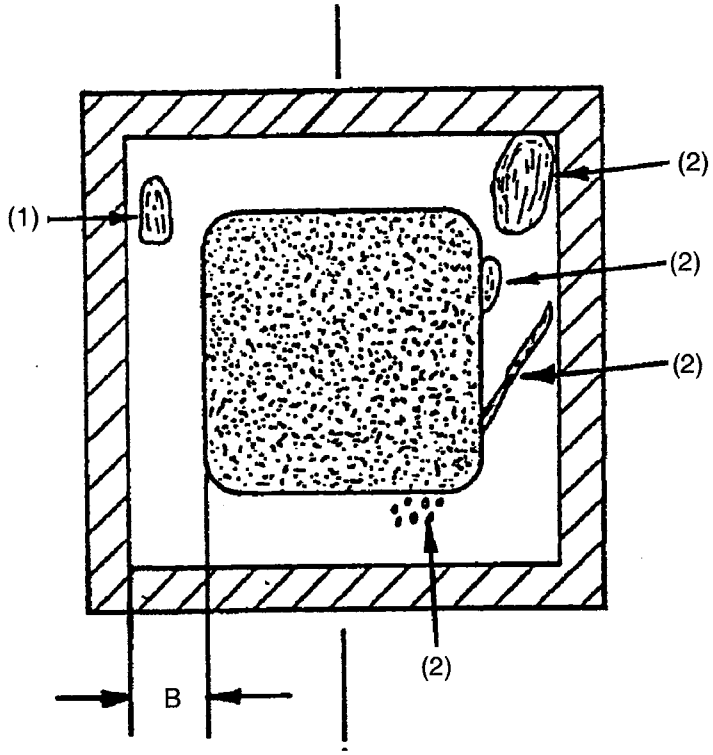
(i) Scratches, voids or missing oxide that come closer to the metallisation than 50% of the design separation distance between the metallisation and the exposed substrate.

FIGURE XXIII - METALLISATION DEFECTS (3.3.3)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.3.3(c)	Peeled or lifted
2	X		3.3.3(d)	<50% H
3		X	3.3.3(d)	>50% H
4	X		3.3.3(e)	<25% L
5	X		3.3.3(f)	<50% of design separation
6		X	3.3.3(f)	>50% of design separation
7	X		3.3.3(g)	<10% of side-length
8		X	3.3.3(g)	>10% of side-length
9		X	3.3.3(h)	>50% reduction

FIGURE XXIV - OXIDE AND DIFFUSION FAULTS (3.3.4)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.4(i)	Further than 50% B
2		X	3.3.4(i)	Closer than 50% B

3.3.5 Die-Mounting Defects (See Figure XXV)

(a) One or more dies of a die stack tilted by more than 10° from its mounting plane.

(b) Pinnacles of unattached mounting material higher than half the height of the die.

(c) Mounting material touching the die surface.

(d) Mounting material on the die surface.

(e) Voids in the fillet whose length are greater than 25% of one side-length.

(f) A die which has shifted laterally greater than 25% of the thickness of the die.

(g) Missing mounting material which is greater than the solder thickness, or is greater than 25% of the perimeter.

(h) Excessive mounting material greater than twice the solder thickness.

(i) When the contact of the element is less than two thirds of the diameter.

(j) Die damaged during the mounting process.

3.3.6 Mechanical Defects (see Figure XXVI)

(a) Less than two thirds of the contact button touches the bottom of the whisker.

(b) The angle between the base of the whisker and the contact area is greater than 10°.

(c) Whisker is deformed by more than 20° from the horizontal.

(d) Whisker is compressed by more than 50% of its specified height.

(e) No evidence of pressure of the lower whisker arm on the button.

(f) Point contact between the base of the whisker and the die.

(g) Heel or edge contact between the base of the whisker and the die. For diodes where this type of contact is permitted by design, the complete width of the 'S' or 'C' whisker must cover the contact area.

(h) Less than 250µm spacing between each half of the whisker.

(i) Whisker in contact with the glass body wall.

(j) The position of the contact stud is tilted by more than 5° relative to the centre-line of the unit.

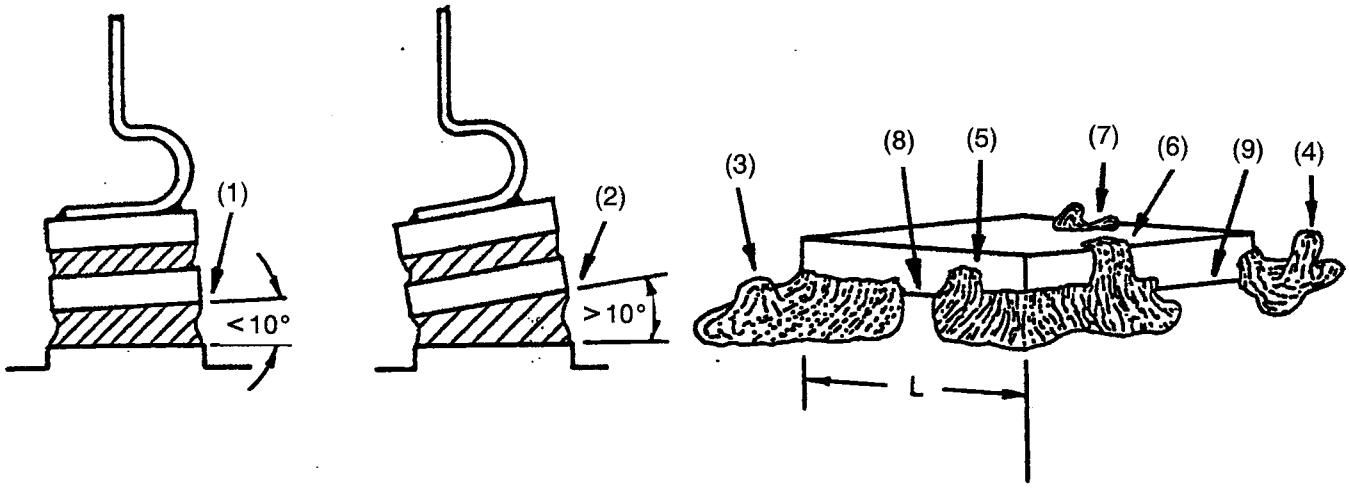
(k) The centre-line of a stud or whisker is displaced by more than quarter diameter relative to the centre of the contact spot (alloy area).

(l) Less than 50% of the anode post end surface welded to the whisker.

(m) Less than 50% perimeter coverage of the anode lead-to-die solder contact.

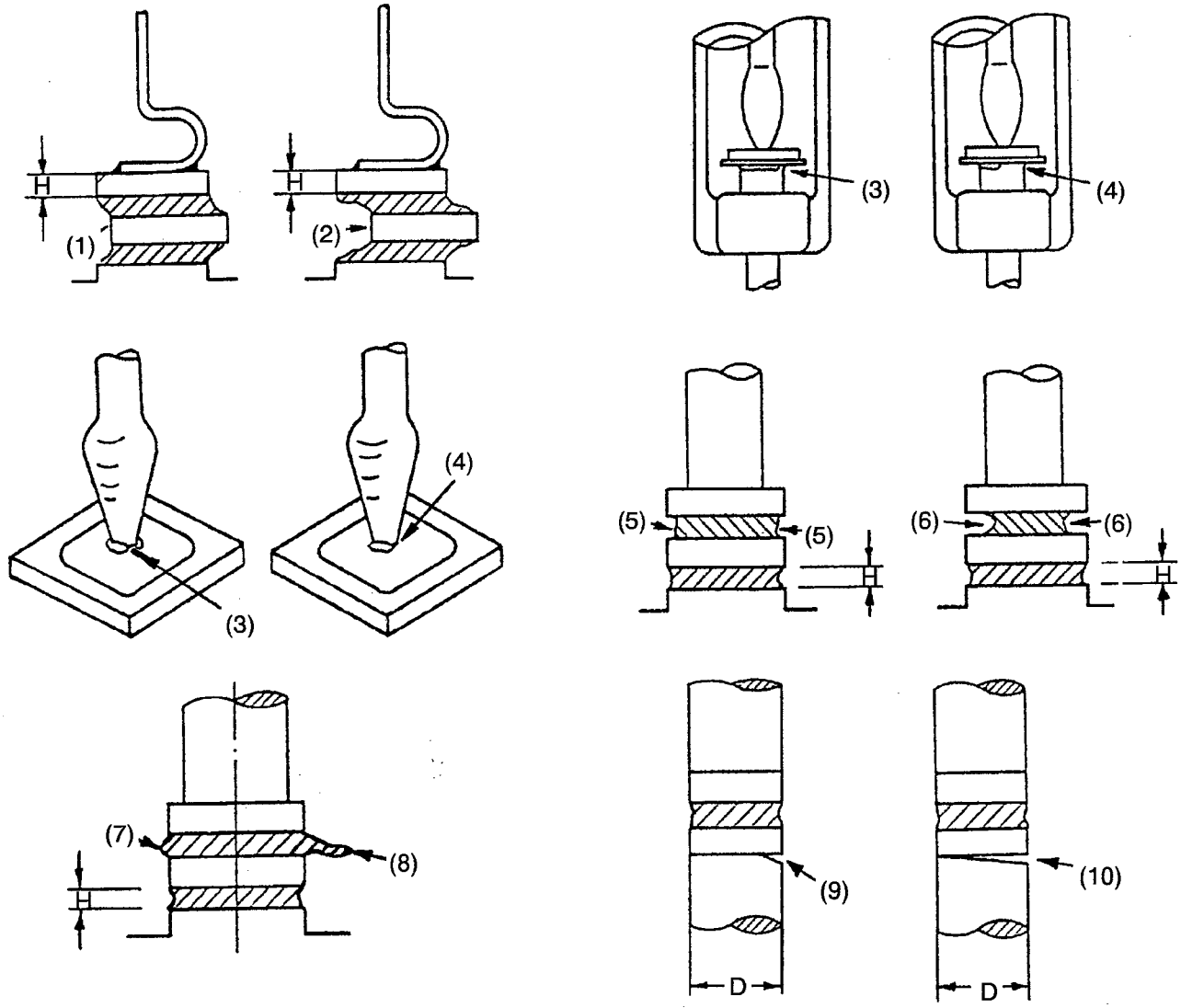
(n) Excessive solder flow at the lead-to-die contact bridging any passivated area of the die.

FIGURE XXV - DIE-MOUNTING DEFECTS (3.3.5)



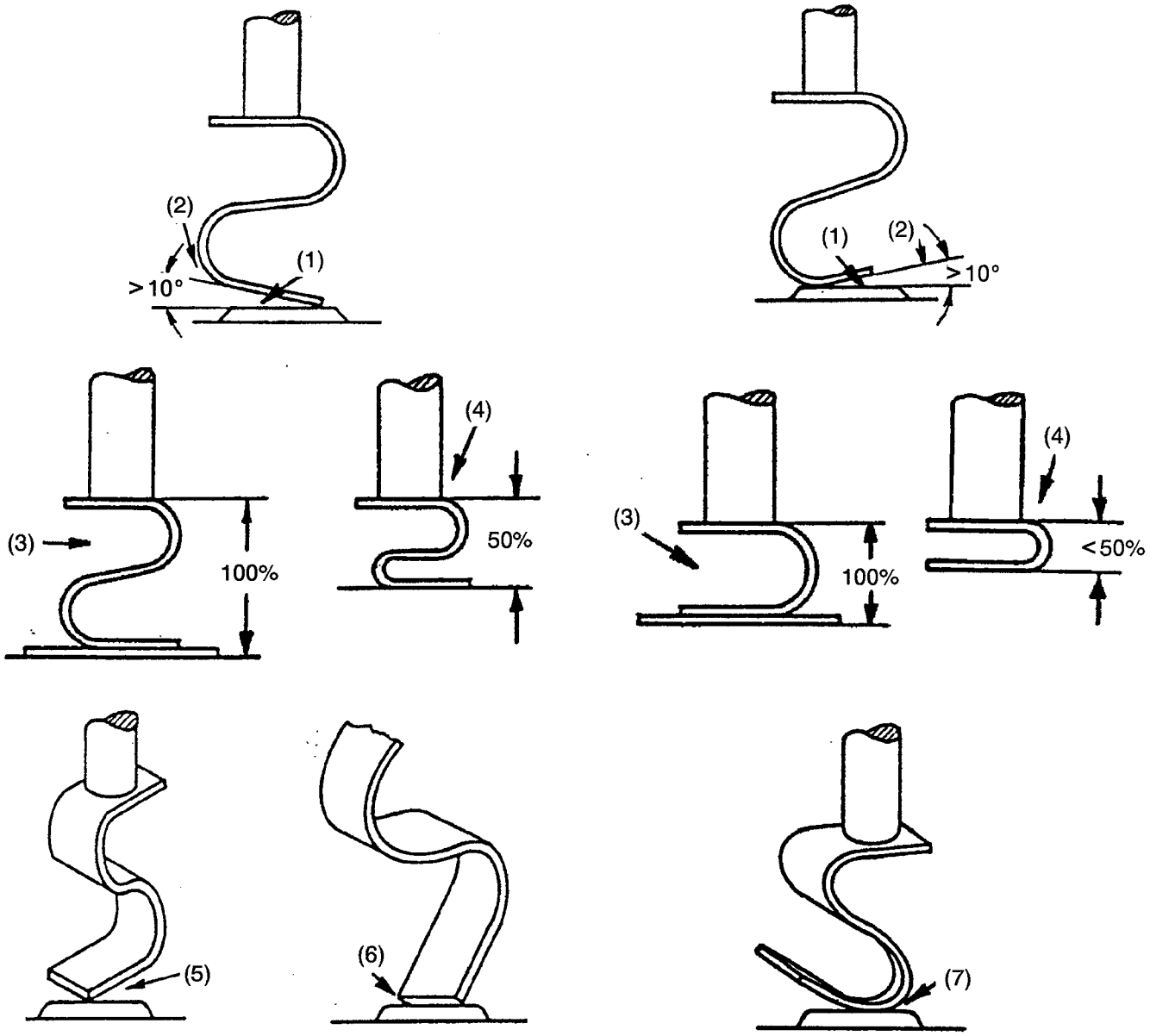
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.5(a)	Tilt < 10%
2		X	3.3.5(a)	Tilt > 10%
3	X		3.3.5(b)	< 1/2 height of die
4		X	3.3.5(b)	> 1/2 height of die
5	X		3.3.5(c)	Correct mounting
6		X	3.3.5(c)	Material touches die surface
7		X	3.3.5(d)	Material on die surface
8	X		3.3.5(e)	Length < 25%
9		X	3.3.5(e)	Length > 25%

FIGURE XXV - DIE-MOUNTING DEFECTS (3.3.5) (CONTINUED)



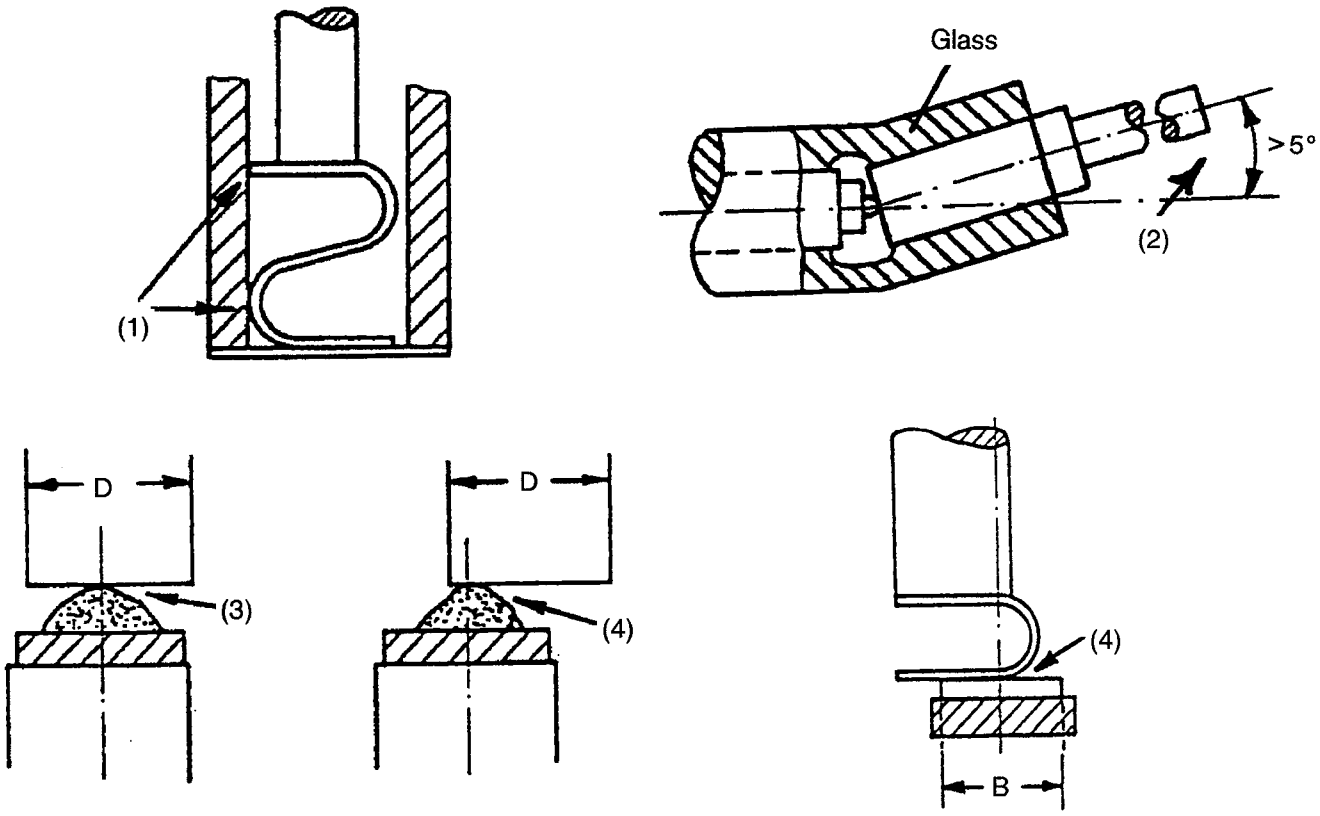
FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.5(f)	Shift < 25%H
2		X	3.3.5(f)	Shift > 25%H
3	X		3.3.5(g)	< 25% perimeter missing
4		X	3.3.5(g)	> 25% perimeter missing
5	X		3.3.5(g)	< h missing
6		X	3.3.5(g)	> h missing
7	X		3.3.5(h)	< 2 x solder thickness
8		X	3.3.5(h)	> 2 x solder thickness
9	X		3.3.5(i)	> 2/3 contact
10		X	3.3.5(i)	< 2/3 contact

FIGURE XXVI - MECHANICAL DEFECTS (3.3.6)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.3.6(a)	< 2/3 physical contact
2		X	3.3.6(b)	> 10°
3	X		3.3.6(d)	Compression ≤ 50%
4		X	3.3.6(d)	Compression > 50%
5		X	3.3.6(f)	Point contact
6		X	3.3.6(g)	Edge contact
7		X	3.3.6(g)	Heel contact

FIGURE XXVI - MECHANICAL DEFECTS (3.3.6) (CONTINUED)



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1		X	3.3.6(i)	Whisker contacting glass
2		X	3.3.6(j)	Tilt >5°
3	X		3.3.6(k)	Displacement < D/4
4		X	3.3.6(k)	Displacement > B/4 or D/4

3.3.7 Glass Body and End Seal Defects (see Figure XXVII)

(a) Glass-to-glass or glass-to-metal seal with a width of less than 500 µm.

(b) Glass thickness in the sealing area less than one half of the glass body nominal thickness.

(c) "Pinch-in" of the glass body greater than one half of the glass body nominal thickness.

(d) Chip-outs or flaking in the glass body, or chip-outs in the seal area which are greater than one half of the seal inner radius or greater than 90° of the perimeter of the seal centre.

(e) Insufficient flow of glass at the boundary of glass to metal.

(f) Glass bead or any portion of it higher than the first seal opening due to glass-to-glass seal fusing to high.

(g) Fusion area not completely encircling the lead.

(h) Voids and bubbles in the glass body which are greater than one third of the glass body nominal thickness, or several small voids or bubbles, or notches or voids whose depths are not definable.

(i) Voids or bubbles or an area of adjacent bubbles greater than 12.5% of the seal area.

(j) Glass body tilted to the centre-line at an angle greater than 5°.

(k) Cracks in the outer glass body where the depth is not definable, radial cracks of any depth in the seal of dimension greater than one half of the seal inner radius.

(l) Circular cracks of any depth of dimension greater than 90° of the glass perimeter.

(m) Eccentricity of lead passing through the end of the body greater than one half of the seal inner radius.

(n) Lead tilted by greater than 5%.

(o) Lead touching or overhanging the passivation when the die is central to the post.

(p) Meniscus height greater than twice the lead diameter.

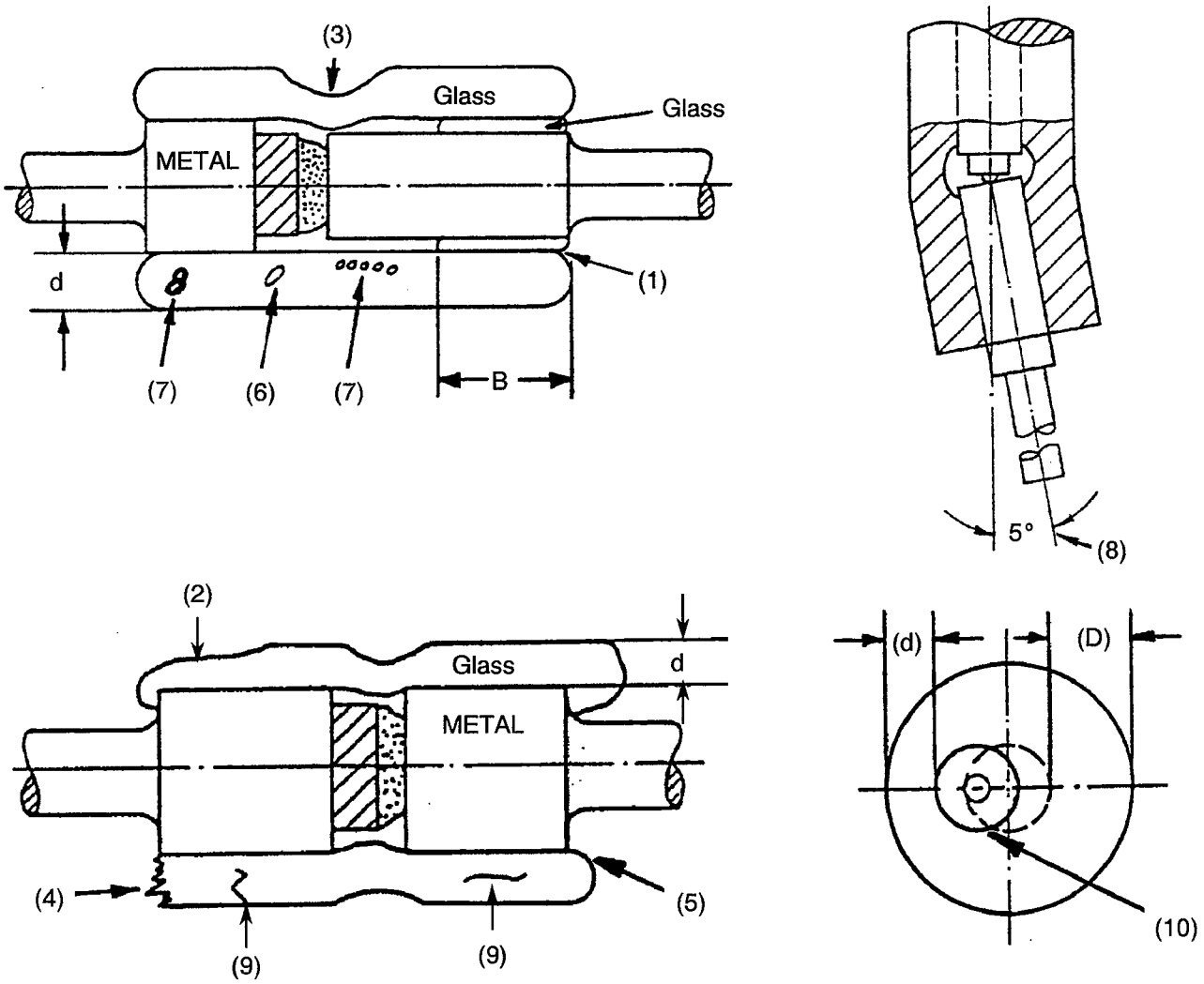
(g) Foreign particles enclosed in the glass seal.

3.3.8 Foreign Matter

(a) Metallic particles greater than 40µm within the package.

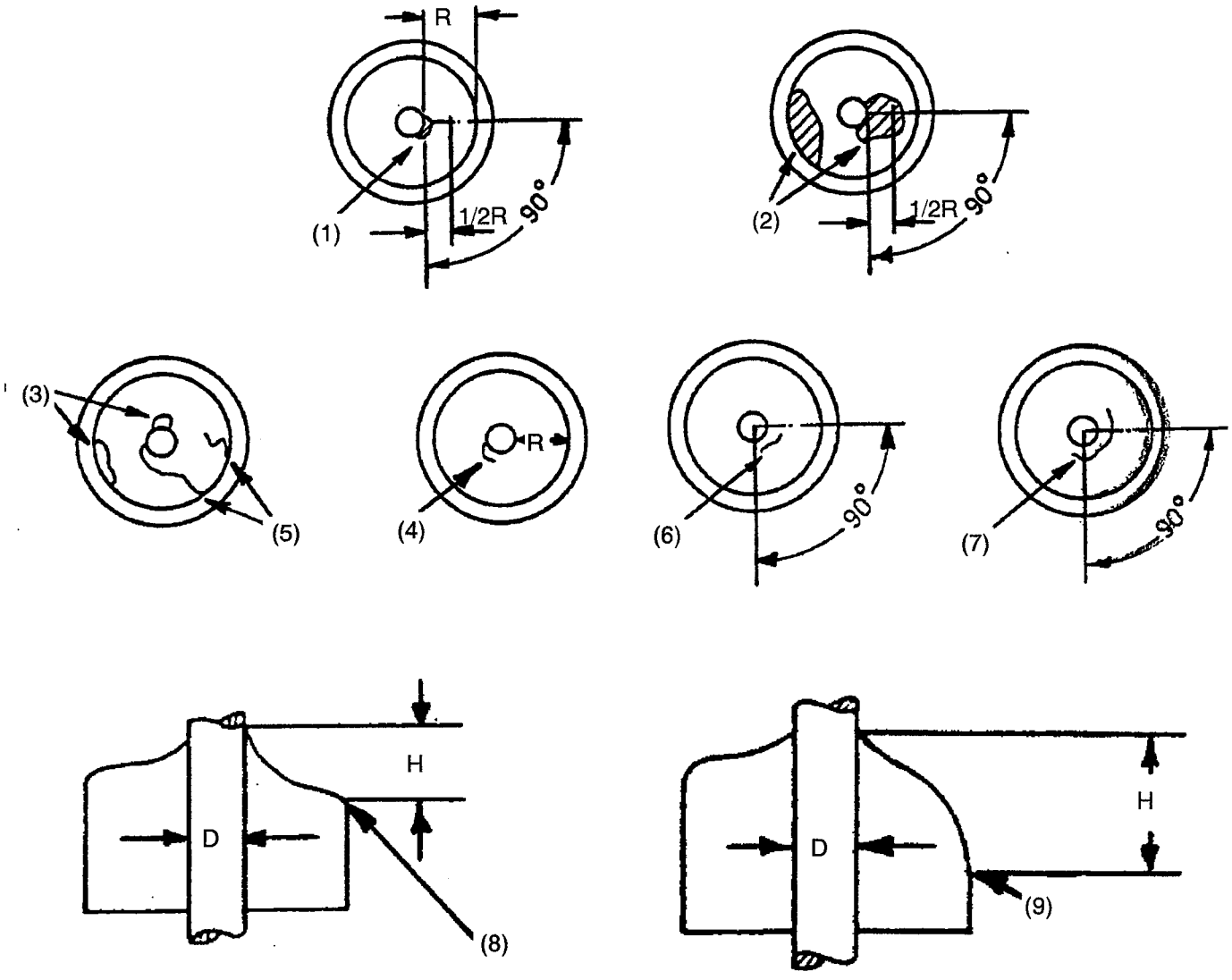
(b) Non-metallic particles greater than 200µm within the package.

FIGURE XXVII - GLASS BODY AND END SEAL DEFECTS (3.3.7)



FAULT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X	3.3.7(a)	Seal width B<500μm
2	X	3.3.7(b)	Glass thickness <d/2
3	X	3.3.7(c)	"Pinch-in" >d/2
4	X	3.3.7(d)	Chipped glass body
5	X	3.3.7(e)	Insufficient glass flow
6	X	3.3.7(h)	Void, bubble>d/3
7	X	3.3.7(h)	Several small voids
8	X	3.3.7(j)	Body tilted >5°
9	X	3.3.7(k)	Cracks >d/2
10	X	3.3.7(m)	Eccentricity >D/2

FIGURE XXVII - GLASS BODY AND END SEAL DEFECTS (3.3.7) CONTINUED



FAULT	ACCEPT	REJECT	APPLICABLE SECTION	JUSTIFICATION
1	X		3.3.7(d)	Chip-out < R/2
2		X	3.3.7(d)	Chip-out > R/2 or 90°
3		X	3.3.7(h)	Undefinable depth
4	X		3.3.7(k)	Radial crack < R/2
5		X	3.3.7(k)	Radial crack > R/2
6	X		3.3.7(l)	Circular crack < 90°
7		X	3.3.7(l)	Circular crack > 90°
8	X		3.3.7(p)	Meniscus height < 2xD
9		X	3.3.7(p)	Meniscus height > 2xD