



Pages 1 to 25

**TRANSISTORS, MICROWAVE, SMALL SIGNAL, SILICON,  
BIPOLAR**

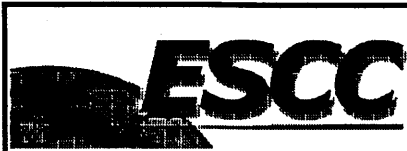
**BASED ON TYPES BFY180 THRU BFY183,  
BFY193, BFY193C, BFY196 AND BFY280**

**ESCC Detail Specification No. 5611/006**

Issue 4	June 2011
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640	Specification upissued to incorporate editorial and technical changes per DCR.



**TABLE OF CONTENTS**

	<u>Page</u>
<b>1. <u>GENERAL</u></b>	<b>5</b>
1.1 Scope	5
1.2 Component Type Variants	5
1.3 Maximum Ratings	5
1.4 Parameter Derating Information	5
1.5 Physical Dimensions	5
1.6 Functional Diagram	5
1.7 Handling Precautions	5
<b>2. <u>APPLICABLE DOCUMENTS</u></b>	<b>5</b>
<b>3. <u>TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS</u></b>	<b>5</b>
<b>4. <u>REQUIREMENTS</u></b>	<b>10</b>
4.1 General	10
4.2 Deviations from Generic Specification	10
4.2.1 Deviations from Production Control	10
4.2.2 Deviations from Final Production Tests	10
4.2.3 Deviations from Burn-in and Electrical Measurements	10
4.2.4 Deviations from Qualification Tests	10
4.2.5 Deviations from Lot Acceptance Tests	10
4.3 Mechanical Requirements	11
4.3.1 Dimension Check	11
4.3.2 Weight	11
4.3.3 Terminal Strength	11
4.3.4 Bond Strength	11
4.3.5 Die Shear	11
4.4 Materials and Finishes	12
4.4.1 Case	12
4.4.2 Lead Material and Finish	12
4.5 Marking	12
4.5.1 General	12
4.5.2 Terminal Identification	12
4.5.3 The ESCC Component Number	12
4.5.4 Traceability Information	12
4.6 Electrical Measurements	12
4.6.1 Electrical Measurements at Room Temperature	12
4.6.2 Electrical Measurements at High and Low Temperatures	13
4.6.3 Circuits for Electrical Measurements	13
4.7 Burn-in Tests	13
4.7.1 Parameter Drift Values	13
4.7.2 Conditions for High Temperature Reverse Bias Burn-in	13
4.7.3 Conditions for Power Burn-in	13
4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-in	13
4.7.5 Electrical Circuit for Power Burn-in	13
4.8 Environmental and Endurance Tests	13
4.8.1 Electrical Measurements on Completion of Environmental Tests	13
4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests	13
4.8.3 Conditions for Operating Life Test	23
4.8.4 Electrical Circuit for Operating Life Test	23
4.9 Total Dose Irradiation Testing	23
4.10 Special Testing	23



**TABLES**

	<u>Page</u>
1(a) Type Variants	6
1(b) Maximum Ratings	7
2 Electrical Measurements at Room Temperature - DC Parameters	14
Electrical Measurements at Room Temperature - AC Parameters	15
3 Electrical Measurements at High and Low Temperatures	17
4 Parameter Drift Values	19
5(a) Conditions for High Temperature Reverse Bias Burn-in	20
5(b) Conditions for Power Burn-in and Operating Life Tests	20
6 Electrical Measurements at Intermediate Points and on Completion of Endurance Testing	24
7 Electrical Measurements During and on Completion of Irradiation Testing	24

**FIGURES**

1 Parameter Derating Information	8
2 Physical Dimensions	9
3 Functional Diagram	9
4 Circuits for Electrical Measurements	17
5 Electrical Circuit for Burn-in	21
6 Bias Conditions for Irradiation Testing	24

**APPENDICES (Applicable to specific Manufacturers only)**

'A' Agreed Deviations for INFINEON TECHNOLOGIES (D)	25
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## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Microwave, Small Signal, Silicon, Bipolar, based on Types BFY180 thru BFY183, BFY193, BFY193C, BFY196 and BFY280. It shall be read in conjunction with ESCC Generic Specification No. 5010, the requirements of which are supplemented herein.

### 1.2 COMPONENT TYPE VARIANTS

Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

### 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the component specified herein, are scheduled in Table 1(b).

### 1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the components specified herein is shown in Figure 1.

### 1.5 PHYSICAL DIMENSIONS

The physical dimensions of the components specified herein are shown in Figure 2.

### 1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the components specified herein, is shown in Figure 3.

### 1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture test, packaging, shipping and handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500V for Variants 01 to 03 and 1000V for Variants 04 to 08.

## 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components.
- (b) MIL-STD-750, Test Methods for Semiconductor Devices.

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

MAG	=	Maximum Available Gain.
MSG	=	Maximum Stable Gain.
R <sub>B</sub>	=	External Base Resistor
R <sub>E</sub>	=	External Emitter Resistor
R <sub>TH(J-A)</sub>	=	Thermal Resistance, Junction to Ambient.
R <sub>TH(J-S)</sub>	=	Thermal Resistance, Junction to Soldering Point.
R <sub>TH(S-A)</sub>	=	Thermal Resistance, Soldering Point to Ambient.
V <sub>CC</sub>	=	Output Voltage from Collector Power Supply.
V <sub>BB</sub>	=	Output Voltage from Collector Power Supply



**TABLE 1(a) - TYPE VARIANTS**

(1) VARIANT	(2) TYPE	(3) CASE	(4) FIGURE	(5) LEAD MATERIAL AND FINISH
01	BFY180	MICRO-X1	2	D2
02	BFY280	MICRO-X1	2	D2
03	BFY181	MICRO-X1	2	D2
04	BFY182	MICRO-X1	2	D2
05	BFY183	MICRO-X1	2	D2
06	BFY193	MICRO-X1	2	D2
07	BFY196	MICRO-X1	2	D2
08	BFY193C	MICRO-X1	2	D2

**TABLE 1(b) - MAXIMUM RATINGS**

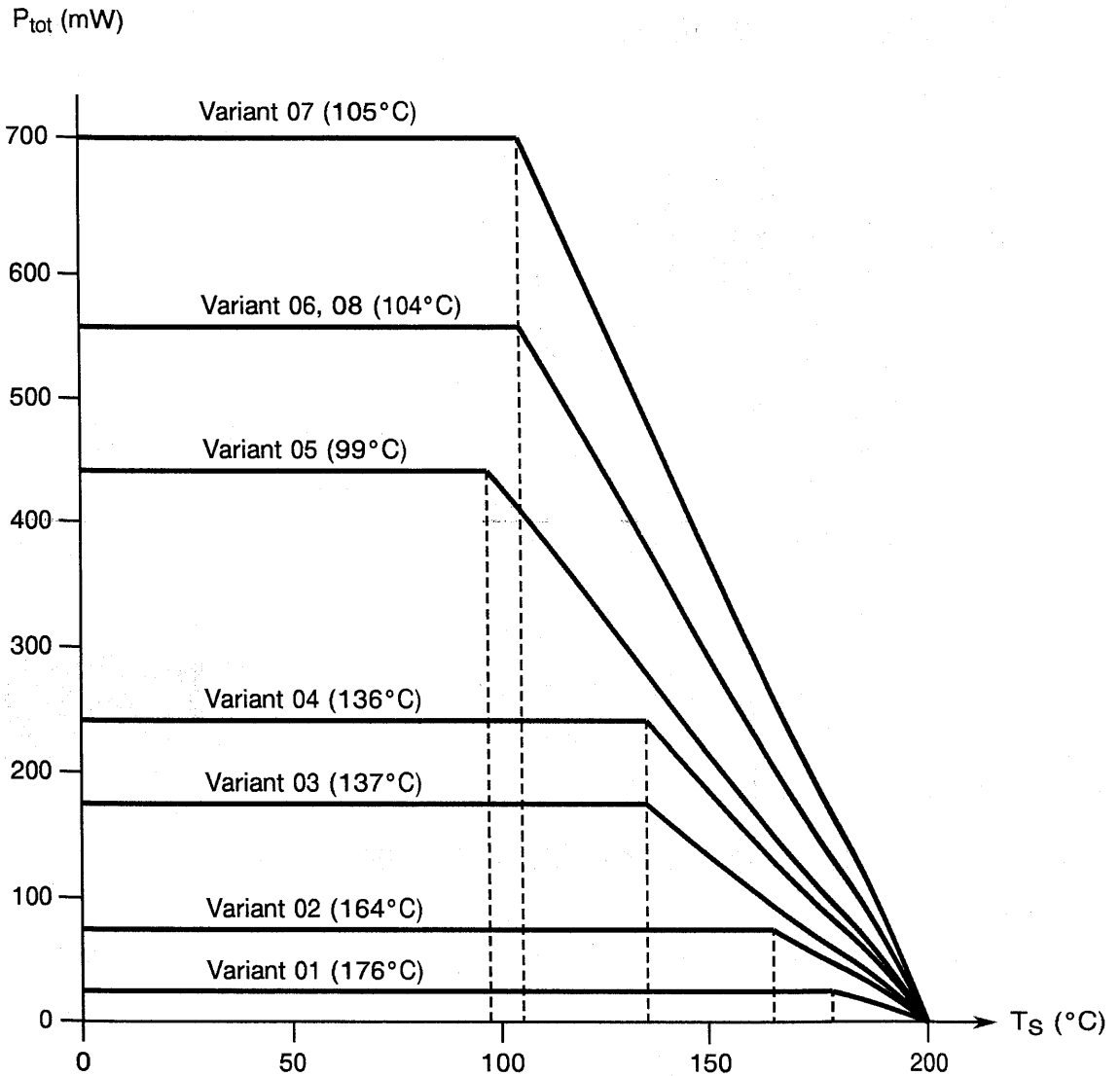
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Collector-Emitter Voltage Variants 01 and 02 Variants 03 to 08	$V_{CE0}$	8 12	V	
2	Collector-Emitter Voltage Variants 01 and 02 Variants 03 to 08	$V_{CES}$	15 20	V	
3	Collector-Base Voltage Variants 01 and 02 Variants 03 to 08	$V_{CBO}$	15 20	V	
4	Emitter-Base Voltage	$V_{EBO}$	2	V	
5	Collector Current Variant 01 Variant 02 Variant 03 Variant 04 Variant 05 Variant 06, 08 Variant 07	$I_C$	4 10 20 35 65 80 100	mA	
6	Base Current Variant 01 Variant 02 Variant 03 Variant 04 Variant 05 Variant 06, 08 Variant 07	$I_B$	0.5 1.2 2 4 5 10 12	mA	Note 1
6	Power Dissipation Variant 01 Variant 02 Variant 03 Variant 04 Variant 05 Variant 06, 08 Variant 07	$P_{tot}$	30 ( $T_S \leq 176^\circ\text{C}$ ) 80 ( $T_S \leq 164^\circ\text{C}$ ) 175 ( $T_S \leq 137^\circ\text{C}$ ) 250 ( $T_S \leq 136^\circ\text{C}$ ) 450 ( $T_S \leq 99^\circ\text{C}$ ) 580 ( $T_S \leq 104^\circ\text{C}$ ) 700 ( $T_S \leq 105^\circ\text{C}$ )	mW	Notes 2 and 3
8	Operating Temperature Range	$T_{op}$	-65 to +200	$^\circ\text{C}$	$T_{amb}$
9	Storage Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$	
10	Soldering Temperature	$T_{sol}$	+250	$^\circ\text{C}$	Note 4
11	Junction Temperature	$T_J$	+200	$^\circ\text{C}$	

**NOTES**

- Maximum ratings must not be exceeded under any combination of DC ratings and RF voltage/current swings, except that the maximum base current can be exceeded for the purpose of Base-Emitter-Forward Voltage pulsed measurement provided that the pulse duration  $< 1\text{s}$  and  $I_C = 0\text{A}$ .
- $T_S$  is measured on the collector lead at the soldering point to the pcb.
- At the  $T_S$  specified. For derating at  $T_S$  greater than specified, see Figure 1.
- Duration 5 seconds maximum at a distance of not less than 0.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.



**FIGURE 1 - PARAMETER DERATING INFORMATION**



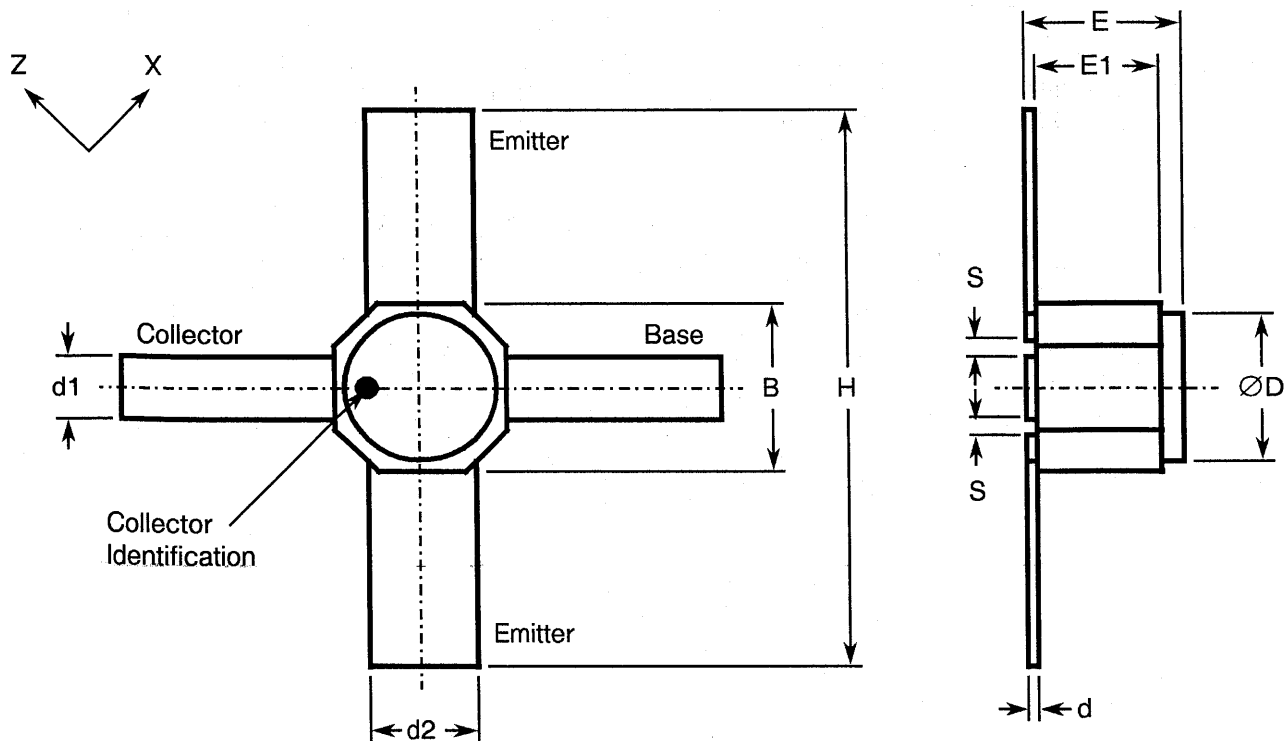
Power Dissipation versus Solder-Point Temperature

**NOTES**

Thermal Resistance, Junction to Soldering Point  $R_{TH(J-S)}$ :

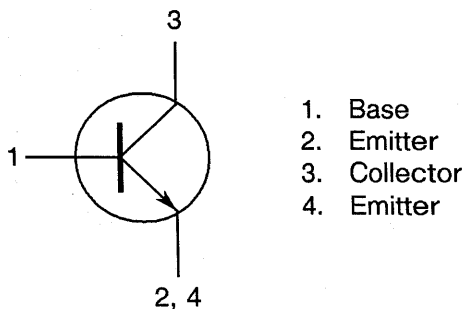
- Variant 01: 805°C/W
- Variant 02: 450°C/W
- Variant 03: 360°C/W
- Variant 04: 255°C/W
- Variant 05: 225°C/W
- Variant 06: 165°C/W
- Variant 07: 135°C/W
- Variant 08: 165°C/W

**FIGURE 2 - PHYSICAL DIMENSIONS**



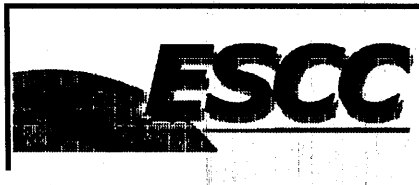
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
B	1.68	1.88	
d	0.07	0.15	
d1	0.40	0.60	
d2	0.92	1.12	
ØD	1.55	1.85	
E	0.85	1.25	
E1	0.66	0.86	
H	4.00	4.40	
S	0.08	0.30	

**FIGURE 3 - FUNCTIONAL DIAGRAM**



**NOTES**

1. The collector is marked with a black dot.



#### 4. REQUIREMENTS

##### 4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

##### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

###### 4.2.1 Deviations from Production Control

None.

###### 4.2.2 Deviations from Final Production Tests (Chart II(b))

(a) Para. 9.5, Thermal Shock: May also be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C.

(b) Para. 9.7, Particle Impact Noise Detection (PIND) test: May be performed at any point after the position indicated in Chart II(b), but before final seal test, gross leak and fine leak.

###### 4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III(b))

(a) Para. 9.9.2, Table 3 measurements: May be performed at any stage after power burn-in.

(b) Para. 9.9.3, Table 2 measurements: May be performed at any stage after power burn-in.

(c) Para. 9.12, Radiographic Inspection: Shall be performed in X and Z axes only.

###### 4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, constant Acceleration, shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

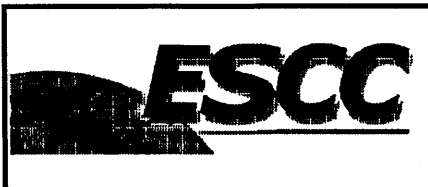
(f) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

###### 4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration, shall not be performed.

(b) Para. 9.9.2 in Electrical Measurements Subgroup: Table 3(b) measurements shall not be performed.

(c) Para. 9.13, Shock Test: Shall not be performed.



- (d) Para. 9.14, Vibration Test: Shall not be performed.
- (e) Para. 9.15, Constant Acceleration: Shall not be performed.
- (f) Para. 9.23, Special Testing: Shall not be performed.
- (g) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

#### 4.3 MECHANICAL REQUIREMENTS

##### 4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

##### 4.3.2 Weight

The maximum weight of the components specified herein shall be 0.03 grammes.

##### 4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

- (a) Condition: 'A' (Tension).
- (b) Force: 2.2N.
- (c) Duration: 5 seconds.

##### 4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

- (a) Condition: 'A' (Tension).
- (b) Bond Strengths:

Variants 01 to 05: 0.015N force minimum at pre-seal tests, 0.012N force minimum at post-seal tests.

Variants 06 to 08: 0.03N force minimum at pre-seal tests, 0.025N force minimum at post-seal tests.

##### 4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be alternatively as follows:-

- (a) Minimum acceptable die shear strengths:

Variants 01 to 06 and 08: 0.5N.

Variant 07: 0.7N.

- (b) In those cases where the clearances in the package do not allow application of the die shear force with a suitable tool, the chip shall be pushed away with a suitable tool and the die attach area inspected afterwards.

Sufficient die attach quality is achieved if objective evidence for sufficient mechanical and thermal contact is found: i.e. more than 50% semiconductor material remains.

#### 4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

##### 4.4.1 Case

The case shall be hermetically sealed and have a ceramic body.

##### 4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESCC Basic Specification No. 23500.

#### 4.5 MARKING

##### 4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

- (a) Terminal Identification.
- (b) The ESCC Component Number.
- (c) Traceability Information.

The primary package shall bear an "ESD Sensitive" label.

##### 4.5.2 Terminal Identification

Collector identification shall be as shown in Figures 2 and 3 of this specification.

##### 4.5.3 The ESCC Component Number

Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:

561100601B

Detail Specification Number \_\_\_\_\_

Type Variant (see Table 1(a)) \_\_\_\_\_

Testing Level (B or C, as applicable) \_\_\_\_\_

##### 4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

#### 4.6 ELECTRICAL MEASUREMENTS

##### 4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +25 \pm 3$  °C.

#### 4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at  $+150(+0 - 5)^{\circ}\text{C}$ , and  $-55(+5 - 0)^{\circ}\text{C}$ .

#### 4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

#### 4.7 BURN-IN TESTS

Burn-in shall be to Chart III(b) of ESCC Generic Specification No. 5010.

##### 4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $T_{\text{amb}} = +25 \pm 3^{\circ}\text{C}$ . The parameter drift values ( $\Delta$ ) applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

##### 4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for high temperature reverse bias burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for high temperature reverse bias burn-in shall be as specified in Table 5(a) of this specification.

##### 4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

##### 4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-in

The circuit for use in performing the high temperature reverse bias burn-in test is shown in Figure 5 of this specification.

##### 4.7.5 Electrical Circuit for Power Burn-in

The circuit for use in performing the power burn-in test is shown in Figure 5 of this specification.

#### 4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESCC GENERIC SPECIFICATION No. 5010)

##### 4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at  $T_{\text{amb}} = +25 \pm 3^{\circ}\text{C}$ .

##### 4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{\text{amb}} = +25 \pm 3^{\circ}\text{C}$ .

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - DC PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Collector Cut-off Current 1	$I_{CBO1}$	4(a)	$I_E = 0\text{mA}$ Variants 01, 02: $V_{CB} = 15\text{V}$ Variants 03 to 08: $V_{CB} = 20\text{V}$	-	100	$\mu\text{A}$
2	Collector Cut-off Current 2	$I_{CBO2}$	4(a)	$I_E = 0\text{mA}$ Variants 01, 02: $V_{CB} = 8\text{V}$ Variants 03 to 08: $V_{CB} = 10\text{V}$	-	50	nA
3	Emitter Cut-off Current 1	$I_{EBO1}$	4(a)	$V_{EB} = 2\text{V}, I_C = 0\text{mA}$	-	25	$\mu\text{A}$
4	Emitter Cut-off Current 2	$I_{EBO2}$	4(a)	$V_{EB} = 1\text{V}, I_C = 0\text{mA}$	-	0.5	$\mu\text{A}$
5	Collector-Emitter Cut-off Current	$I_{CEX}$	4(a)	$V_{CE} = 8\text{V}$ Variant 01: $I_B = 0.05\mu\text{A}$ Variant 02: $I_B = 0.1\mu\text{A}$ $V_{CE} = 12\text{V}$ Variant 03: $I_B = 0.1\mu\text{A}$ Variant 04: $I_B = 0.2\mu\text{A}$ Variant 05: $I_B = 0.3\mu\text{A}$ Variant 06, 08: $I_B = 0.5\mu\text{A}$ Variant 07: $I_B = 1\mu\text{A}$ (Note 1)	-	50 100 100 200 300 600 1000	$\mu\text{A}$
6	DC Forward Current Transfer Ratio	$h_{FE}$	4(a)	$V_{CE} = 1\text{V}, I_C = 0.25\text{mA}$ Variants 01, 02: $V_{CE} = 6\text{V}, I_C = 5\text{mA}$ Variant 03: Variant 04: Variant 05: $V_{CE} = 8\text{V}, I_C = 30\text{mA}$ Variant 06, 08: $V_{CE} = 5\text{V}, I_C = 50\text{mA}$ Variant 07:	30 55 55 55 50 50	175 175 170 160 175 175	
7	Base-Emitter Forward Voltage	$V_{FBE}$	4(a)	$I_C = 0\text{mA}$ Variant 01: $I_E = 3\text{mA}$ Variant 02: $I_E = 5\text{mA}$ Variant 03: $I_E = 15\text{mA}$ Variant 04: $I_E = 20\text{mA}$ Variants 05, 06, 08: $I_E = 30\text{mA}$ Variant 07: $I_E = 50\text{mA}$ (Note 2)	-	1.0	V

**NOTES:**

See Page 16.

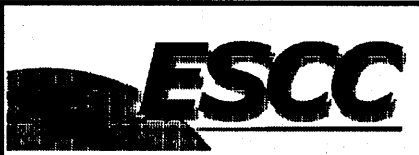
**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - AC PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
8	Collector-Base Capacitance	$C_{CB}$	4(a)	$I_E = 0\text{mA}$ , $f = 1\text{MHz}$ Variant 01: $V_{CB} = 5\text{V}$ Variant 02: $V_{CB} = 5\text{V}$ Variant 03: $V_{CB} = 10\text{V}$ Variant 04: $V_{CB} = 10\text{V}$ Variant 05: $V_{CB} = 10\text{V}$ Variant 06, 08: $V_{CB} = 10\text{V}$ Variant 07: $V_{CB} = 10\text{V}$ (Note 3)	-	0.24	pF
9	Emitter-Base Capacitance	$C_{EB}$	4(a)	$V_{EB} = 0.5\text{V}$ , $I_C = 0\text{mA}$ , $f = 1\text{MHz}$ Variant 01 Variant 02 Variant 03 Variant 04 Variant 05 Variant 06, 08 Variant 07 (Note 4)	-	0.4	pF
10	Insertion Power Gain	$ S_{21} ^2$	4(b)	$f = 2\text{GHz}$ , $V_{CE} = 5\text{V}$ Variant 01: $I_C = 2\text{mA}$ Variant 02: $I_C = 6\text{mA}$ Variant 03: $I_C = 10\text{mA}$ Variant 04: $I_C = 15\text{mA}$ Variant 05: $I_C = 20\text{mA}$ Variant 06, 08: $I_C = 40\text{mA}$ Variant 07: $I_C = 70\text{mA}$ (Notes 5 and 6)	6.5	-	dB
11	Noise Figure	NF	4(c)	$f = 2\text{GHz}$ , $V_{CE} = 5\text{V}$ Variant 01: $I_C = 2\text{mA}$ Variant 02: $I_C = 2\text{mA}$ Variant 03: $I_C = 4\text{mA}$ Variant 04: $I_C = 5\text{mA}$ Variant 05: $I_C = 8\text{mA}$ Variant 06, 08: $I_C = 15\text{mA}$ Variant 07: $I_C = 20\text{mA}$ (Notes 7 and 10)	-	3.2	dB
12	Maximum Available/Stable Gain	MAG/MSG	4(b)	$f = 2\text{GHz}$ , $V_{CE} = 5\text{V}$ Variant 01: $I_C = 2\text{mA}$ Variant 02: $I_C = 6\text{mA}$ Variant 03: $I_C = 10\text{mA}$ Variant 04: $I_C = 15\text{mA}$ Variant 05: $I_C = 20\text{mA}$ Variant 06, 08: $I_C = 40\text{mA}$ Variant 07: $I_C = 70\text{mA}$ (Notes 5 and 8)	12	-	dB

**NOTES:**

See Page 16.





**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - AC PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
13	Gain Band-Width Product	$f_T$	4(b)	f = 500MHz, $V_{CE} = 5V$ Variant 01: $I_C = 2mA$ Variant 02: $I_C = 6mA$ Variant 03: $I_C = 10mA$ Variant 04: $I_C = 15mA$ Variant 05: $I_C = 20mA$ Variant 06, 08: $I_C = 40mA$ Variant 07: $I_C = 70mA$ (Notes 5 and 9)	5.5 6.5 6.5 6.5 6.5 6.5 6	- - - - - - -	GHz
14	Output Power	$P_{OUT}$	4(b)	f = 2GHz, $V_{CE} = 5V$ Variant 05: $I_C = 30mA$ , $P_{IN} = 7dBm$ Variant 06, 08: $I_C = 50mA$ , $P_{IN} = 10dBm$ Variant 07: $I_C = 80mA$ , $P_{IN} = 15dBm$ (Notes 5 and 11)	13.5 16.5 18.5	- - -	dBm
15	1/f Noise	$F_{10Hz}$	-	f = 10Hz, $V_{CE} = 3V$ $I_C = 8mA$ , $R = 2k\Omega$ Variant 08 (Notes 12, 13)	-	300	nV/ $\sqrt{Hz}$

**NOTES**

1. This is an alternative method of establishing  $V_{(BR)CEO}$  and assures that  $V_{(BR)CEO}$  for Variants 01 and 02 is  $> 8V$  and for Variants 03 to 08 is  $> 12V$ , if the stated base current is not exceeded.
2. Pulsed measurement: Pulse Duration,  $< 1$  second. For the purpose of  $V_{FBE}$  measurement,  $I_{Bmax}$  may be exceeded during a pulsed measurement provided that the pulse length duration  $< 1$  second and  $I_C = 0mA$ .
3. The emitter is connected to the ground terminal.
4. The collector is connected to the ground terminal.
5. Measured in a  $50\Omega$  system.
6. Small signal measurement.
7. Input tuned for  $NF_{min}$ .
8. MAG if  $K \geq 1$ ; MSG if  $K < 1$ .

$$9. f_T = f \times |h_{21}|, \quad h_{21} = \frac{-2 \cdot S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} \cdot S_{21}}$$

10. LTPD15 sample testing with the maximum allowed limit reduced by 0.2dB. In case of failure, 100% testing shall be applied.
11. LTPD15 sample testing with the minimum allowed limit increased by 0.5dB. In case of failure, 100% testing shall be applied.
12. Measured using a suitable noise analyser.
13. LTPD15 per wafer, sample testing. In case of failure, 100% testing shall be applied.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE**

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
2	Collector Cut-off Current 2	$I_{CBO2}$	4(a)	$I_E = 0mA$ Variants 01, 02: $V_{CB} = 8.0V$ Variants 03 to 08: $V_{CB} = 10V$	-	10	$\mu A$

**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE**

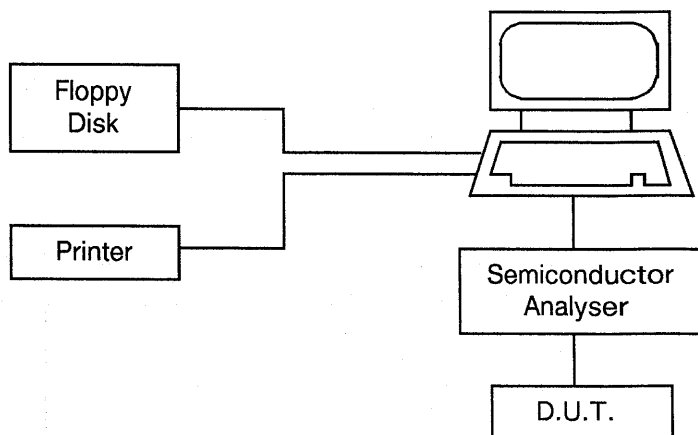
No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
6	DC Forward current Transfer Ratio (Note 1)	$h_{FE}$	4(a)	Variants 01, 02: $V_{CE} = 1V, I_C = 0.25mA$ Variants 03 to 05: $V_{CE} = 6V, I_C = 5mA$ Variant 06, 08 $V_{CE} = 8V, I_C = 30mA$ Variant 07: $V_{CE} = 5V, I_C = 50mA$	10 30 30 30	- - - -	-

**NOTES:**

1. This test shall be performed on 5 assembled samples per wafer. If a failure occurs, 100% measurements shall be performed.

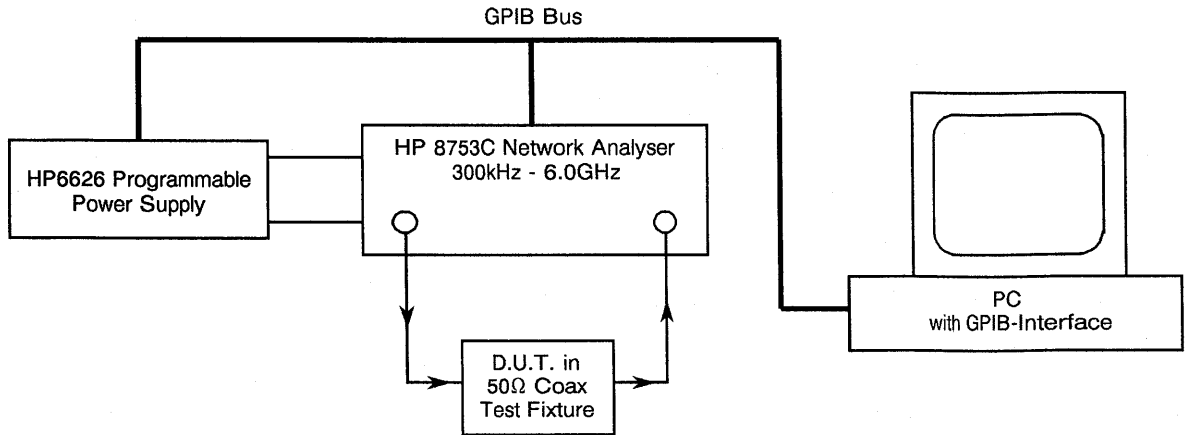
**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS**

**FIGURE 4(a) - TEST CIRCUIT FOR DC PARAMETERS**

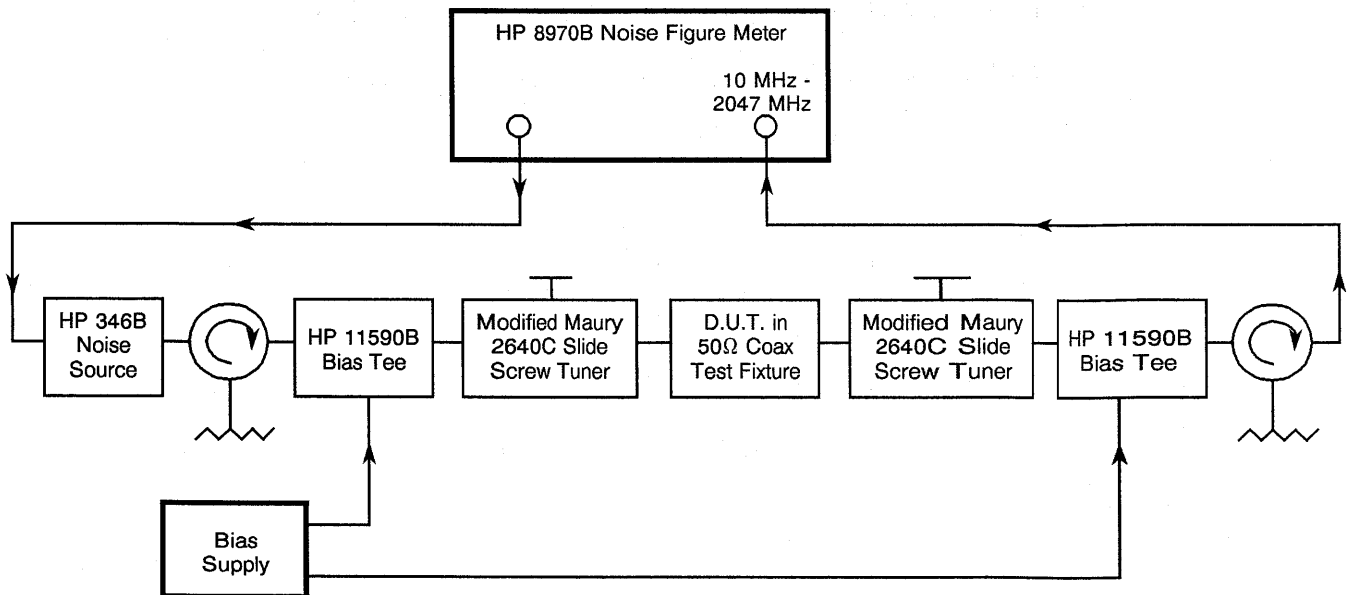


**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(b) - TEST SET-UP FOR S-PARAMETER MEASUREMENT**



**FIGURE 4(c) - TEST SET-UP FOR NOISE FIGURE MEASUREMENT**



**TABLE 4 - PARAMETER DRIFT VALUES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )	UNIT
2	Collector Cut-off Current 2	$I_{CBO2}$	As per Table 2	As per Table 2	$\pm 10$ or (2) +100 / -50	nA % (3)
4	Emitter Cut-off Current 2	$I_{EBO2}$	As per Table 2	As per Table 2	$\pm 10$ or (2) +100 / -50	nA % (3)
6	DC Forward Current Transfer Ratio	$h_{FE}$	As per Table 2	As per Table 2	$\pm 10$	% (3)
7	Base-Emitter Forward Voltage	$V_{FBE}$	As per Table 2	As per Table 2	$\pm 10$	% (3)

**NOTES**

1.  $\Delta 1 = \Delta 2$ .
2. Whichever is greater.
3. Referred to the initial measurement.

**TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN**

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Case Temperature	$T_{case}$	+ 150( + 0 - 5)	°C
2	Collector-Emitter Voltage	$V_{CES}$	Variants 01, 02: 12 Variants 03 to 08: 16	V

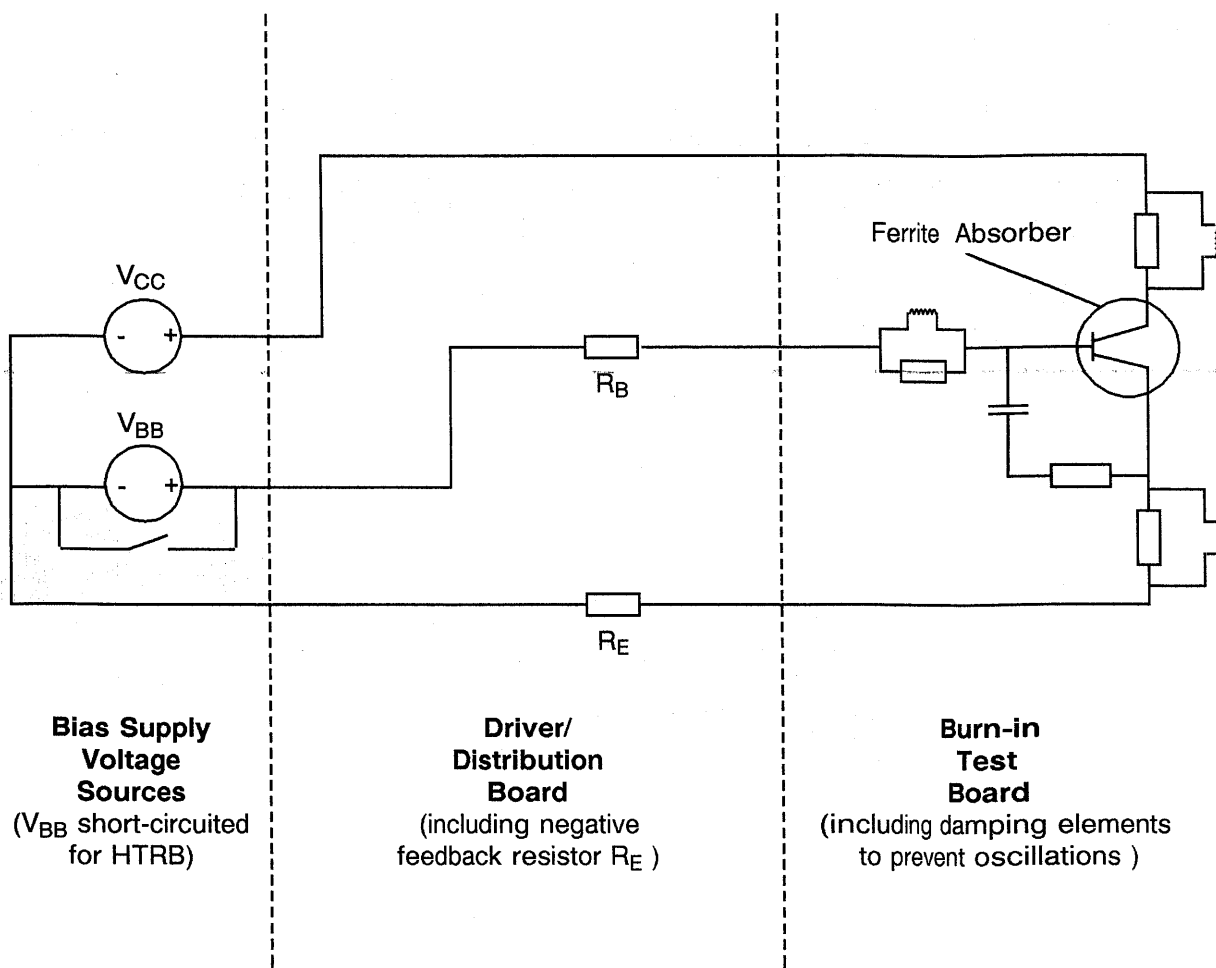
**TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS**

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	$T_{amb}$	Variants 01, 02: +175 Variant 03: +125 Variants 04 to 08: +100 (Note 1)	°C
2	Junction Temperature	$T_J$	+ 200 ( + 0 - 5)	°C
3	Power Dissipation	$P_{tot}$	Variant 01: 26.2 Variant 02: 41.7 Variant 03: 147 Variant 04: 247 Variant 05: 267 Variant 06, 08: 317 Variant 07: 350	mW
4	Collector-Emitter Voltage	$V_{CE}$	Variants 01, 02: 6.4 Variants 03 to 08: 9.6	V

**NOTES**

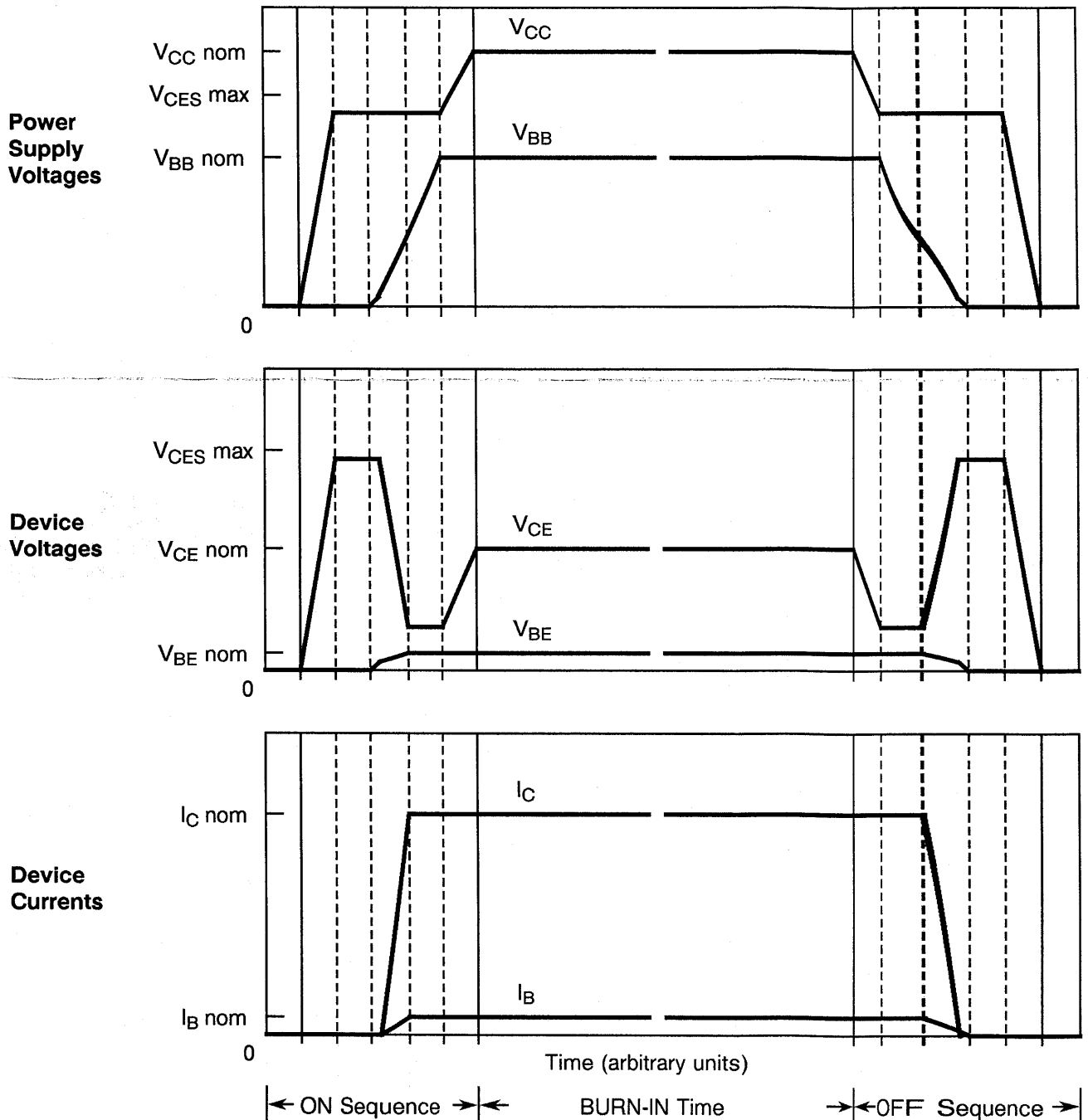
1. Because the components are mechanically clamped within the Burn-in fixture, an additional thermal resistance soldering point to ambient, e.g.  $R_{TH(S-A)} = 150^{\circ}\text{C/W}$  must be considered for the calculation of  $T_J$ .  $T_{amb}$  shall be adjusted to provide the required  $T_J$ .

**FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN**



**FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN (CONTINUED)**

TIMING SEQUENCE FOR POWER BURN-IN ON/OFF BIASING



**NOTES:**

1. The maximum ratings shall not be exceeded during the ON- and OFF-sequence. The sketched ON- and OFF-sequence timing is regarding  $V_{CC}$  performed in two steps for the case that  $V_{CC\ nom}$  ( $= V_{CE\ nom} + I_{E\ nom} \times R_E$ ) exceeds the maximum ratings for  $V_{CES}$  ( $V_{CES\ max}$ ). In case that  $V_{CC\ nom}$  does not exceed  $V_{CES\ max}$  a single step ON- and OFF-sequence may be used.



4.8.3 Conditions for Operating Life Test (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for operating life testing are specified in Table 5(b) of this specification.

4.8.4 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.





**TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS  
AND ON COMPLETION OF ENDURANCE TESTING**

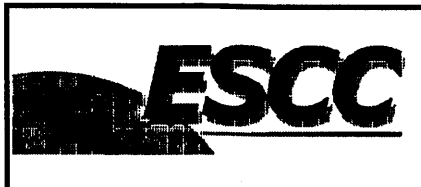
No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Collector Cut-off Current 1	$I_{CBO1}$	As per Table 2	As per Table 2	-	120	$\mu A$
2	Collector Cut-off Current 2	$I_{CBO2}$	As per Table 2	As per Table 2	-	60	nA
4	Emitter Cut-off Current 2	$I_{EBO2}$	As per Table 2	As per Table 2	-	0.6	$\mu A$
6	DC Forward Current Transfer Ratio	$h_{FE}$	As per Table 2	As per Table 2 Variants 01, 02: Variant 03: Variant 04: Variant 05: Variant 06, 08: Variant 07:	27 50 50 50 45 45	190 190 185 175 190 190	-
7	Base-Emitter Forward Voltage	$V_{FBE}$	As per Table 2	As per Table 2	-	1.1	V

**FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING**

Not applicable.

**TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING**

Not applicable.



**APPENDIX 'A'**

**AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Paras. 5.2.4 and 10.5: If Wafer Lot Acceptance Test Data is specified in the purchase order, such data will not be delivered but will be available for review at Infineon Technologies.
Para. 4.2.3	Para. 9.12, Radiographic Inspection: Exposure 100kV, duration 5 minutes may be used.
Para. 4.2.5	Para. 8.2.3(e): Witnessing of LA3 testing by the Orderer shall be limited to Electrical Measurements at Room Temperature - DC Parameters. Notification of the Orderer shall be made 5 working days before the commencement of this testing.