TRANSISTORS, MOSFET, N-CHANNEL, POWER,

BASED ON TYPE 2N6782

ESCC Detail Specification No. 5205/014

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space components
coordination group

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		P2. DCN		None
		P16. Table 2	: Limits for items 6 and 7 amended	22968
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

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APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Silicon, N-channel, enhancement-mode, MOSFET, 3.5A power transistor, based on Type 2N6782.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information applicable to the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification, of the transistors specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling.

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CHARACTERISTICS	LEAD MATERIAL AND FINISH
01	2N6782	See Table 2	D2

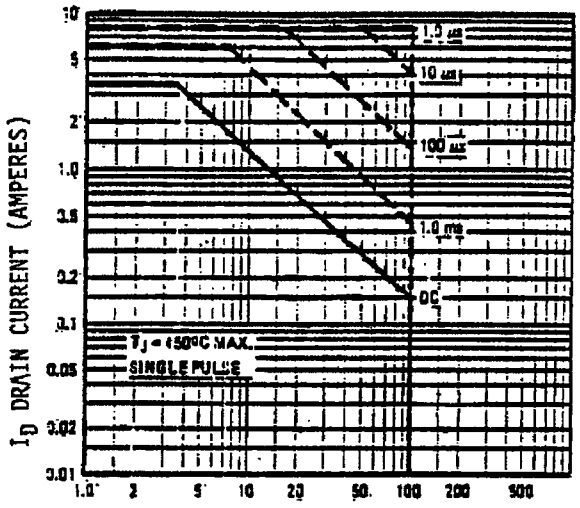
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage	V_{DS}	100	Vdc	
2	Gate-Source Voltage	V_{GS}	±20	Vdc	
3	Gate-Drain Voltage	V_{GD}	100	Vdc	
4	Drain Current (Continuous)	I_D	3.5	Adc	At T_{case} = +25°C
5	Drain Current (Continuous)	I_D	2.25	Adc	At T_{case} = +100°C
6	Drain Current (Pulsed)	I_{DM}	8.0	Adc	
7	Total Power Dissipation (see curve Figure 1)	P_{tot}	15	W	$T_{amb} \leq$ +25°C (1)
8	Operating Temperature Range	T_{op}	−55 to +150	°C	T_{amb}
9	Storage Temperature Range	T_{stg}	−55 to +150	°C	
10	Soldering Temperature	T_{sol}	+235	°C	Time: ≤10s Distance to case: ≥1.5mm

NOTES

1. Derate linearly 0.12W/°C for $T_{case} > 25°C$.

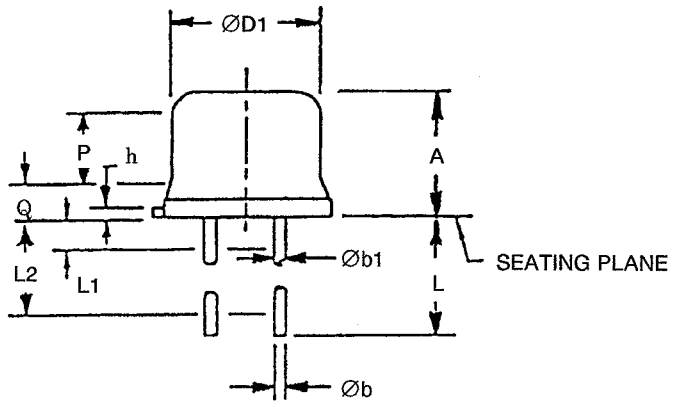
FIGURE 1 - PARAMETER DERATING INFORMATION



V_{DS} DRAIN-SOURCE VOLTAGE (VOLTS)

Maximum Safe Operating Area

FIGURE 2 - PHYSICAL DIMENSIONS



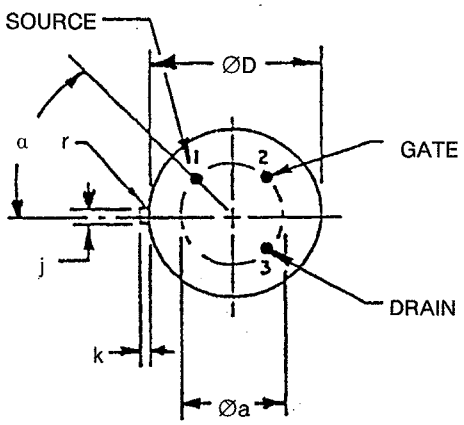


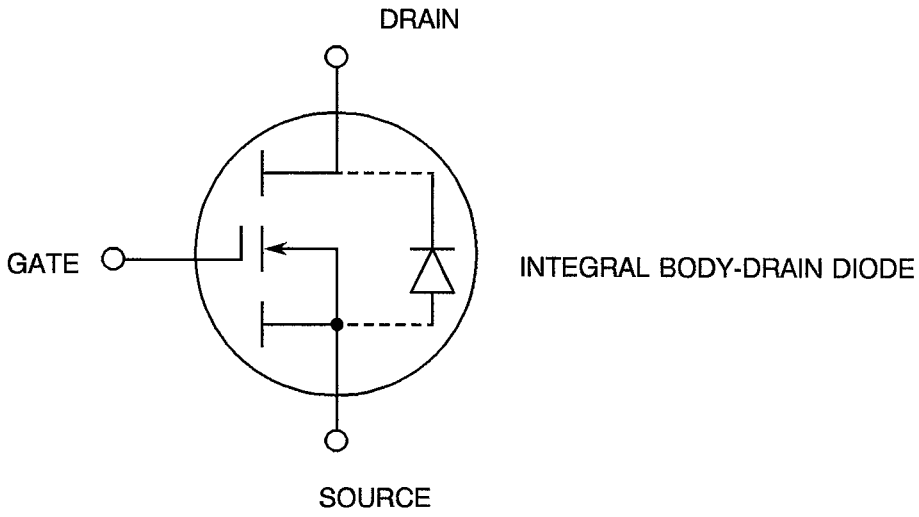
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

SYMBOL	INCHES		MILLIMETRES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.180	4.074	4.57	
Øa	0.200 Typical		0.200 Typical		1
Øb	0.016	0.021	0.41	0.53	7, 8
Øb1	0.016	0.019	0.41	0.48	7, 8
ØD	0.335	0.370	8.51	9.40	
ØD1	0.305	0.335	7.75	8.51	
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.71	0.86	2
k	0.029	0.045	0.74	1.14	3
L	0.500	0.750	12.70	19.05	7, 8
L1	-	0.050	-	1.27	7, 8
L2	0.250	-	6.35	-	7, 8
P	0.100	-	2.54	-	5
Q	-	0.050	-	1.27	4
r	-	0.010	-	0.25	9
α	45° Typical		45° Typical		6

NOTES

1. Metric equivalents are given for general information only and are based upon 1inch = 25.4mm.
2. Beyond r (radius) maximum, j shall be held for a minimum length of 0.11" (0.28mm).
3. k measured from maximum ØD.
4. Outline in this zone is not controlled.
5. ØD1 shall not vary more than 0.010" (0.25mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane 0.054" + 0.001", -0.001", -0.000" (1.37 + 0.03, -0.00 mm) below seating plane shall be within 0.007" (0.18mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gaugeing procedure shown in Figure 2.
7. Øb1 applies between L1 and L2. Øb applies between L2 and L minimum. Diameter is uncontrolled in L1 and beyond L minimum.
8. All three leads.
9. r (radius) applies to both inside corners of tab.

FIGURE 3 - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

(c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein are stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

The following deviations from ESA/SCC Generic Specification No. 5000 shall apply:-

4.2.1 Deviations from Special In-process Controls

(a) For testing levels 'B' and 'C', a Scanning Electron Microscope (SEM) inspection shall be performed on samples from each metallisation lot in accordance with ESA/SCC Basic Specification No. 21400.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Burn-in Test: The duration shall be 240 hours.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 1.1 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition : 'A' (Tension).
Applied Force : 8 Ounces.
Duration : 10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Metal case, hermetically sealed, similar to JEDEC TO-39.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

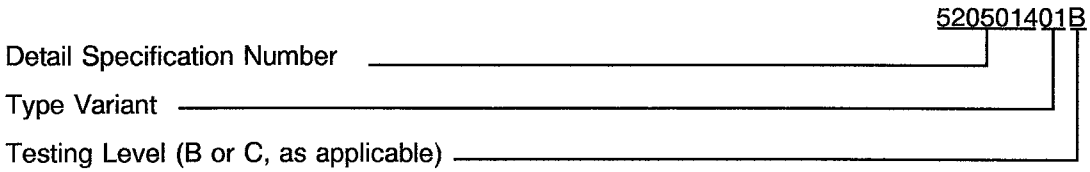
(c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) The SCC Component Number.

(b) Date Code.

(c) Serial Number

(d) Manufacturers Identification or Symbol.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Breakdown Voltage Drain-Source	B_{VDSS}	3407	$I_D = 0.25$mAdc Bias Cond. 'C' $V_{GS} = 0$V	100	-	Vdc
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.5$mAdc	2.0	4.0	Vdc
3	Gate Current	I_{GSS}	3411	$V_{GS} = 20$Vdc Bias Cond. 'C' $V_{DS} = 0$V	-	100	nAdc
4	Drain Current	I_{DSS}	3413	$V_{DS} = 100$Vdc Bias Cond. 'C' $V_{GS} = 0$V	-	0.25	mAdc
5	Drain-Source ON Resistance	$r_{DS(ON)}$	3421	$V_{GS} = 10$Vdc $I_D = 2.25$Adc Note 1	-	0.6	Ω
6	Drain-Source ON Voltage	$V_{DS(ON)}$	3421	$V_{GS} = 10$Vdc $I_D = 3.5$Adc Note 1	-	2.10	Vdc
7	Body Drain Diode Forward Voltage	V_{SD}	4011	$I_S = 3.5$Adc Note 1	0.75	1.5	Vdc

NOTES

1. Pulsed Measurement: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS (NOTE 6)	LIMITS		UNIT
					MIN	MAX	
1	Forward Transconductance	gfs	3455	V_{DS} = 5.0V I_D = 2.25Adc Note 1	1.0	3.0	S
2	Turn-on Delay Time	$t_{d(ON)}$	3459	See Figure 4(a) I_D = 2.25 Adc V_{DD} = 34Vdc	-	15	ns
3	Rise Time	t_r	3251		-	25	ns
4	Turn-on Delay Time	$t_{d(OFF)}$	3251		-	25	ns
5	Fall Time	t_f	3251		-	20	ns
6	Common Source Input Capacitance	C_{iss}	3431	V_{DS} = 25Vdc V_{GS} = 0V, f = 1.0MHz See Figure 4(b)	60	250	pF
7	Common Source Reverse Transfer Capacitance	C_{rss}	3433		7.0	25	pF
8	Common Source Output Capacitance	C_{oss}	3453		40	100	pF

NOTES

1. Pulsed Measurement: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

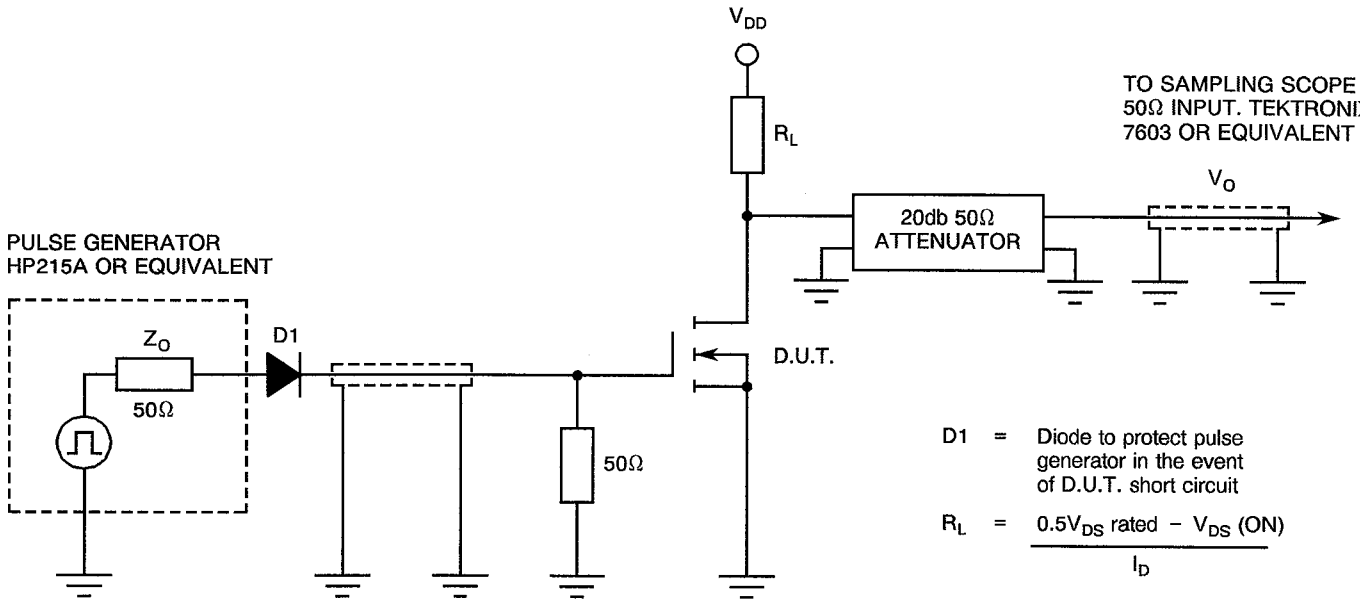
No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.5$mAdc $T_{amb} = +125°C$	1.0	-	Vdc
2	Gate Current	I_{GSS}	3411	$V_{GS} = 20$Vdc Bias Condition 'C' $V_{DS} = 0$V $T_{amb} = +125°C$	-	200	nAdc
3	Drain Current	I_{DSS}	3413	$V_{DS} = 80$Vdc Bias Cond. 'C' $T_{amb} = +125°C$ Note 1	-	1.0	mAdc
4	Drain Source ON Resistance	$r_{DS(ON)}$	3421	$V_{GS} = 10$V $I_D = 2.25$Adc $T_{amb} = +125°C$ Note 1	-	1.08	Ω
5	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.5$mAdc $T_{amb} = -55°C$	-	5.0	Vdc

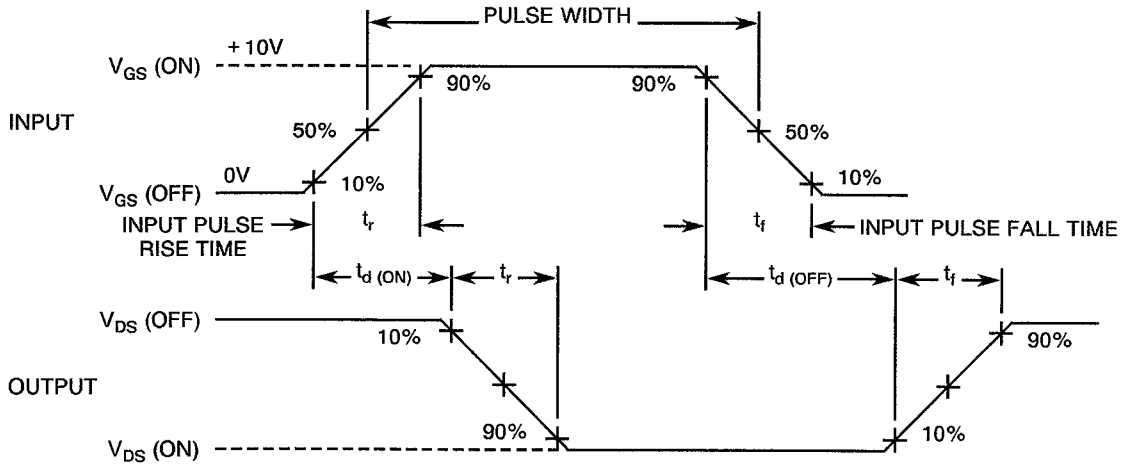
NOTES

1. Pulsed: Pulse Width ≤300μs, Duty Cycle ≤2.0%.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(a) - SWITCHING TIMES TEST CIRCUIT





NOTES

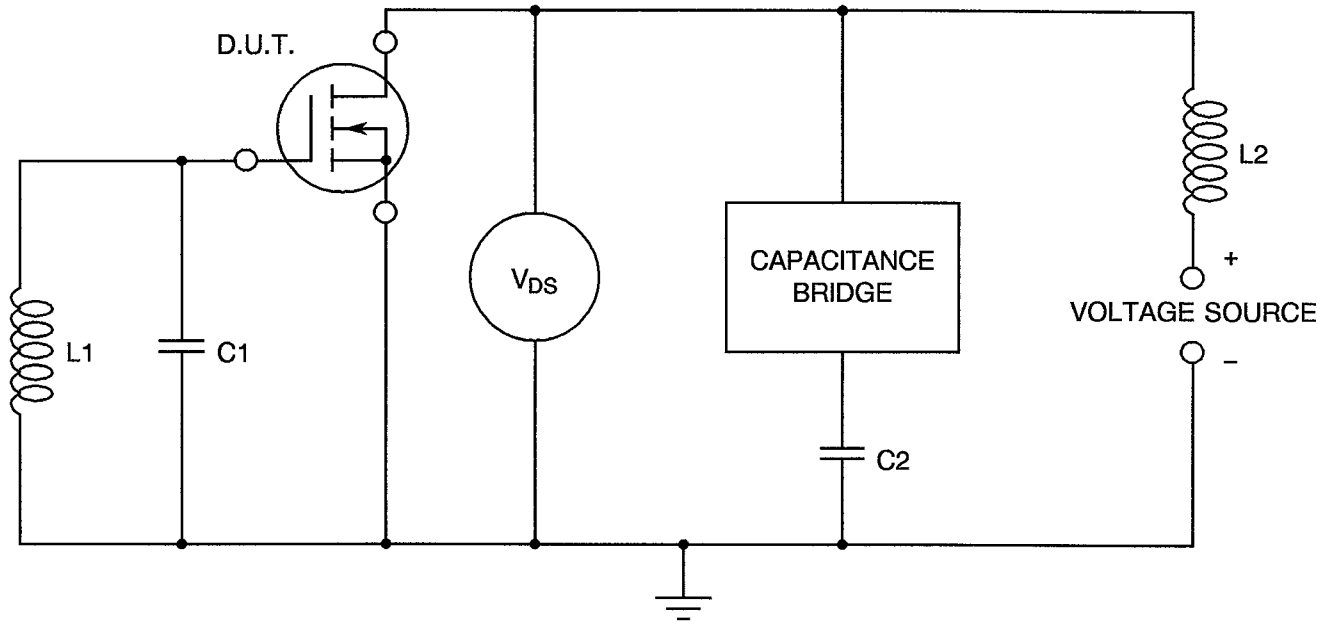
1. When measuring rise time, V_{GS} (ON) shall be as specified on the input waveform.

   When measuring fall time, V_{GS} (OFF) shall be as specified on the input waveform.

   The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - CAPACITANCE TEST CIRCUIT



Test circuit for small-signal, common-source, short-circuit, output capacitance.

PROCEDURE

The capacitors C1 and C2 shall present apparent short circuits at the test frequency. L1 and L2 shall present a high a.c. impedance at the test frequency for isolation. The bridge shall have low d.c. resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Gate Current	ΔI_{GSS}	3411	V_{GS} = 20Vdc Bias Condition 'C' V_{DS} = 0V	±20 or ±100 of initial value, whichever is greater	nAdc %
2	Drain Current	ΔI_{DSS}	3413	Vdc = 100Vdc Bias Condition 'C' V_{GS} = 0V	±25 or ±100 of initial value, whichever is greater	µAdc %
3	Drain-Source On Resistance	$\Delta r_{DS(ON)}$	3421	V_{GS} = 10Vdc I_D = 2.25Adc Note 1	±20 of initial value	%
4	Gate Threshold Voltage	$\Delta V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ I_D = 0.5mAdc	±20 of initial value	%

NOTES

1. Pulsed: Pulse Width ≤300µs, Duty Cycle ≤2.0%.

TABLE 5 - CONDITIONS FOR HTRB (PRE-CONDITIONING STRESS)

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150	°C
2	Drain-Source Voltage	V_{DS}	80	Vdc
3	Gate-Source Voltage	V_{GS}	0	Vdc
4	Duration	-	48	Hrs

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS

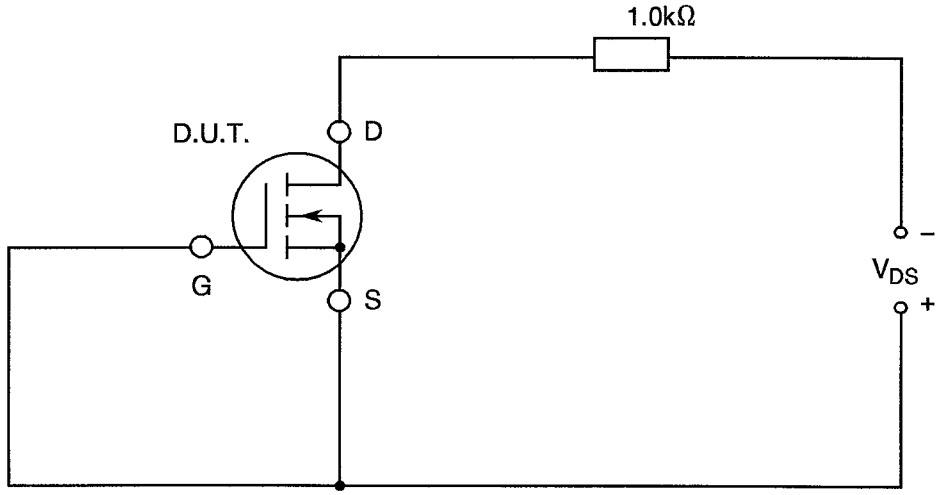


TABLE 5(b) - CONDITIONS FOR BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Junction Temperature	T_J	+140 ± 10 (1)	°C
2	Drain-Source Voltage	V_{DS}	+10 min.	Vdc
3	Gate-Source Voltage	V_{GS}	1.0 to 16	Vdc

NOTES

1. Using the circuit shown in Figure 5(b), power shall be applied to the device to achieve the specified junction temperature. The junction temperature (T_J) should be determined as follows:-

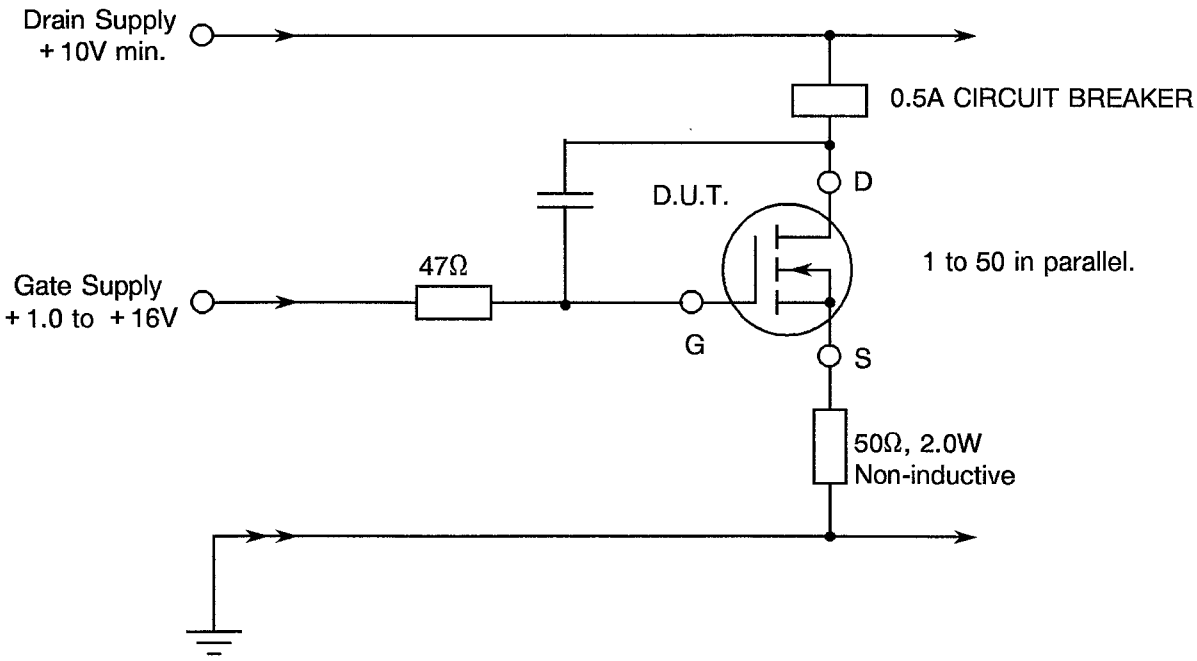
   $T_J = (P_T) \times (R_{TH(J-C)}) + T_{case}$.

   $P_T = (V_{PS}) \times (I_P)$.

   $R_{TH(J-C)}$ = 8.33°C/W.

   T_{case} = Measured value at the hottest point on the case.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 6

4.8.3 Conditions for Operation Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5(b) for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in Figure 5(b) for the burn-in test.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.5$mAdc	2.0	4.0	Vdc
2	Gate Current	I_{GSS}	3411	$V_{GS} = 20$Vdc Bias Condition 'C' $V_{DS} = 0$V	-	100	nAdc
3	Drain Current	I_{DSS}	3413	Bias Condition 'C' $V_{DS} = 100$Vdc $V_{GS} = 0$V	-	0.5	mAdc