INTEGRATED CIRCUITS, SILICON MONOLITHIC,

HCMOS 8-BIT ADDRESSABLE LATCHES

BASED ON TYPE 54HC259

ESCC Detail Specification No. 9203/073

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Pages 1 to 40

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ESA/SCC Detail Specification No. 9203/073

space components
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE		Approved DCR No.
		Reference	Item	
		This Issue supersedes Issue 1 and incorporates all modifications agreed on the basis of the following DCR:-		
		Cover Page	Page Contents amended.	221149
		DCN		None
		Table 1(a)	Variants 01 to 05 deleted.	221149
			Variants 06 to 09, Figures amended.	221149
		Figure 2(a)	Figure deleted.	221149
		Figure 2(b)	Figure deleted.	221149
		Figure 2(c)	Figure deleted.	221149
		Figure 2(d)	Figure 2(d) amended to 2(a).	221149
		Figure 2(e)	Figure 2(e) amended to 2(b).	221149
		Figure 2(f)	Figure 2(f) amended to 2(c).	221149
		Notes to Figures	Title amended.	221149
			Note 1 amended.	221149
		Figure 3(e)	Variants 01 to 05, Networks deleted.	221149
		Para. 4.4.2	Lead Finish, Types amended.	221149
		Para. 4.5.2	Lead identification figures amended.	221149
		Para. 4.5.3	Type Variant amended.	221149
		Table 2	Nos. 4 to 5 corrected to "4 to 12".	221149
			Following Nos. incremented by 7.	221149
		Table 3	Nos. 4 to 5 corrected to "4 to 12".	221149
			Following Nos. incremented by 7.	221149
		Figure 4(a)	Pattern Nos. added.	221149
		Table 4	Nos. 4 to 5 corrected to "4 to 12".	221149
			Following Nos. incremented by 7.	221149
		Table 6	Nos. 4 to 5 corrected to "4 to 12".	221149
			Following Nos. incremented by 7.	221149
		Table 7	Nos. 4 to 5 corrected to "4 to 12".	221149
			Following Nos. incremented by 7.	221149
		Appendix 'B'	Deleted.	221149
'A'	Dec. '01	P1. Cover page	Page count amended	221603
		P2. DCN		None
		P4. T of C	Appendix 'B' and Deviation added	221603
		P5. Para. 1.3	New sentence added	221603
		P6. Table 1(a)	New Variants 10 and 11 added	221564
		P10. Notes to Figures	Title amended to read 2(a) to 2(d)	221564
			Note 9 text amended to include SO	221564
		P10A. Figure 2(d)	New Figure added	221564
		P11. Figure 3(a)	Titles amended to include SO	221564
			Text amended to include SO	221564
		P15. Para. 4.3.2	Text amended to include SO	221564
		Para. 4.4.2	New sentence inserted after 'No. 23500'	221564
		Para. 4.5.2	Text amended to include SO packages	221564
		P40. Appendix 'B'	New Page and Deviation added	221603

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TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, high speed CMOS 8-bit Addressable Latches having fully buffered outputs, based on type 54HC259. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESA/SCC Generic Specification.

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are Categorised as Class 2 with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.11 INPUT AND OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
06	FLAT	2(a)	G4
07	D.I.L.	2(b)	G4
08	CHIP CARRIER	2(c)	7
09	CHIP CARRIER	2(c)	4
10	SO CERAMIC	2(d)	G2
11	SO CERAMIC	2(d)	G4

TABLE 1(b) - MAXIMUM RATINGS

NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{DD}	-0.5 to +7.0	V	Note 1
2	Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	Notes 1, 2
3	Output Voltage	V_{OUT}	-0.5 to V_{DD} +0.5	V	Notes 1, 3
4	Device Dissipation (Continuous)	P_D	300	mW	Note 4
5	Supply Current	I_{DDop}	50	mA	
6	Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	-65 to +150	°C	
8	Soldering Temperature For FP and DIP For CCP	T_{sol}	+265 +245	°C	Note 5 Note 6

NOTES

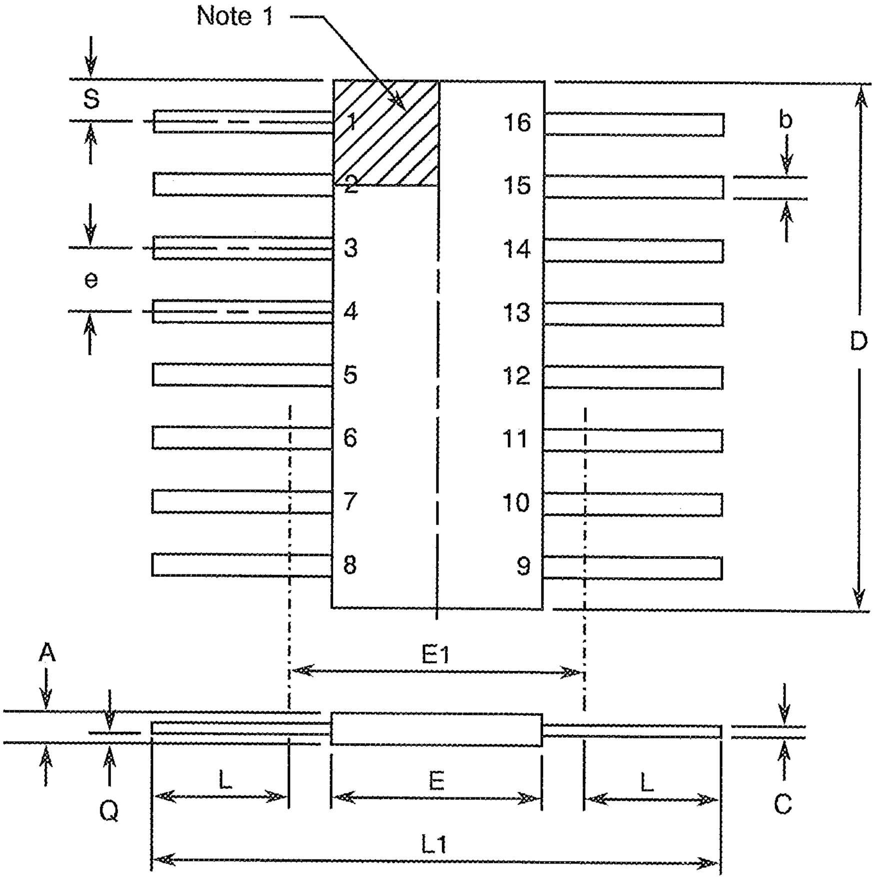
1. Device is functional for $2.0V \leq V_{DD} \leq 6.0V$.
2. Input current limited to $I_{IC} = \pm 20mA$.
3. Output current limited to $I_{OUT} = \pm 25mA$.
4. The maximum device dissipation is determined by I_{DDop} max. (50mA) x 6.0V.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 16-PIN

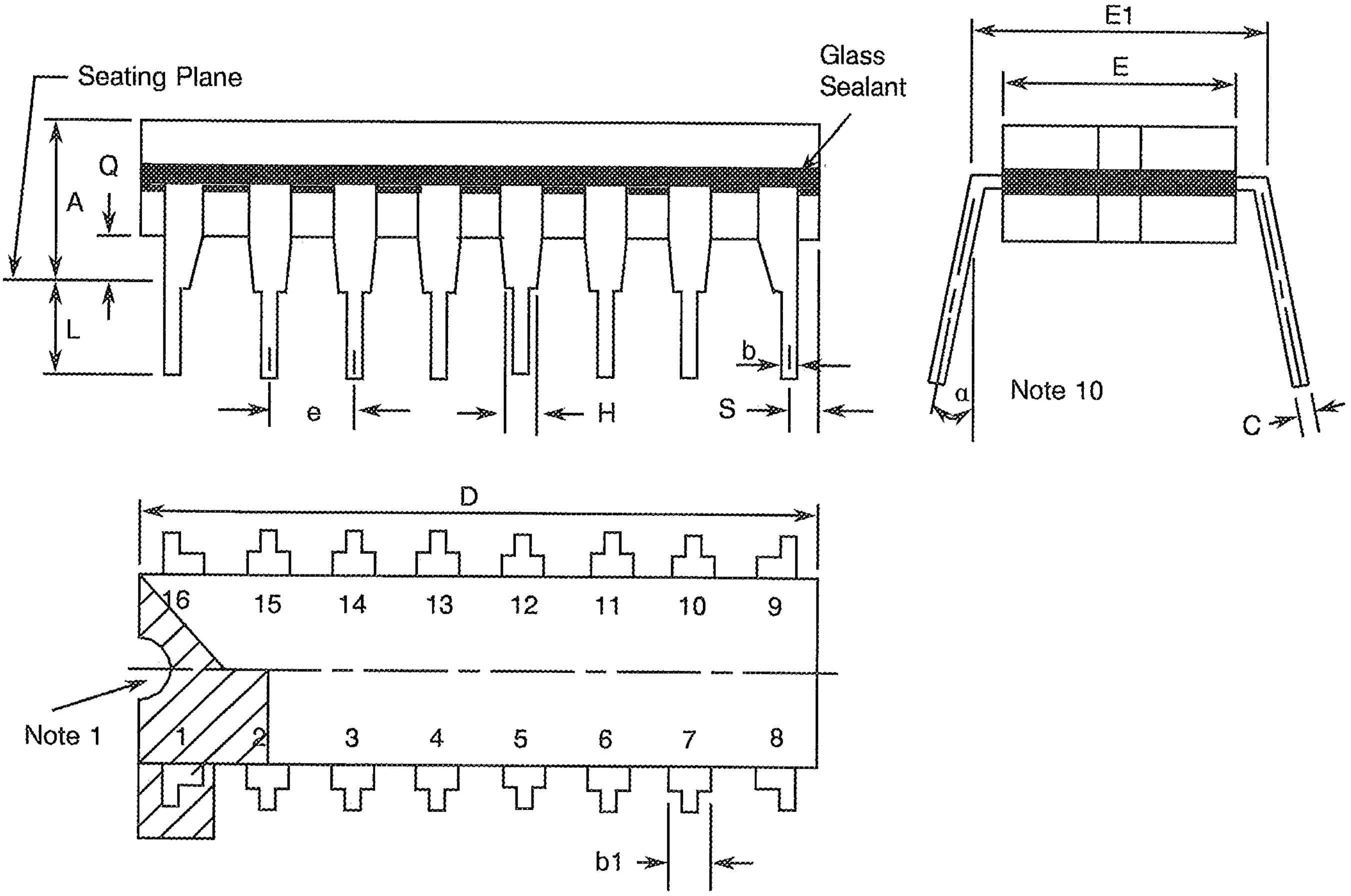


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.27	2.03	
b	0.38	0.56	8
C	0.08	0.23	8
D	9.42	10.16	4
E	6.27	7.24	
E1	7.00 TYPICAL		4
e	1.27 TYPICAL		5, 9
L	7.87	8.89	8
L1	23.88	24.38	
Q	0.51	1.02	2
S	0.25	0.64	7

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 16-PIN

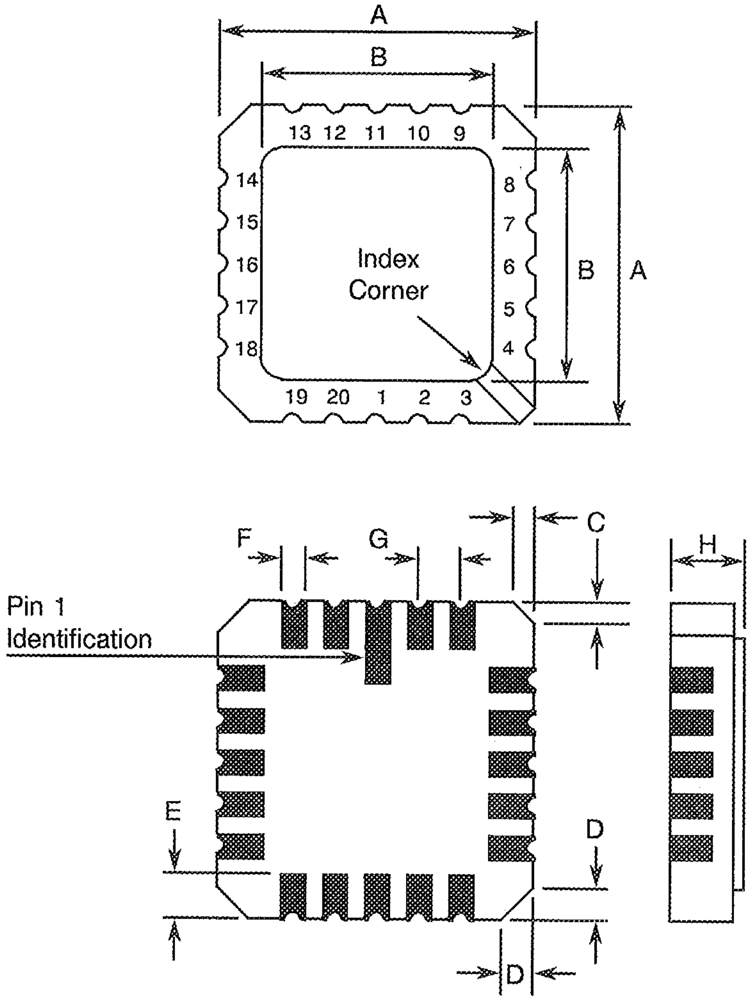


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.66	8
b1	-	1.78	8
C	0.20	0.44	8
D	19.18	19.94	4
E	6.22	7.62	4
E1	7.37	8.13	
e	2.54 TYPICAL		6, 9
F	1.27 TYPICAL		
H	0.76	-	
L	3.30	5.08	8
Q	0.51	-	3
S	0.38	1.27	7
α	0°	15°	10

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE), 20-TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	8.69	9.09	
B	7.80	9.09	
C	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

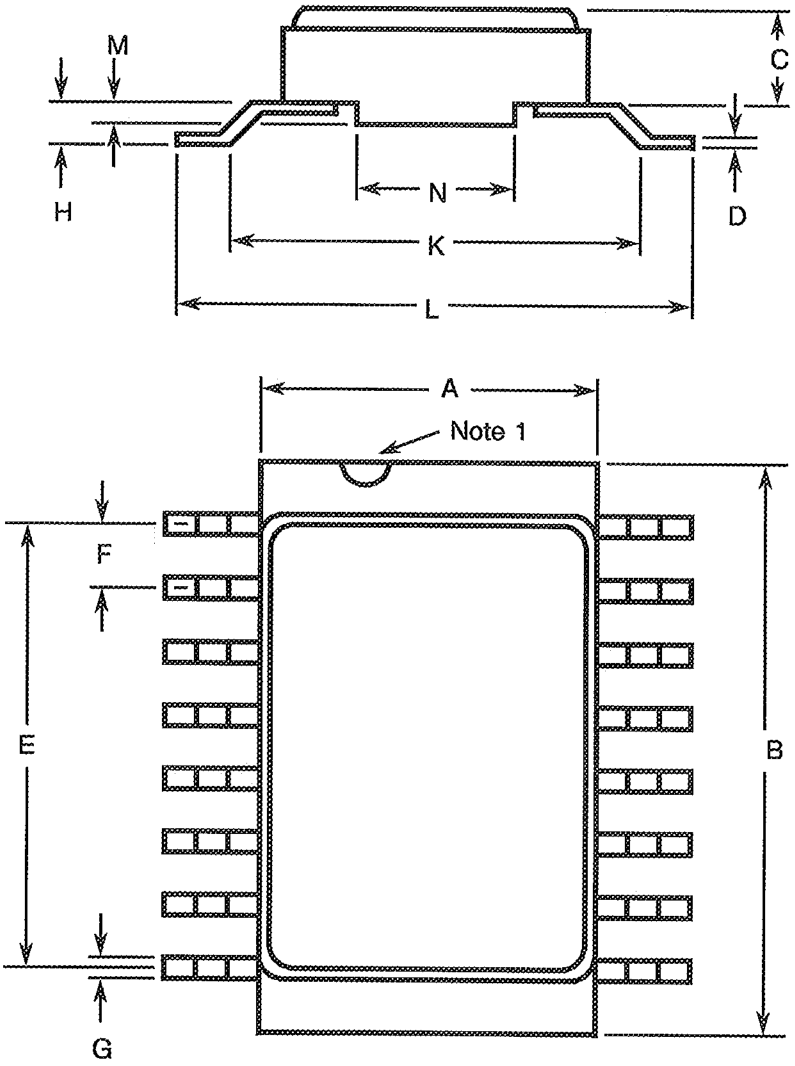
NOTES TO FIGURES 2(a) TO 2(d) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(c).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. The dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of it's true longitudinal position relative to Pin 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of it's true longitudinal position relative to Pin 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 14 spaces for flat, SO and dual-in-line packages.

   16 spaces for chip carrier packages.
10. Lead centreline when α is 0°.
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SMALL OUTLINE CERAMIC PACKAGE, 16-PIN

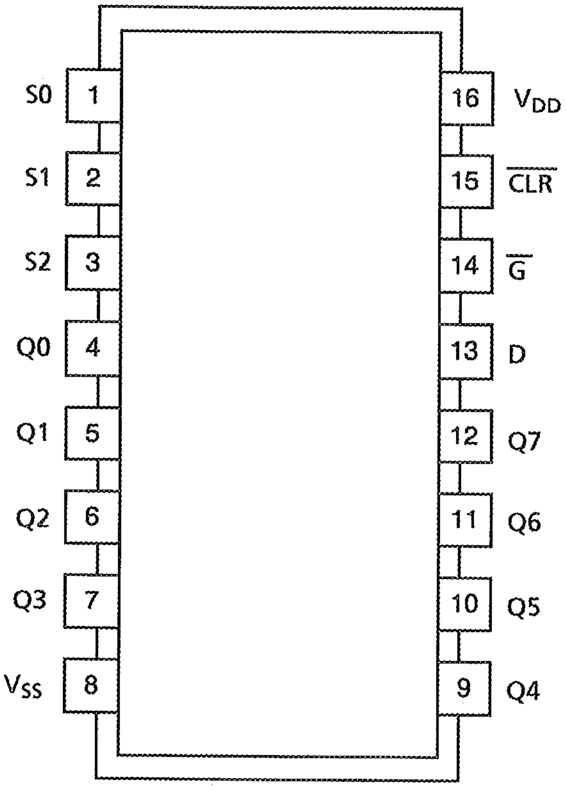


SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.102	0.152	8
E	8.76	9.01	
F	1.27 TYPICAL		5, 9
G	0.38	0.48	8
H	0.60	0.90	8
K	9.00 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

NOTES: See Page 10.

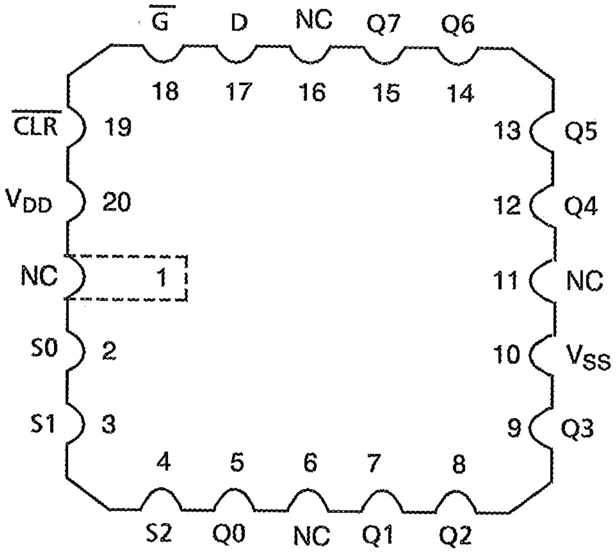
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE, SO AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

FIGURE 3(b) - TRUTH TABLE

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{G}}$			
H	L	D	Qi0	Addressable Latch
H	H	Qi0	Qi0	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

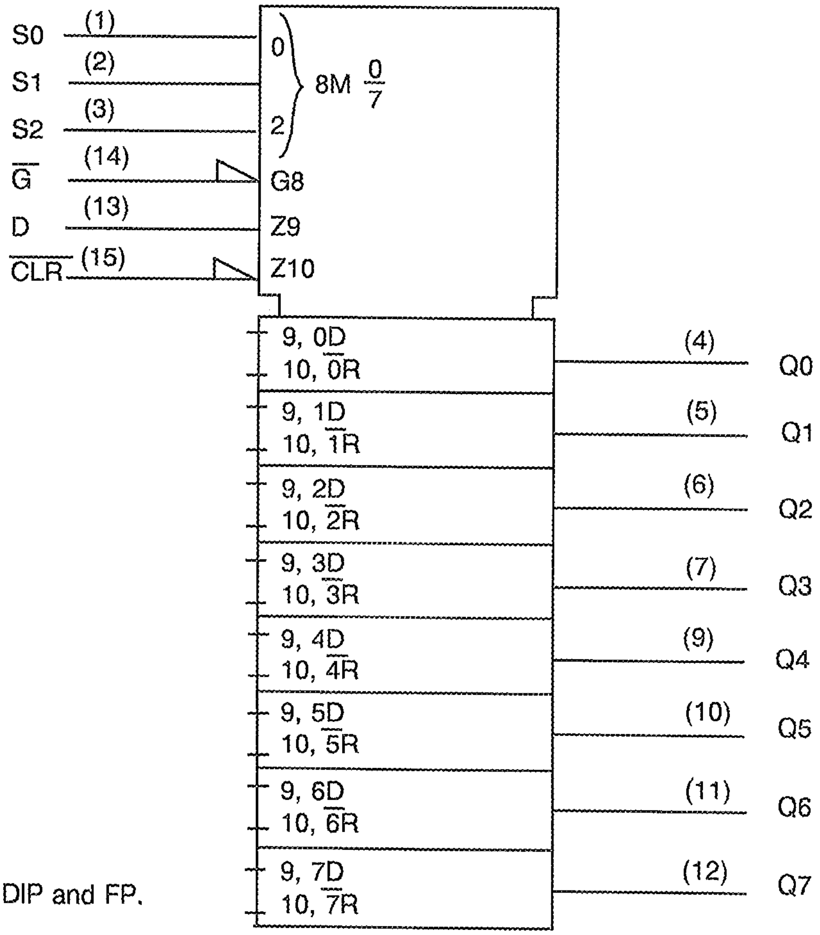
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

NOTES
1. Logic Level Definitions: L = Low Level, H = High Level.
2. D = the level at the Data Input.
3. Qi0 = The level before the indicated steady-state input conditions were established (i = 0, 1...7).

FIGURE 3(c) - CIRCUIT SCHEMATIC

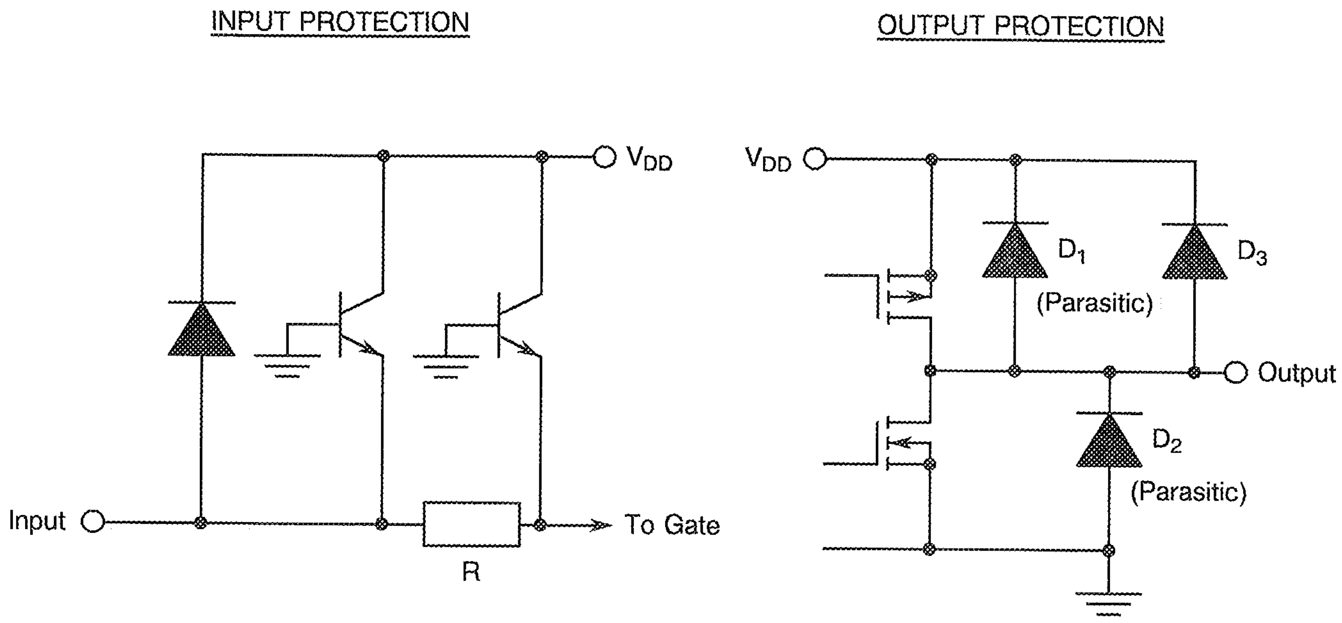
Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



NOTES
1. Pin numbers shown are for DIP and FP.

FIGURE 3(e) - INPUT AND OUTPUT PROTECTION NETWORKS


INPUT PROTECTION

OUTPUT PROTECTION

VARIANTS 06 TO 09

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:

V_{IC} = Input Clamp Voltage.

I_{IC} = Input Clamp Diode Current.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalant to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during irradiation qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on an irradiation lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

None.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes for the dual-in-line package, 0.7 grammes for the flat and SO packages and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For SO ceramic packages, the material shall be Type 'G' with either Type '2' or Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line, flat and SO packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

920307306 BF

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125$ (+0 -5) °C and -55 (+5 -0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to H.T.R.B. and Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

For H.T.R.B. Burn-in, the parameter drift values (Δ) shall be applied before the N-Channel (0 hours) and after the P-Channel (144 hours) burn-in.

4.7.2 Conditions for H.T.R.B. and Power Burn-in

The requirements for H.T.R.B. and Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Power Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

4.7.3 Electrical Circuits for H.T.R.B. and Power Burn-in

Circuits for use in performing the H.T.R.B. and Power Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.3V, V_{IH} = 1.5V V_{DD} = 2.0V, V_{SS} = 0V t_r < 1.0µs, f = 10kHz (min) Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.9V, V_{IH} = 3.15V V_{DD} = 4.5V, V_{SS} = 0V t_r = t_f < 500ns f = 10kHz (min) Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 1.2V, V_{IH} = 4.2V V_{DD} = 6.0V, V_{SS} = 0V t_r = t_f < 400ns f = 10kHz (min) Note 1	-	-	-
4 to 12	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 6.0V V_{DD} = 6.0V, V_{SS} = 0V All Outputs Open (Pin D/F 16) (Pin C 20)	-	0.4	µA
13 to 18	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 6.0V V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-	-50	nA
19 to 24	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 6.0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-	50	nA

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
25 to 32	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	V_{IL} = 0.3V, V_{IH} = 1.5V I_{OL} = 20µA V_{DD} = 2.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
33 to 40	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OL} = 20µA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
41 to 48	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OL} = 20µA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
49 to 56	Output Voltage Low Level 4	V_{OL4}	3007	4(d)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.26	V
57 to 64	Output Voltage Low Level 5	V_{OL5}	3007	4(d)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OL} = 5.2mA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.26	V
65 to 72	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{IL} = 0.3V, V_{IH} = 1.5V I_{OH} = −20µA V_{DD} = 2.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	1.9	-	V

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
73 to 80	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OH} = −20μA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	4.4	-	V
81 to 88	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OH} = −20μA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	5.9	-	V
89 to 96	Output Voltage High Level 4	V_{OH4}	3006	4(e)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OH} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	3.98	-	V
97 to 104	Output Voltage High Level 5	V_{OH5}	3006	4(e)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OH} = −5.2mA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	5.48	-	V
105	Threshold Voltage N-Channel	V_{THN}	-	4(f)	S0 Input at Ground All Other Inputs: V_{IN} = 5.0V V_{DD} = 5.0V, I_{SS} = -10μA (Pin D/F 8) (Pin C 10)	-0.45	-1.45	V
106	Threshold Voltage P-Channel	V_{THP}	-	4(g)	S0 Input at Ground All Other Inputs: V_{IN} = -5.0Vdc V_{SS} = -5.0V, I_{DD} = 10μA (Pin D/F 16) (Pin C 20)	0.45	1.35	V

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
107 to 112	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(h)	I_{IN} (Under Test) = -0.1mA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-0.4	-0.9	V
113 to 118	Input ClampVoltage (to V_{DD})	V_{IC2}	-	4(h)	I_{IN} (Under Test) = 0.1mA V_{DD} = 0V, V_{SS} = Open, All Other Pins Open (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	0.4	0.9	V

NOTES

1. Maximum time to output comparator strobe 30µs.
2. Guaranteed but not tested.
3. Measurements shall be performed on a 100% basis go-no-go, with read and record on a sample basis, LTPD7 (32 pieces) after Chart III (Burn-in) Tests.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
119 to 124	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) =0Vdc V_{DD} = V_{SS} = 0V Note 2 (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-	10	pF
125	Propagation Delay Low to High, (D to Q0)	t_{PLH1}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b). V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 13 to 4 Pins C 17 to 5	-	26	ns
126	Propagation Delay High to Low, (D to Q0)	t_{PHL1}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 13 to 4 Pins C 17 to 5	-	26	ns
127	Propagation Delay Low to High, (S0 to Q0)	t_{PLH2}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 1 to 4 Pins C 1 to 5	-	40	ns
128	Propagation Delay High to Low, (S0 to Q0)	t_{PHL2}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 1 to 4 Pins C 1 to 5	-	40	ns

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
129	Propagation Delay Low to High, ($\overline{G}$ to Q0)	t_{PLH3}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 14 to 4 Pins C 18 to 5	-	34	ns
130	Propagation Delay High to Low, ($\overline{G}$ to Q0)	t_{PHL3}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 14 to 4 Pins C 18 to 5	-	34	ns
131	Propagation Delay High to Low, ($\overline{CLR}$ to Q0)	t_{PHL4}	3003	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 Pins D/F 15 to 4 Pins C 19 to 4	-	38	ns
132	Transition Time Low to High	t_{TLH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin D/F 4) (Pin C 5)	-	15	ns
133	Transition Time High to Low	t_{THL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Figure 3(b) V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin D/F 4) (Pin C 5)	-	15	ns

NOTES: See Page 20.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.3V, V_{IH} = 1.5V V_{DD} = 2.0V, V_{SS} = 0V t_r < 1.0µs, f = 10kHz (min) Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.9V, V_{IH} = 3.15V V_{DD} = 4.5V, V_{SS} = 0V t_r = t_f < 500ns f = 10kHz (min) Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 1.2V, V_{IH} = 4.2V V_{DD} = 6.0V, V_{SS} = 0V t_r = t_f < 400ns f = 10kHz (min) Note 1	-	-	-
4 to 12	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 6.0V V_{DD} = 6.0V, V_{SS} = 0V All Outputs Open (Pin D/F 16) (Pin C 20)	-	8.0	µA
13 to 18	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 6.0V V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-	-1.0	µA
19 to 24	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 6.0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-	1.0	µA

NOTES: See Page 20.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
25 to 32	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	V_{IL} = 0.3V, V_{IH} = 1.5V I_{OL} = 20µA V_{DD} = 2.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
33 to 40	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OL} = 20µA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
41 to 48	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OL} = 20µA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.1	V
49 to 56	Output Voltage Low Level 4	V_{OL4}	3007	4(d)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.4	V
57 to 64	Output Voltage Low Level 5	V_{OL5}	3007	4(d)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OL} = 5.2mA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	-	0.4	V
65 to 72	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{IL} = 0.3V, V_{IH} = 1.5V I_{OH} = −20µA V_{DD} = 2.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	1.9	-	V

NOTES: See Page 20.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
73 to 80	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OH} = −20µA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	4.4	-	V
81 to 88	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OH} = −20µA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	5.9	-	V
89 to 96	Output Voltage High Level 4	V_{OH4}	3006	4(e)	V_{IL} = 0.9V, V_{IH} = 3.15V I_{OH} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	3.7	-	V
97 to 104	Output Voltage High Level 5	V_{OH5}	3006	4(e)	V_{IL} = 1.2V, V_{IH} = 4.2V I_{OH} = −5.2mA V_{DD} = 6.0V, V_{SS} = 0V (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	5.2	-	V
107 to 112	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(h)	I_{IN} (Under Test) = -0.1mA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	-0.1	-1.2	V
113 to 118	Input ClampVoltage (to V_{DD})	V_{IC2}	-	4(h)	I_{IN} (Under Test) = 0.1mA V_{DD} = 0V, V_{SS} = Open, All Other Pins Open (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	0.1	1.2	V

NOTES: See Page 20.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

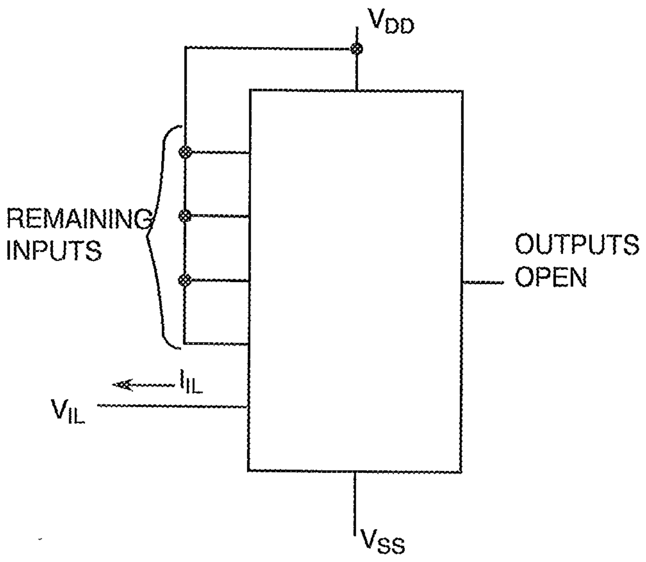
FIGURE 4(a) - QUIESCENT CURRENT TEST TABLE

PATTERN NO.	INPUTS						OUTPUTS								PACKAGE	D.C. SUPPLY	
	1 2	2 3	3 4	13 17	14 18	15 19	4 5	5 7	6 8	7 9	9 12	10 13	11 14	12 15	DIL, FP CCP	8 10	16 20
1	0	0	0	0	0	0	OPEN									V_{SS}	V_{DD}
2	0	0	0	1	0	1	OPEN										
3	1	0	0	1	0	1	OPEN										
4	0	1	0	1	0	1	OPEN										
5	1	1	0	1	0	1	OPEN										
6	0	0	1	1	0	1	OPEN										
7	1	0	1	1	0	1	OPEN										
8	0	1	1	1	0	1	OPEN										
9	1	1	1	1	0	1	OPEN										

NOTES

1. Figure 4(a) illustrates one series of test patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: 1 = V_{IH} = V_{DD}, 0 = V_{IL} = V_{SS}.

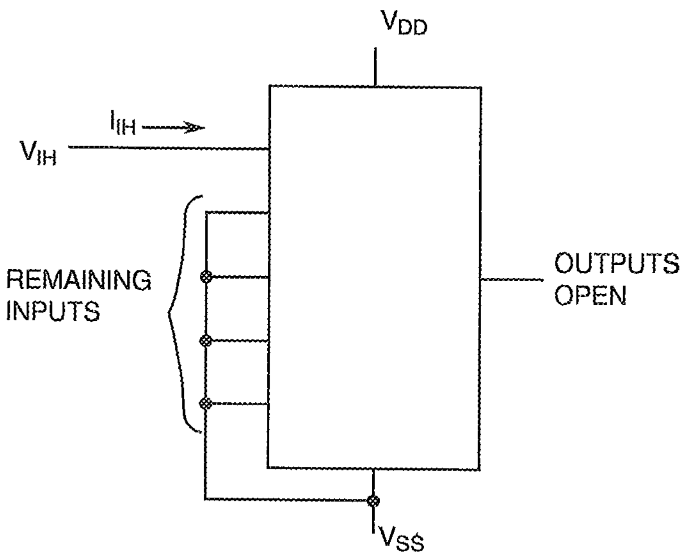
FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES

1. Each input to be tested separately

FIGURE 4(c) - INPUT CURRENT HIGH LEVEL

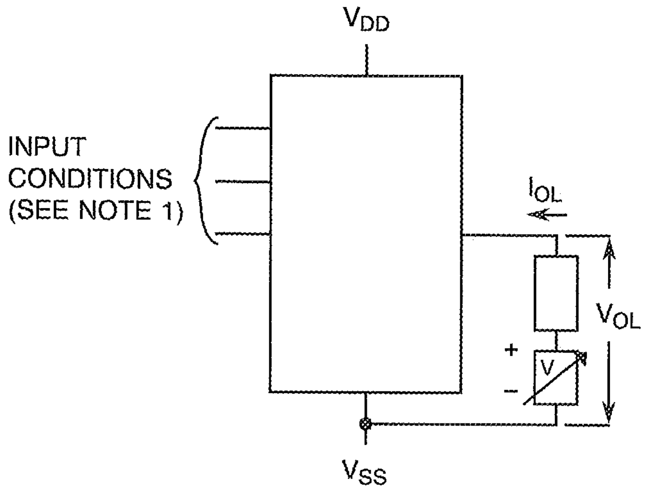


NOTES

1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

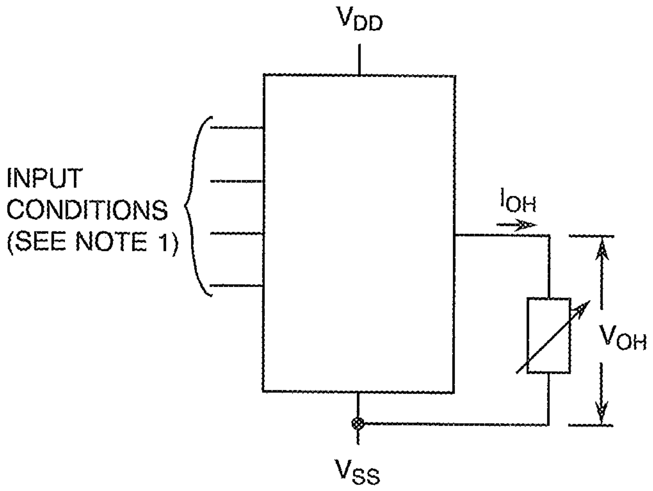
FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



NOTES

1. $V_{IN} = V_{IL}$ (max.) and/or V_{IH} (min.) as per Truth Table to give V_{OL}.
2. Each output to be tested separately.

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



NOTES

1. $V_{IN} = V_{IL}$ (max.) and/or V_{IH} (min.) as per Truth Table to give V_{OH}.
2. Each output to be tested separately.

FIGURE 4(f) - THRESHOLD VOLTAGE N-CHANNEL

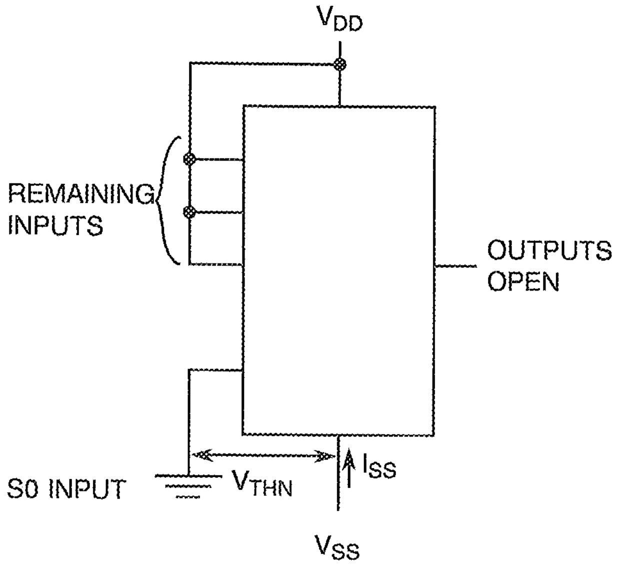


FIGURE 4(g) - THRESHOLD VOLTAGE P-CHANNEL

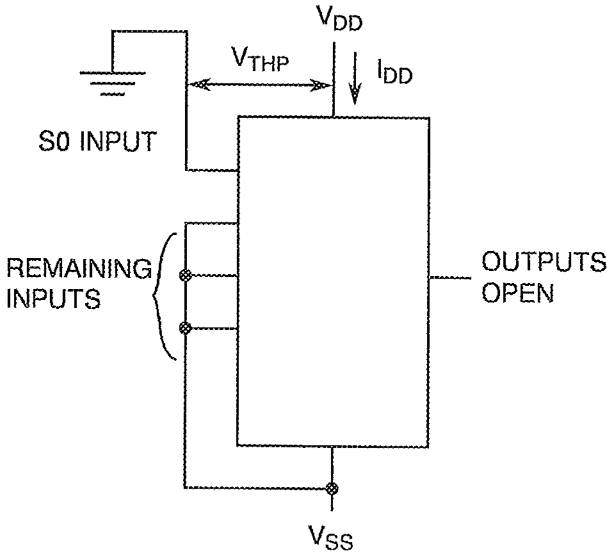
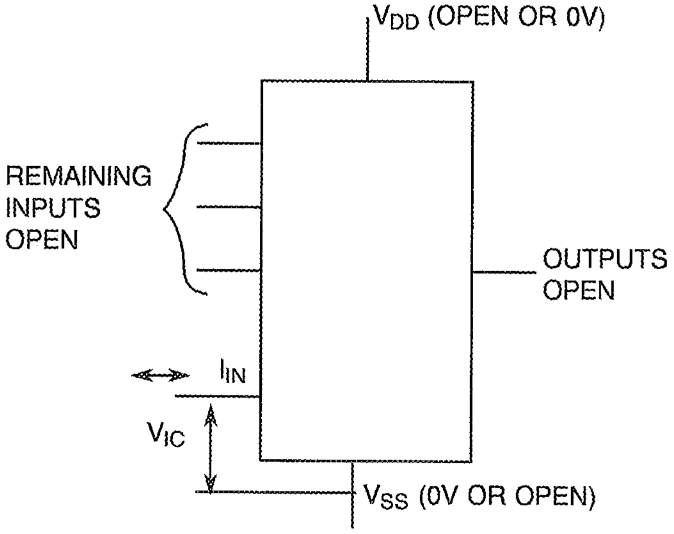


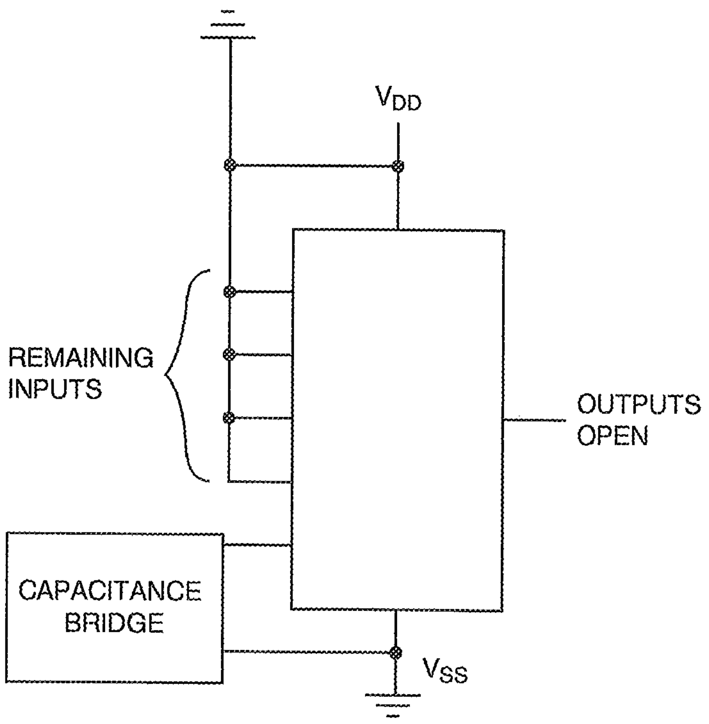
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - INPUT CLAMP VOLTAGE



NOTES 1. Each input to be tested separately.

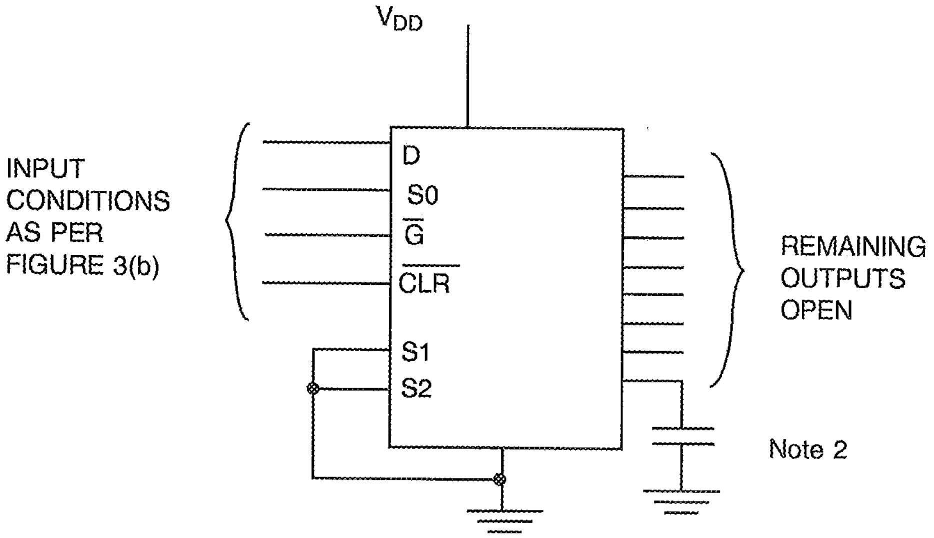
FIGURE 4(i) - INPUT CAPACITANCE



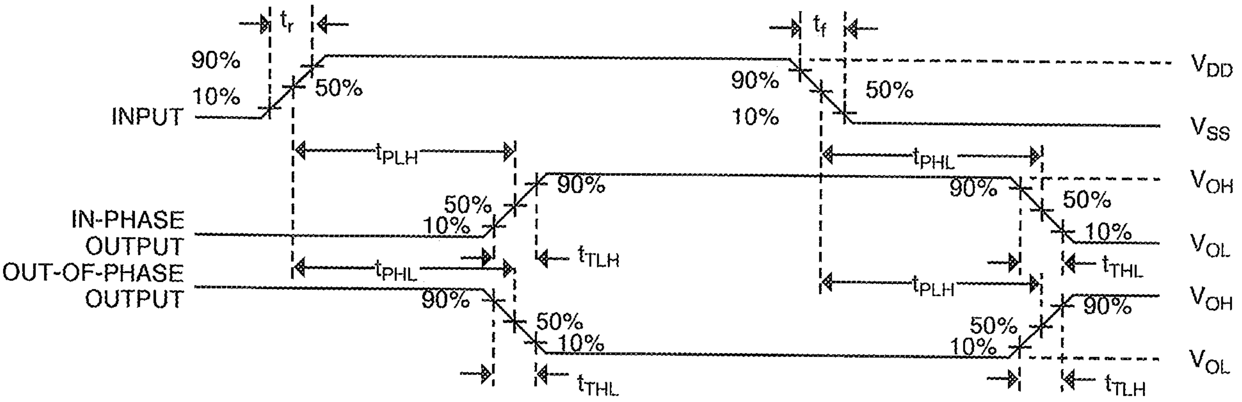
NOTES 1. Each input to be tested separately.
2. f = 100KHz to 1MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY AND TRANSITION TIME



VOLTAGE WAVEFORMS



NOTES

1. Pulse Generator - V_P = 0 to V_{DD}, t_r and $t_f \leq 6$ns, f = 1.0MHz minimum, 50% Duty Cycle, $Z_{OUT} = 50\Omega$.
2. C_L = 50pF ± 5% including scope, wiring and stray capacitance without package in test fixture.

TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
4 to 12	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	± 120	nA
13 to 18	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 20	nA
19 to 24	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	± 20	nA
49 to 56	Output Voltage Low Level 4	V_{OL4}	As per Table 2	As per Table 2	± 0.026	V
89 to 96	Output Voltage High Level 4	V_{OH4}	As per Table 2	As per Table 2	± 0.2	V
105	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	± 0.3	V
106	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	± 0.3	V

TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	V_{OUT}	Open or V_{SS}	-
3	Inputs - (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	V_{IN}	V_{SS}	V
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V_{DD}	6.0(+0-0.5)	V
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	V_{SS}	0	V
6	Duration	t	72	Hours

NOTES

1. Input Protection Resistor = 680Ω min. to 47kΩ max.
2. Output Load = 1kΩmin. to 10kΩ max.

TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	V_{OUT}	Open or V_{DD}	-
3	Inputs - (Pins D/F 1-2-3-13-14-15) (Pins C 2-3-4-17-18-19)	V_{IN}	V_{DD}	V
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V_{DD}	6.0(+0-0.5)	V
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	V_{SS}	0	V
6	Duration	t	72	Hours

NOTES

1. Input Protection Resistor = 680Ω min. to 47kΩ max.
2. Output Load = 1kΩ min. to 10kΩ max.

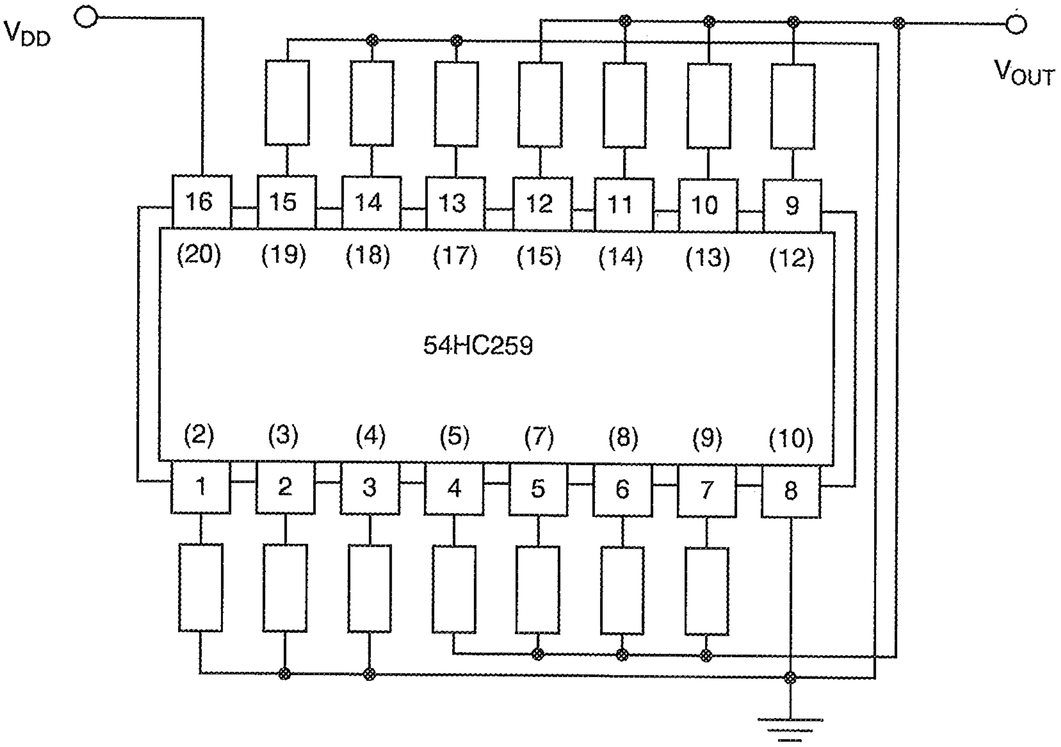
TABLE 5(c) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-9-10-11-12) (Pins C 5-7-8-9-12-13-14-15)	V_{OUT}	V_{DD}	V
3	Input - (Pin D/F 13) (Pin C 17)	V_{IN}	V_{GEN1}	Vac
4	Input - (Pin D/F 1) (Pin C 2)	V_{IN}	V_{GEN2}	Vac
5	Input - (Pin D/F 2) (Pin C 3)	V_{IN}	V_{GEN3}	Vac
6	Input - (Pin D/F 3) (Pin C 4)	V_{IN}	V_{GEN4}	Vac
7	Inputs - (Pins D/F 14-15) (Pins C 18-19)	V_{IN}	V_{SS}	V
8	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
9	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2} f_{GEN3} f_{GEN4}	100k ±10% 50k ±10% 25k ±10% 12.5k ±10% 50 ± 15% Duty Cycle $t_r = t_f \leq 400ns$	Hz
10	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V_{DD}	6.0(+0-0.5)	V
11	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	V_{SS}	0	V

NOTES

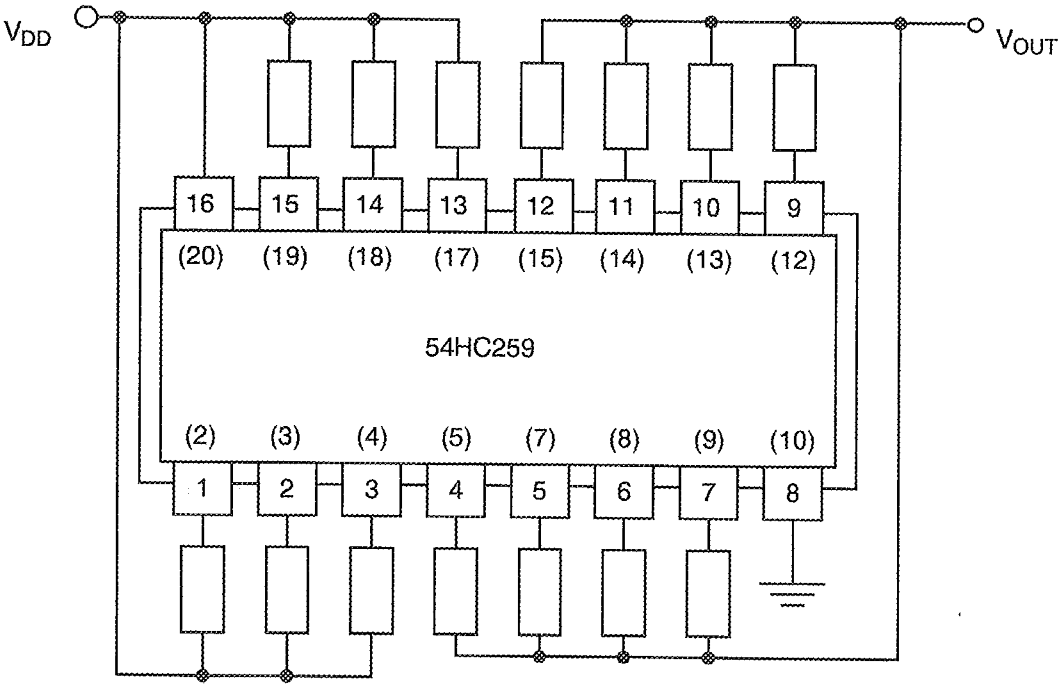
1. Input Protection Resistor = 680Ω min. to 47kΩ max.
2. Output Load = 1kΩ min. to 10kΩ max.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS



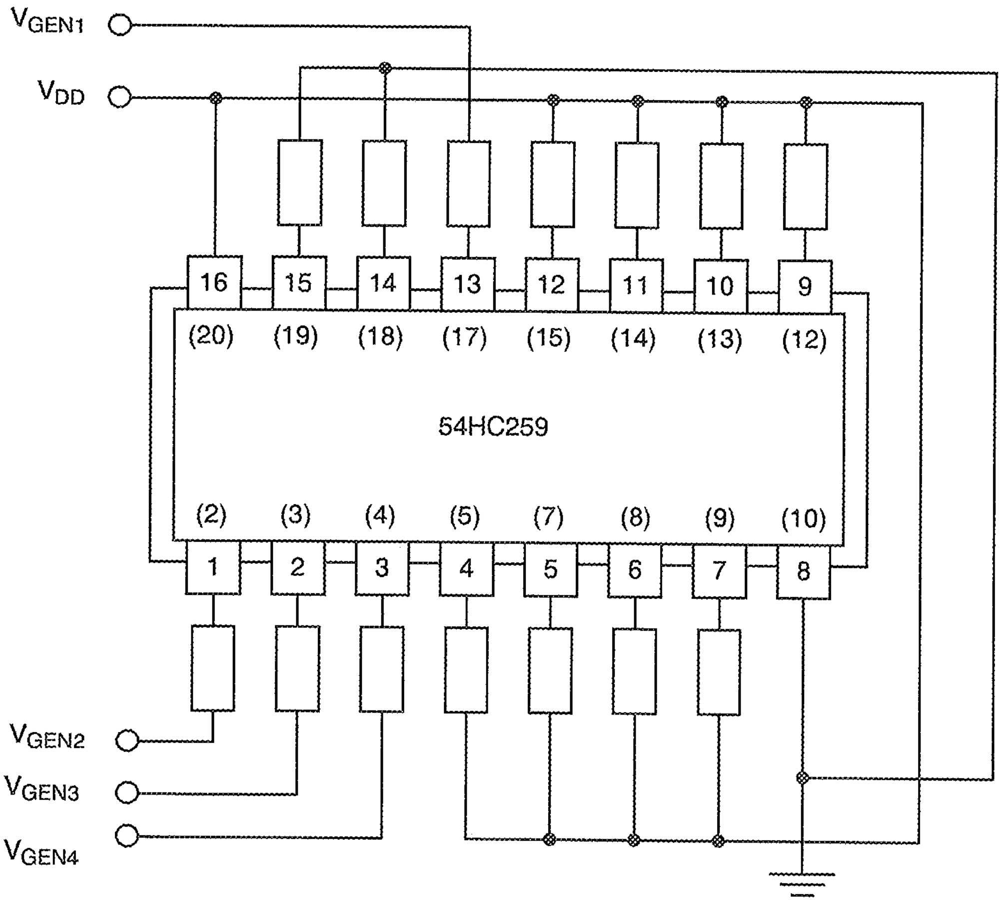
NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS



NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

FIGURE 5(c) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST



NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

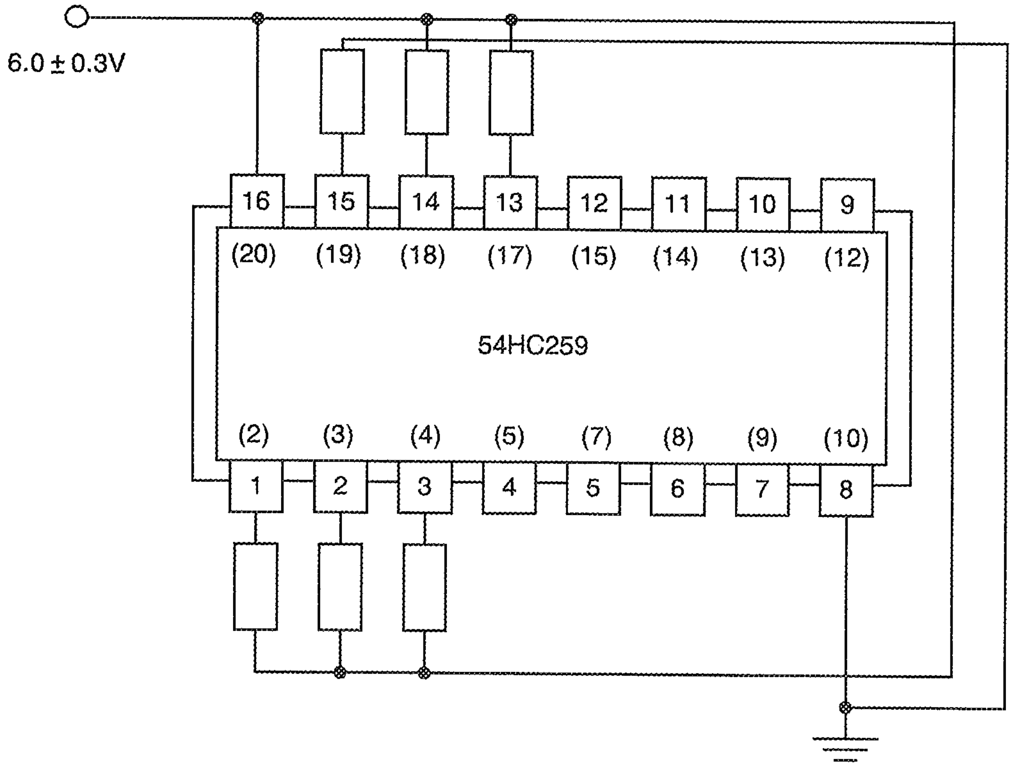
TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ) (NOTE 1)	ABSOLUTE		UNIT
						MIN	MAX	
1	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-	-
2	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-	-
3	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-	-
4 to 12	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±0.12	-	0.4	µA
13 to 18	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±20	-	-50	nA
19 to 24	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±20	-	50	nA
49 to 56	Output Voltage Low Level 4	V_{OL4}	As per Table 2	As per Table 2	±0.026	-	0.26	V
57 to 64	Output Voltage Low Level 5	V_{OL5}	As per Table 2	As per Table 2	±0.026	-	0.26	V
89 to 96	Output Voltage High Level 4	V_{OH4}	As per Table 2	As per Table 2	±0.2	3.98	-	V
97 to 104	Output Voltage High Level 5	V_{OH5}	As per Table 2	As per Table 2	±0.2	5.48	-	V
105	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	−0.45	−1.45	V
106	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	0.45	1.35	V

NOTES

1. The change limits (Δ) are applicable to the Operating Life test only. The change in parameters between initial and end point measurements shall not exceed the limits given. In addition, the absolute limits shall not be exceeded.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.
2. Input Protection Resistor = 680Ω min. to 47kΩ max.

TABLE 7 - ELECTRICAL MEASUREMENT DURING AND ON COMPLETION OF IRRADIATION TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN	MAX	
4 to 12	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	-	40	µA
105	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.6	−0.4	-1.5	V
106	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.6	0.4	1.4	V

APPENDIX 'A'

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AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.3	Para. 9.9.2, "Electrical Measurements at High and Low Temperatures": Only a test result summary, based on go-no-go tests and presented in histogram form is required.

APPENDIX 'B'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.3	Para. 7.1.1(b): Power Burn-in test is performed using STMicroelectronics Specification Ref.: 0019255. Para. 9.23, High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Para. 9.24, Power Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.4	Para. 9.21.1, Operating Life During Qualification Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.5	Para. 9.21.2, Operating Life Test During Lot Acceptance Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.