EVALUATION TEST PROGRAMME FOR INTEGRATED CIRCUITS:

MONOLITHIC AND MULTICHIP MICROCIRCUITS, WIRE-BONDED, HERMETICALLY SEALED

AND

FLIP-CHIP MONOLITHIC MICROCIRCUITS WITH NON-ORGANIC SUBSTRATE, HERMETICALLY AND NON-HERMETICALLY SEALED

ESCC Basic Specification No. 2269000

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1 PURPOSE

The purpose of this specification is to establish the procedure to be followed in the evaluation of component capabilities as required for space applications and thereby to anticipate, as far as possible, component behaviour during qualification testing. Therefore, the aim of such testing shall be to overstress specific characteristics of the component concerned with a view to the detection of possible failure modes. Additionally, a detailed destructive physical analysis shall be performed to detect any design and construction defects which may affect the reliability of the component and to facilitate failure analysis activities. The evaluation shall also include a check of the susceptibility of the component to ESD damage.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the evaluation.

2.1 ESCC SPECIFICATIONS

- No. 9000, Integrated Circuits: Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits with Non-Organic Substrate, Hermetically and Non-Hermetically Sealed and Die.
- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 21001, Destructive Physical Analysis of EEE Components.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 22500, Guidelines for Displacement Damage Irradiation Testing.
- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.
- No. 25100, Single Event Effects Test Method and Guidelines

NOTE:
Unless otherwise stated herein, reference within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- IEC Publication No. 60068 Part 2, Basic Environmental Testing Procedures.
- MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.
- MIL-STD-883, Test Methods and Procedures for Microelectronics.
- ECSS-Q-ST-60, Electrical, Electronic and Electromechanical (EEE) Components.
- ECSS-Q-ST-70-02, Thermal Vacuum Test for the Screening of Space Materials.
- J-STD-020, IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification For Non-Hermetic Surface-Mount Devices.
- JESD22-A101, EIA/JEDEC Standard Test Method: Highly-Accelerated Temperature and Humidity Stress Test (HAST).
- JESD22-A110, EIA/JEDEC Standard Test Method: Steady-State Temperature Humidity Bias Life Test.
- JESD22-B117, EIA/JEDEC Standard Test Method: Solder Ball Shear.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

Integrated Circuit (Microcircuit):	A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. Monolithic Microcircuits and Multichip Microcircuits are considered as Integrated Circuits.
Monolithic Microcircuit:	A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate (with a single semiconductor die).
Multichip Microcircuit	A microcircuit consisting of two or more semiconductor dice coming from the same manufacturer, from one or more foundries, individually attached to a single package cavity.
Wire-Bonded Integrated Circuit:	Either a monolithic or multichip microcircuit with the die/dice wire bonded to the package terminals.
Flip-Chip Integrated Circuit:	A monolithic microcircuit bumped top-side down to a substrate.
Add-on Components:	Capacitors and/or resistors mounted in and electrically connected to an Integrated Circuit assembly. Other component types are not permitted.
Hermetic Package	A component encapsulation which by design and construction is able to pass a seal test.
Non-Hermetic Package	A component encapsulation which by design or construction is unable to pass a seal test.

4 PROCEDURE

Unless otherwise specified, standard components shall be selected from a homogeneous lot at the Manufacturer to be evaluated. These components shall not have been submitted to any screening or burn-in but must have been manufactured in conformity with high reliability practice and an established Process Identification Document (PID) or an identifiable process which shall form the basis for the PID.

The tests specified in the programme shall be performed in the sequence shown in the appropriate chart, where:

- Chart IA is the Evaluation Test Programme for Wire-bonded Integrated Circuit components
- Chart IB is the Evaluation Test Programme for Hermetic Flip-Chip Integrated Circuit components
- Chart IC is the Evaluation Test Programme for Non-Hermetic Flip-Chip Integrated Circuit components

All results shall be recorded and failed components submitted to a failure analysis. Probable failure modes and mechanisms shall be determined.

The evaluation test programme shall be performed, under the supervision of the ESCC Executive, by the Manufacturer or at a test laboratory approved by the ESCC Executive.

4.1 AGREED DEVIATIONS TO CHART IA, CHART IB, CHART IC TEST REQUIREMENTS

Deviations to the test requirements of Chart IA, Chart IB or Chart IC (as applicable) may be approved subject to full justification being provided by the Manufacturer to the ESCC Executive. Approved deviations shall be fully documented and all details shall be included in the Evaluation Test Programme.

4.2 MANDATORY PREREQUISITES FOR FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS

Prior to the start of an evaluation implementing the requirements of this evaluation test programme, and in order to adequately comply with the requirements of ESCC Basic Specification Nos. 20100 and 22600, the Manufacturer shall have completed a development and process qualification plan specifically including assessments of, and creating specifications for, the following:

- bump dimension and co-planarity.
- Electromigration at bump level.
- Alloy composition in compliance with ECSS-Q-ST-60.
- Ionic contamination resulting from the use of flux, and within the underfill.
- Electrical characterisation over the temperature range pre- and post- ball/column attachment.
- Level 2 interconnect (e.g. balls, columns) attachment to package, representative of manufacturing and screening effects.
- Underfill and thermal interface material evaluation.
- Adequacy of substrate finishing.
- Package mounting on PCB.

Such assessments may be performed on representative test structures but, in any case, shall be fully documented and must be repeated in the event of material, process and supply chain changes.

The Manufacturer shall have systematic control over all materials used in the construction of the Flip-Chip Integrated Circuit components, particularly for underfill and thermal interface material. This shall be documented in the PID.

5 TEST PROGRAMME SEQUENCE AND SAMPLE DISTRIBUTION

5.1 SELECTION OF COMPONENTS FOR EVALUATION TESTING

The number of components to be selected for evaluation testing shall depend on whether a single component type or a family of parts is evaluated and the number of component types chosen to represent the family.

For Wire-bonded Integrated Circuit components with Hermetic Packages, not less than 111 specimens (plus additional samples as specified) shall be used for each test programme.

For Flip-Chip Integrated Circuit components with Hermetic Packages, not less than 109 specimens (plus additional samples as specified) shall be used for each test programme.

For Flip-Chip Integrated Circuit components with Non-Hermetic Packages, not less than 119 specimens (plus additional samples as specified), with or without balls/columns attached, shall be used for each test programme.

The component types chosen to represent a family shall cover the range of components to be evaluated and be representative of the different package and pin configurations under consideration. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses.

The total number of specimens may be a combination of components and representative test structures as agreed by the ESCC Executive. The samples shall be as specified by, or as agreed with, the ESCC Executive.

The above-mentioned quantity shall be submitted to the full evaluation procedure whenever a new technology has been applied to the components concerned, where there is insufficient experience in their production.

5.2 DETAIL SPECIFICATIONS

Should a Detail Specification for the component(s) to be evaluated not exist, the Manufacturer shall prepare such a document(s) in accordance with the established ESCC format and submit it to the ESCC Executive for provisional approval. This shall then serve as a basis for the ordering and testing of the relevant components.

5.3 INSPECTION RIGHTS

The ESCC Executive reserves the right to inspect at any time the components processed for evaluation purposes. The Manufacturer shall notify the ESCC Executive at least three working days in advance of the date of internal visual inspection (but see Para. 5.4).

5.4 CONTROL DURING FABRICATION

The components shall be produced as defined in Para. 4 of this specification. Internal visual inspections shall be performed on the lot to be tested to the extent that this forms part of the Manufacturer's standard procedures. Progress of the components shall be observed closely and recorded together with an analysis of any reject. A chart showing the numbers in/out and failure cause for each fabrication stage shall be submitted to the ESCC Executive.

6 INSPECTION

6.1 GENERAL

The components shall be checked to verify their suitability for the Evaluation Test Programme. Defects or deviations from the established ESCC requirements may invalidate the evaluation. For each measurement or inspection performed, the results shall be summarised in terms of quantity tested, quantity passed and quantity rejected. If components are rejected, the reason shall be clearly identified.

6.2 DIMENSIONS (100%)

All components shall be inspected (go-no-go) in accordance with Physical Dimensions and Terminal Identification in the Detail Specification. Where gauges exist for performance of measurements, these may be used. For packages with a high pin count, the measurements may be performed using a sampling scheme which shall be approved by the ESCC Executive. Rejected components shall be replaced.

6.3 WEIGHT (100%)

All components shall be weighed (go-no-go). Any components that exceed the weight defined in the Detail Specification shall be rejected and replaced.

6.4 ELECTRICAL MEASUREMENTS (100%)

These measurements shall be performed (go-no-go) in accordance with Room Temperature Electrical Measurements in the Detail Specification at an ambient temperature of +22 ±3°C. Rejected components shall be replaced.

6.5 EXTERNAL VISUAL INSPECTION (100%)

All components shall be inspected in accordance with ESCC Generic Specification No. 9000. Rejected components shall be replaced.

6.6 PARTICLE IMPACT NOISE DETECTION (PIND) (100%)

All components shall be tested in accordance with the defined in ESCC Generic Specification No. 9000. Rejected components shall be replaced.

6.7 RADIOGRAPHIC INSPECTION (100%)

Not applicable to Flip-Chip Integrated Circuit components.

All components shall be inspected in accordance with ESCC Generic Specification No. 9000. Additional axes may be radiographed if, by so doing, it is possible to observe any faults. Rejected components shall be replaced.

6.8 HERMETICITY (100%)

Applicable to hermetically sealed components only.

Fine and gross leak tests shall be performed on all components in accordance with the requirements defined in ESCC Generic Specification No. 9000. Rejected components shall be replaced.

6.9 MARKING AND SERIALISATION (100%)

All components shall be marked and serialised in accordance with the standard procedures of the Manufacturer concerned.

6.10 MATERIALS AND FINISHES

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components specified herein shall be tested in accordance with ECSS-Q-ST-70-02 to verify its outgassing requirements, unless relevant data is available. See also Para. 8.3.4.2 herein.

6.11 COMPLETION OF INSPECTION

The completion of inspection shall result in a batch of components that have been verified as to their suitability for the Evaluation Test Programme, i.e. each component has satisfied the requirements of Paras. 6.2 to 6.10 inclusive.

7 INITIAL ELECTRICAL MEASUREMENTS (100% READ AND RECORD)

These measurements shall be made according to the Room, High and Low Temperatures Electrical Measurements in the Detail Specification. All characteristics shall be recorded against serial numbers. Rejected components shall be replaced.

8 EVALUATION TEST PROGRAMME

8.1 GENERAL

The evaluation tests shall be performed as specified in Chart IA, Chart IB or Chart IC (as applicable). The components shall be randomly divided into groups and their associated subgroups in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable). When a family of components is under investigation, the variations within that family must be represented in each group/subgroup which might require samples in addition to the quantities specified in Chart IA, Chart IB or Chart IC (as applicable) (see Para. 5.1).

The Subgroup 2A tests shall be completed and the results analysed before the Subgroup 3B tests are commenced.

All failed components shall be analysed. The depth of analysis shall depend upon the circumstances in which failure occurred and upon whether useful information may be gained. As a minimum, the failure mode shall be determined in each case. Components not failing catastrophically, i.e. those displaying out-of-tolerance electrical parameters shall not be removed from the test sequence but monitored to observe degradation trends.

8.2 GROUP 1 - CONTROL GROUP

This group shall be retained for comparison purposes. Whenever electrical measurements are made on any components under test, these components shall also be measured.

8.3 GROUP 2 - DESTRUCTIVE TESTS

8.3.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable).

Testing of Integrated Circuit components with ball or column terminals (i.e. CGA or BGA) may be performed on parts without balls/columns unless otherwise specified.

The use of representative test structures (including empty packages) is subject to agreement with the ESCC Executive and to be specified in advance in the applicable test plan.

8.3.2 Subgroup 2A - Step-Stress Tests

8.3.2.1 General

This subgroup shall be randomly divided into further subgroups in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable).

For both the Temperature and Power Step-Stress Tests, the step-stress sequence shall be terminated when 50% (rounded up) of the specimens have been destroyed, unless practical reasons prevent this.

8.3.2.2 Subgroup 2A(i) - Determination of Thermal Resistance/Conductivity

MIL-STD-883, Method 1012.

8.3.2.3 Parameters to be Measured During Step-Stress Tests

During step-stress tests, electrical measurements shall be made in accordance with Parameter Drift Values in the Detail Specification. If parameter drift values are not specified in the Detail Specification, then the parameters to be measured shall be selected from Room Temperature Electrical Measurements in the Detail Specification. In the case of doubt as to the applicability of any given parameter, the parameter shall be measured. Quiescent current (if applicable) shall be measured in all cases. At the termination of the step-stress sequences, any surviving components shall have their thermal resistance/conductivity measured as specified in Para. 8.3.2.2.

8.3.2.4 Subgroup 2A(ii) - Temperature Step-Stress Test

The tests in this subgroup shall be performed as specified in Chart II. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting temperature (which will be no higher than the maximum operating temperature as defined in the Detail Specification) and the temperature steps (with a maximum step of 25°C) to be employed will be decided by the ESCC Executive.

8.3.2.5 Subgroup 2A(iii) - Power Step-Stress Test

(a) Applicability:

This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure:

The tests in this subgroup shall be performed as specified in Chart III. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting power (which will be no higher than the maximum input power as defined in the Detail Specification) and the power steps (with a maximum step of 20%) to be employed will be decided by the ESCC Executive.

8.3.2.6 Analysis of Subgroup 2A

The analysis of Subgroup 2A shall be presented to the ESCC Executive in a graphical form, supported by the actual results, as follows:

- The number of functional failures shall be plotted against each temperature or power level (if applicable) applied. The cumulative failure rate shall also be plotted.
- The parameters (as defined in Para. 8.3.2.3 above) shall be monitored, recorded and plotted against time for each temperature or power level (if applicable) as appropriate.
- The average drift of the parameters at each temperature or power level applied shall be plotted against temperature or power (if applicable) as appropriate.

The analysis of the results of Subgroup 2A(ii) and 2A(iii) (as/if applicable)) shall be used to determine the most effective temperatures and power (if applicable) for the accelerated electrical endurance test (Subgroup 3B).

8.3.3 Subgroup 2B - Radiation Tests

8.3.3.1 Total Dose Steady-State Radiation Test

8.3.3.1.1 General

The component technology shall be evaluated thoroughly for degradation due to total dose steady-state irradiation effects. Components shall be tested in accordance with a Radiation Test Plan, approved by the ESCC Executive, and in accordance with ESCC Basic Specification No. 22900 except as specified herein.

The Radiation Test Plan shall be designed to determine worst case bias conditions, to detect the degree of variation in radiation response from wafer lot to lot, and the degree of time dependence of the radiation response. The use of Process Validation modules and representative test structures is encouraged for evaluation testing.

For high impedance component terminals, e.g. MOS gates, the influence of voltage value and duty cycles of bias shall be studied so as to determine the worst-case bias condition. The applicability of shorted terminals for transport and storage shall be validated for non-CMOS technologies. Time dependent effects shall be studied for MOS devices or those technologies having inherent MOS structures such as bipolar devices with oxide isolation. Cases of "rebound" (a net degradation of performance due to changes in trapped oxide charge and interface state density over periods of time of the order of several weeks) in N-channel MOS elements or their equivalent in other devices shall be identified and reported explicitly. The significance of other cases of time-dependence for tests conducted at low dose rates shall be reported.

Enhanced Low Dose Rate Sensitivity (ELDRS) (bipolar components demonstrate increased electrical parameter degradation with decreasing dose rates) shall be studied for devices that contain bipolar transistors and optoelectronics, by comparing at a given dose level, low dose rate test results (within the Low Dose Rate (see ESCC No. 22900) for discrete devices and ≤ 36 RAD(Si)/hour for Integrated Circuits) with high dose rate test results (at least 2 orders of magnitude higher than low dose rate) on parts from the same wafer lot. A part is considered as ELDRS sensitive if the enhancement factor observed at the lower dose rate is greater than 1.5 on the median value of the most sensitive measured parameter. Devices containing bipolar transistors and MOS elements (e.g. BiCMOS) shall be evaluated for both ELDRS and MOS specific effects.

8.3.3.1.2 Sample Selection

A minimum sample of 10 components shall be selected at random from different wafers and wafer locations from a minimum of two different wafer lots, making a minimum of 20 components in all. One additional component shall be designated the unirradiated control. For each wafer lot, the sample size for each unique set of test conditions as defined in the Radiation Test Plan shall be at least 5. As a minimum, the test conditions shall include biased and unbiased testing. The components shall have been screened to commercial or military grade and assembled in one of the final manufacturing packages (preferably with Kovar lids, if within the range of packages to be covered by evaluation). The components shall originate from the same supplier, fabrication plant and processing line as intended for future hi-rel production.

8.3.3.1.3 Sample Serialisation

Immediately after selection, each individual component shall be serialised to facilitate pre- and post-irradiation data identification and comparison. The system of marking shall be such as to ensure that the components are clearly identified by:

(a) a unique, individual serial number
(b) a Date Code, Wafer Lot Number and Wafer Number

8.3.3.1.4 Radiation Test Levels

Components shall be exposed to a series of multiple exposures until either functional failure occurs (up to an absolute maximum of 1.5MRAD(Si)), or the targeted ESCC radiation hardness assurance evaluation level is reached, whichever is first.

The ESCC radiation hardness assurance evaluation level is 150% of the Total Dose Radiation Level specified in the Detail specification.

Unless otherwise specified in the Radiation Test Plan, the multiple exposures shall be as follows:

- Exposure 1: 25% of the specified Total Dose Radiation Level
- Exposure 2: 50% of the specified Total Dose Radiation Level
- Exposure 3: 100% of the specified Total Dose Radiation Level
- Exposure 4: 150% of the specified Total Dose Radiation Level

8.3.3.1.5 Radiation Exposure and Test Sequence

The sequence and details of steps for the radiation exposure and test sequence during technology evaluation shall be as given below. The Standard Dose Rate (see ESCC No. 22900) shall be used unless otherwise specified. The value of bias voltage used shall not be altered between steps (c) and (g). The flow chart for the evaluation test sequence is as per ESCC No. 22900 Figure 2.

(a) Serialisation of the components and the unirradiated control.
(b) Initial electrical testing (see Note 1) of the components and the unirradiated control, with special emphasis given to parameters tested after irradiation. All measurements shall be read and recorded in the Total Dose Radiation Test Report against serial numbers.
(c) Set-up of radiation source and bias of components for irradiation as specified.
(d) Irradiation of components in multiple exposures, with electrical testing after each exposure (see Para. 8.3.3.1.4).
(e) Post-radiation electrical tests (see Note 2) after each exposure on the components and the unirradiated control. All tested parameters shall be recorded in the Total Dose Radiation Test Report against serial numbers.
(f) Room temperature anneal, under bias (see Note 1), for a total of 168 hours with electrical testing (see Note 2) of the components and the unirradiated control at 24, 48 and 168 hours during annealing.

(g) Accelerated ageing, under bias (see Note 3). The components shall be baked at +100 ±5°C under bias for 168 hours. Alternative conditions are allowed if these conditions have been demonstrated to cause equal or greater rebound effects (e.g. degradation in speed, timing and output drive). Lower temperatures and times are required if the above ageing conditions have been demonstrated to produce excessive performance recovery.

(h) Final electrical testing (see Note 1) of the components and the unirradiated control

NOTES:

1. Electrical test parameters shall be those of "Room Temperature Electrical Measurements" in the Detail Specification, if existing, or the specified parameters in the Radiation Test Plan expected to form the subsequent basis for such measurements.
2. Electrical test parameters shall, as a minimum, be those of "Electrical Measurements for Total Dose Radiation Testing" in the Detail Specification, if existing, or those specified parameters in the Radiation Test Plan expected to form the subsequent basis for such measurements.
3. Components irradiated unbiased shall remain unbiased during steps (f) and (g).

8.3.3.1.6 Reporting

Electrical test results and other observations from radiation testing shall be collected in a Total Dose Radiation Test Report. Recommendations regarding the form of the tests to be performed in subsequent phases shall be given, including the requirements for:

(a) Worst case bias.

(b) Room temperature anneal times.

(c) Accelerated ageing temperature and time for MOS components.

(d) Sample size.

(e) Detection of wafer lot to lot variation in radiation response.

(f) The specified values of Total Dose Radiation Level and radiation dose rate requirements.

(g) Parameters and conditions to be entered in the "Electrical Measurements for Total Dose Radiation Testing" section of the Detail Specification.

8.3.3.2 Single Event Effects Test (SEE)

In accordance with ESCC Basic Specification No. 25100, if applicable.

8.3.3.3 Displacement Damage

In accordance with ESCC Basic Specification No. 22500, if applicable.

8.3.4 Subgroup 2C - Construction Analysis

PRECAUTIONS: If it is known, or believed, that beryllium oxide or other toxic substances are used in the construction of the component, precautionary measures shall be employed.

8.3.4.1 Internal Water Vapour Content

Applicable to components with hermetic packages only.

MIL-STD-883, Method 1018, Procedure 1.

8.3.4.2 Outgassing

Applicable to components with non-hermetic packages only.

ECSS-Q-ST-70-02 (performed on suitable raw material samples of all those used in the component).

8.3.4.3 Opening

The components shall be opened using a technique which does not contaminate the internal structure or in any way impair the ability to observe defects.

8.3.4.4 Internal Visual Inspection

Each component shall be visually inspected in accordance with ESCC Generic Specification No. 9000. Photographs shall be taken as follows:

(a) An overall photograph of the opened component.

(b) An overall photograph of the die (see note) plus any Add-on Components.

(c) Photographs of any anomalies found.

NOTE:

May be excluded for Flip-Chip Integrated Circuit components with thermal interface material between the die and the lid/heat-spreader.

8.3.4.5 Scanning Electron Microscope (SEM) Inspection

This inspection shall include, but shall not necessarily be limited to, examination of the following:

(a) Detailed examination of any anomalies identified by the internal visual inspection (Para. 8.3.4.4 above).
Photographs shall be taken of the above.

(b) Low magnification (up to 500x) shall be used to assess:
(i) Clearance of bond wires at the die edge.
(ii) Quality of bonding at the die.
(iii) Quality of bonding at the post.
Photographs shall be taken of the above.

(c) High magnification (1000x or greater) shall be used to assess:
(i) Metallisation coverage and consistency at steps.
(ii) Metallisation coverage at contact windows, bonding pads, etc.
Photographs shall be taken of the above.

In the case of components with a glassivated surface, this examination shall first be attempted through the glassivation.

If the resolution is inadequate, the glassivation shall be removed. This step must be postponed until the bond strength (Para. 8.3.4.6) test has been performed.

For components with multi-level metallisation, the upper layer(s) shall be removed to permit assessment of the above mentioned features. This step shall also be postponed until the bond strength test (Para. 8.3.4.6) has been performed.

For deep sub-micron components, SEM inspection of the die may be impracticable; in which case the Manufacturer shall fully justify any deviations in accordance with Para. 4.1.

8.3.4.6 Bond Strength Test

Not applicable to Flip-Chip Integrated Circuit components.

In accordance with Bond Strength in ESCC Generic Specification No. 9000.

8.3.4.7 Die Shear Strength or Substrate Attach Strength or Bond Shear (Flip-Chip)
In accordance with Die Shear Strength or Substrate Attach Strength or Bond Shear (Flip-Chip) in ESCC Generic Specification No. 9000.

8.3.4.8 Microsectioning
(a) Glassivation Layer Integrity (if applicable): MIL-STD-883, Method 2021.

(b) Mounting:
The component(s) shall be mounted on a carrier or in a transparent thermosetting resin. This shall have a curing temperature below the maximum storage temperature of the component(s). The resin shall be evacuated after mixing and after the component has been mounted in the uncured resin.

(c) Microsectioning
The component(s) shall be ground and polished to achieve a surface finish of at least 0.1 micron. To improve definition and detail, chemical etches shall be used to highlight junction definition, metallographic features, etc. The following, not exhaustive, features shall be assessed:
(i) Diffusion and oxide characteristics.
(ii) Metal/semiconductor interfaces.
(iii) Metal/metal interfaces.
(iv) Thickness and consistency of layers; particularly insulating layers in components with multiple layer metallisation.
(v) Plating thickness and consistency on posts and pins.
(vi) Bumps/balls/columns shall be included.
(vii) Under bump metallization interface.

Photographs shall be taken of the above.

8.3.4.9 Lid Attach Strength
Lid Pull or Lid Shear, as applicable, shall be performed in accordance with MIL-STD-883, Test Method 2027 (Pull test) or 2019 (Shear test).

8.3.4.10 Terminal Strength
(a) For chip carrier packages: MIL-STD-883, Test Method 2004, Test Condition D.
(b) For ball grid array packages: JESD22-B117.
(c) For column grid array packages: MIL-STD-883, Test Method 2038.
(d) For other packages: MIL-STD-883, Test Method 2004, Test Condition B2.

8.3.5 Subgroup 2D - Package Tests

8.3.5.1 General
The samples in this group shall be randomly divided between subgroups 2D(i) to 2D(iv) or 2D(v), as applicable, in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable). Any components from 2D(i) or 2D(ii-c) that have not been destroyed shall then also be subjected to subgroup 2D(iii).

8.3.5.2 Subgroup 2D(i) - Thermal Tests

8.3.5.2.1 Thermal Tests for Components with Hermetic Packages (Chart IA and Chart IB)

(a) Applicability:
These tests must be performed on electrically good components.

(b) Procedure:

(i) Temperature Cycling
All components shall be subjected to the test defined in Chart F4A of ESCC Generic Specification No. 9000 except that, for Wire-bonded Integrated Circuit components the number of cycles shall be 100 minimum, and for Flip-Chip Integrated Circuit components the number of cycles shall be 1500 minimum.

(ii) Seal Test
All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(iii) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(iv) Thermal Shock
Not required for Flip-Chip Integrated Circuit components.

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000 with 100 cycles instead of 10 cycles.

(v) Seal Test
Not required for Flip-Chip Integrated Circuit components.

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(vi) Electrical Measurements
Not required for Flip-Chip Integrated Circuit components.

These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(vii) Destructive Physical Analysis
Not applicable to Wire-bonded Integrated Circuit components.

A DPA shall be carried out on one hermetic Flip-Chip Integrated Circuit component, selected from the 15 samples.

NOTE: The DPA content shall be proposed by the Manufacturer and subsequently agreed with the ESCC Executive. ESCC Basic Specification No. 21001 may be used as a guideline. DPA shall be performed by a laboratory mutually approved by the Manufacturer and by the ESCC Executive.

8.3.5.2.2 Thermal Tests for Flip-Chip Integrated Circuit Components with Non-Hermetic Packages (Chart IC)

(a) Applicability:
These tests must be performed on electrically good components.

(b) Procedure:

(i) Scanning Acoustic Microscopy (SAM) – Initial Inspection
MIL-STD-883, Method 2030.

(ii) Preconditioning
J-STD-020. Preconditioning per applicable Moisture Sensitivity Level as specified by the Manufacturer. Conditions shall be agreed with the ESCC Executive prior to evaluation testing.

(iii) Scanning Acoustic Microscopy (SAM) – Intermediate Inspection
MIL-STD-883, Method 2030.

(iv) Temperature Cycling
All components shall be subjected to the test defined in Chart F4A of ESCC Generic Specification No. 9000. 1500 cycles instead of 100 cycles.

(v) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(vi) Scanning Acoustic Microscopy (SAM) – Final Inspection
MIL-STD-883, Method 2030.

(vii) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(viii) Destructive Physical Analysis
A DPA shall be carried out on two hermetic Flip-Chip Integrated Circuits, selected from the 15 samples.

NOTE: The DPA content shall be proposed by the Manufacturer and subsequently agreed with the ESCC Executive. ESCC Basic Specification No. 21001 may be used as a guideline. DPA shall be performed by a laboratory mutually approved by the Manufacturer and by the ESCC Executive.

8.3.5.3 Subgroup 2D(ii) - Mechanical and Thermal Vacuum Tests

8.3.5.3.1 Subgroup 2D(ii-a) - Mechanical Tests

(a) Applicability

These tests must be performed on electrically good components.

(b) Procedure

(i) Preconditioning

Applicable to Flip-Chip Integrated Circuit components with Non-Hermetic Packages only.

Preconditioning shall be performed in accordance with J-STD-020, per the applicable Moisture Sensitivity Level specified by the Manufacturer. Conditions shall be agreed with the ESCC Executive prior to evaluation testing.

(ii) Mechanical Shock

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000 with 50 pulses (per orientation) instead of 5 pulses (per orientation).

(iii) Seal Test

Not applicable to components with Non-Hermetic Packages.

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(iv) Electrical Measurements

These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(v) Vibration

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000 with 120 sweeps (total) instead of 12 sweeps (total).

(vi) Constant Acceleration

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000 (for Qualification, Periodic Testing and Lot Validation Testing).

(vii) Seal Test

Not applicable to components with Non-Hermetic Packages.

All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(viii) Electrical Measurements

These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

8.3.5.3.2 Subgroup 2D(ii-b) - Thermal Vacuum Test

(a) Applicability:
3 of the samples specified in this subgroup shall be subjected to these tests.

These tests must be performed on electrically good components.

(b) Procedure:

(i) Scanning Acoustic Microscopy (SAM) – Initial Inspection
MIL-STD-883, Method 2030.

(ii) Thermal Vacuum
All components shall be subjected to thermal vacuum with the following conditions:

- 20 cycles
- T_{amb} = -30°C to + 70°C
- pressure: ≤ 1mPa
- dwell time: 2 hours
- slope: 2°C/min

(iii) Scanning Acoustic Microscopy (SAM) – Final Inspection
MIL-STD-883, Method 2030.

8.3.5.3.3 Subgroup 2D(ii-c) - Mechanical Tests:

(a) Applicability:
All components subjected to Mechanical Subgroup 2D(ii-a) tests, including any failures, shall be subjected to these tests.

(b) Procedure:

(i) Solderability
All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

For Flip-Chip Integrated Circuit components Solderability shall be performed on parts with balls/columns attached.

(ii) Permanence of Marking
All components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(iii) Lid Torque
Applicable to packages which use a glass-frit-seal to lead frame, lead or package body only (i.e. wherever frit seal establishes hermeticity or package integrity).

MIL-STD-883, Method 2024.

(iv) Lid Attach Strength
As per Para. 8.3.4.9.

(v) Terminal Strength
As per Para. 8.3.4.10.

8.3.5.4 Subgroup 2D(iii) - Resistance to Soldering Heat

(a) Applicability:
2 samples plus any components from Subgroups 2D(i) or 2D(ii-c) that have not been destroyed shall be subjected to these tests. These tests must be performed on electrically good components. Components previously subjected to Subgroup 2D(i) may be replaced.

(b) Procedure:
IEC Publication No. 60068-2-20 Test Tb, Method 1A with no thermal screen or flux for 10 ±1s, or MIL-STD-750, Method 2031.

Following each cycle, electrical measurements shall be performed (go-no-go) in accordance with Room Temperature Electrical Measurements in the Detail Specification and a Seal test shall be performed in accordance with Para. 8.3.5.3.1(b)(iii) above.

The test shall be repeated until the component has failed or 5 cycles have been performed, whichever is the sooner.

8.3.5.5 Subgroup 2D(iv) - Pin To Pin Isolation

(a) Applicability:
This test must be performed on empty package(s) that have been through the normal assembly procedures up to sealing.

(b) Procedure:
MIL-STD-883, Method 1003.

8.3.5.6 Subgroup 2D(v) – Humidity Test

(a) Applicability:
These tests must be performed on electrically good components.

(b) Procedure:
Either JESD22-A101, Steady-State Temperature Humidity Bias Life Test or JESD22-A110, Highly-Accelerated Temperature and Humidity Stress Test (HAST). The standard to be followed, and the applicable test conditions, are subject to the approval of the ESCC Executive.

8.3.6 Subgroup 2E - Electrical Tests

8.3.6.1 General

The components in this subgroup shall be randomly divided between those tests that are performed.

8.3.6.2 Electrostatic Discharge Sensitivity (ESDS) Test

ESD testing shall be performed in accordance with ESCC Basic Specification No. 23800. If the component under examination is not categorised into one of the 3 classes listed, then the component shall be termed "unclassified".

When the evaluation covers a family or series of components, the types selected for this test shall be representative of all protection circuits within this family or series.

8.3.6.3 Characterisation

(a) Safe Operating Area

(i) Applicability:
This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design.

Additionally, it shall only be applied to integrated circuit components that do not have internal output protection circuitry. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(ii) Procedure:
The ESCC Executive shall review the component type and technology to determine the test conditions.

(b) Current Limits
The design of each component under investigation shall be examined to ensure that no part of the component carries more than the maximum current defined by the technology or process design rules.

(c) Breakdown Voltage, Input or Output

(i) Applicability:
Applicable to digital components only.

(ii) Procedure:
MIL-STD-883, Method 3008 shall be applied to find the limiting value.

(d) Input Interaction

(i) Applicability:
Applicable to digital components only.

(ii) Digital Components Procedure:
The truth table shall be applied at the maximum operating frequency under the conditions specified in the truth table.

(e) Verification of Functionality
The functionality of the component shall be explored over varying temperature ranges, levels of supply voltage, etc. The ESCC Executive shall review the component type and technology to determine the exact procedure to be adopted. Data shall be presented, preferably, in a graphical form: Schmoo plots for example.

8.3.7 Subgroup 2F - Wafer Tests

8.3.7.1 Bump Shear
JESD22-B117 on a minimum of 50 bumps (a special test structure might be necessary for the performance of this test).

8.4 GROUP 3 - ENDURANCE TESTS

8.4.1 General
This group shall be randomly divided into subgroups in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable).

8.4.2 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test
Unless otherwise specified in the Detail Specification, all components shall be subjected to the test defined in ESCC Generic Specification No. 9000.

8.4.3 Subgroup 3B - Accelerated Electrical Endurance Test

This group shall be randomly divided into 3 subgroups in the quantities indicated in Chart IA, Chart IB or Chart IC (as applicable). The applicable tests shall not be performed until the subgroup 2A tests have been completed and analysed, and 3 test conditions selected. The tests in this group shall be performed as specified in Chart IV.

The temperatures T_1, T_2 and T_3 shall be chosen such that within approximately 1000, 500 and 168 hours, the parameter(s) defined in Para. 8.3.2.3 above can be expected to have drifted to an extreme of the permitted range. A common applied power (if applicable) also determined from the Subgroup 2A tests, shall be used. If the power step-stress test (as defined in Para. 8.3.2.5) was not performed, the components shall be operated at their maximum rated dissipation. Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times:

T_1 (1000 hrs)	T_2 (500 hrs)	T_3 (168 hrs)
168 (+24 -0) hrs	168 (+24 -0) hrs	168 (+24 -0) hrs
500 (+24 -0) hrs	500 (+24 -0) hrs	-
1000 (+24 -0) hrs	-	-

Failed components shall be removed for analysis as specified in Para. 8.1.

8.4.4 Subgroup 3C - Extended Burn-in Test

The components shall be tested for 1000 hours at the conditions defined in the Detail Specification for Power Burn-in. Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs and 1000 (+24 -0) hrs.

If the conditions determined for the Subgroup 3B T1 1000 hour Accelerated Electrical Endurance Test in Para. 8.4.3 above are identical to those defined for Power Burn-in, this test shall not be performed.

If the conditions defined for the Subgroup 3D Extended Life Test in Para. 8.4.5 are identical to those defined for Power Burn-in, this test shall not be performed.

8.4.5 Subgroup 3D - Extended Life Test

The components shall be subject to a Life test for 4000 hours at T_{amb} = +125°C per MIL-STD-883, Method 1005. The applied operating conditions shall be based on the conditions defined in the Detail Specification for Operating Life and shall be subject to approval by the ESCC Executive.

Time temperature regression per MIL-STD-883 Method 1005 Class S may be applied.

Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0)hrs, 500 (+24 -0)hrs, 1000 (+24 -0)hrs, 2000 (+24 -0) and 4000 (+24 -0)hrs.

8.5 GROUP 4 - RESERVE

Should any additional tests be considered necessary, the components in this subgroup shall be used.

9 DATA DOCUMENTATION

9.1 GENERAL REQUIREMENTS

An evaluation test report shall be established. This shall comprise the following:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Sample identification.
(e) Production data.
(f) Inspection data.
(g) Initial electrical measurements.
(h) Group 1 - Control Group data.
(i) Subgroup 2A(i) - Thermal Resistance/Conductivity data.
(j) Subgroup 2A(ii) - Temperature Step-Stress test data.
(k) Subgroup 2A(iii) - Power Step-Stress test data (if applicable).
(l) Subgroup 2B - Total Dose Radiation Test Report, and other radiation tests data
(m) Subgroup 2C - Construction Analysis data.
(n) Subgroup 2D - Package tests data including Subgroups 2D(i), 2D(ii-a), 2D(ii-b), 2D(ii-c), 2D(iii), 2D(iv), 2D(v) (as applicable).
(o) Subgroup 2E - Electrical tests data.
(p) Subgroup 2F – Wafer Tests data (if applicable).
(q) Subgroup 3A - HTRB test data (if applicable).
(r) Subgroup 3B - Accelerated Electrical Endurance test data.
(s) Subgroup 3C - Extended Burn-in test data (if applicable).
(t) Subgroup 3D – Extended Life Test data.
(u) Group 4 - Reserve data (if applicable).
(v) Summary of results and conclusions.

Items (a) to (v) inclusive shall be grouped, preferably as subpackages, and for identification purposes, each page shall include the following information:

– Manufacturer's/test house's name.
– Lot identification.
– Date of establishment of the document.
– Page number.

9.2 COVER SHEET(S)

The cover sheet (or sheets) of the evaluation test report shall include as a minimum:

(a) Reference to this document, including issue and date.
(b) Component type(s) and number(s).
(c) Lot(s) identification.
(d) Manufacturer's/test house's name and address.
(e) Location of the manufacturing plant/test house.
(f) Signature on behalf of the Manufacturer/test house.
(g) Total number of pages of the evaluation test report.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be included in the evaluation test report. Where applicable, this list shall contain the inventory number, Manufacturer type number, serial number, calibration status data, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all references or codes which are necessary to correlate the test data provided with the applicable tests.

9.5 SAMPLE IDENTIFICATION (PARA. 5.1)

This shall identify the criteria used for the selection of the particular components used for the tests, when evaluating a range of components by means of representative samples.

9.6 PRODUCTION DATA (PARA. 5.4)

The progress of the components through the normal manufacturing processes shall be documented. The components failing a particular process shall be detailed, together with the reason for their removal.

9.7 INSPECTION DATA (PARA. 6)

The number of components subjected to each test shall be identified together with the number and reason for any rejects. Radiographs of any failed components shall be presented.

9.8 INITIAL ELECTRICAL MEASUREMENTS (PARA. 7)

All data shall be recorded against serial numbers. A histogram of component parameters shall be produced.

9.9 GROUP 1 - CONTROL GROUP DATA (PARA. 8.2)

All data shall be recorded against serial numbers.

9.10 SUBGROUP 2A - STEP-STRESS TESTS DATA (PARA. 8.3.2)

9.10.1 Subgroup 2A(i) - Thermal Resistance/Conductivity Data (Para. 8.3.2.2)

All data shall be recorded against serial numbers.

9.10.2 Subgroup 2A(ii) - Temperature Step-Stress Test Data (Para. 8.3.2.4)

All data shall be recorded against serial numbers. This shall include:

(a) Starting temperature.

(b) Temperature steps.

(c) Electrical measurements tabulated for each step.

(d) Graphical output as defined in Para. 8.3.2.6.

(e) Analysis of any failed components as defined in Para. 8.1.

(f) Thermal resistance/conductivity measurements from surviving components as defined in Para. 8.3.2.2.

9.10.3 Subgroup 2A(iii) - Power Step-Stress Test Data (Para. 8.3.2.5) (if applicable)
All data shall be recorded against serial numbers. This shall include:

(a) Starting power.
(b) Power steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 8.3.2.6.
(e) Analysis of any failed components as defined in Para. 8.1.
(f) Thermal resistance/conductivity measurements from surviving components as defined in Para. 8.3.2.2.

9.11 SUBGROUP 2B - RADIATION TESTS DATA (PARA. 8.3.3)
All data shall be recorded against serial numbers. This shall include, as applicable:

(a) Total dose steady-state test data (i.e. the Total Dose Radiation Test Report).
(b) Single Event Effects test data.
(c) Displacement Damage test data.

9.12 SUBGROUP 2C - CONSTRUCTION ANALYSIS DATA (PARA. 8.3.4)
All data shall be recorded against serial numbers. This shall include:

(a) Internal water vapour content data.
(b) Outgassing data (if applicable).
(c) External Visual Photographs.
(d) SEM photographs.
(e) Results of bond strength test (if applicable).
(f) Results of Die Shear Strength or Substrate Attach Strength or Bond Shear (Flip-Chip) (as applicable).
(g) Glassivation layer integrity test data (if applicable).
(h) Microsectioning photographs.
(i) Lid Attach Strength results.
(j) Terminal Strength test results.

9.13 SUBGROUP 2D - PACKAGE TESTS DATA (PARA. 8.3.5)
All data shall be recorded against serial numbers. This shall include:

(a) Subgroup 2D(i) - Thermal tests data.
(b) Subgroup 2D(ii-a), 2D(ii-b) (if applicable) and 2D(ii-c) - Mechanical and Thermal Vacuum tests data.
(c) Subgroup 2D(iii) - Resistance to soldering heat test data.
(d) Subgroup 2D(iv) - Pin to pin isolation test data.
(e) Subgroup 2D(v) - Humidity test data (if applicable).

9.14 SUBGROUP 2E - ELECTRICAL TESTS DATA (PARA. 8.3.6)
All data shall be recorded against serial numbers. This shall include:

(a) ESDS test data.
(b) Characterisation data.

9.15 SUBGROUP 2F – WAFER TEST DATA (PARA. 8.3.7)
All data shall be recorded against serial numbers. This shall include:

(a) Bump Shear test data (if applicable).

9.16 GROUP 3 - ENDURANCE TESTS DATA (PARA. 8.4)

9.16.1 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test Data (Para. 8.4.2)
All data shall be recorded against serial numbers.

9.16.2 Subgroup 3B - Accelerated Electrical Endurance Test Data (Para. 8.4.3)
All data shall be recorded against serial numbers. This shall include:

(a) Temperatures T1, T2 and T3 chosen.

(b) Power chosen.

(c) Electrical measurements tabulated and plotted for each intermediate time as defined in Para. 8.4.3.

(d) Drift values referred to the initial electrical measurements (Para. 7).

(e) Analysis of any failed components as defined in Para. 8.1.

9.16.3 Subgroup 3C - Extended Burn-in Test Data (Para. 8.4.4) (If Applicable)
All data shall be recorded against serial numbers.

9.16.4 Subgroup 3D - Extended Life Test Data (Para. 8.4.5)
All data shall be recorded against serial numbers.

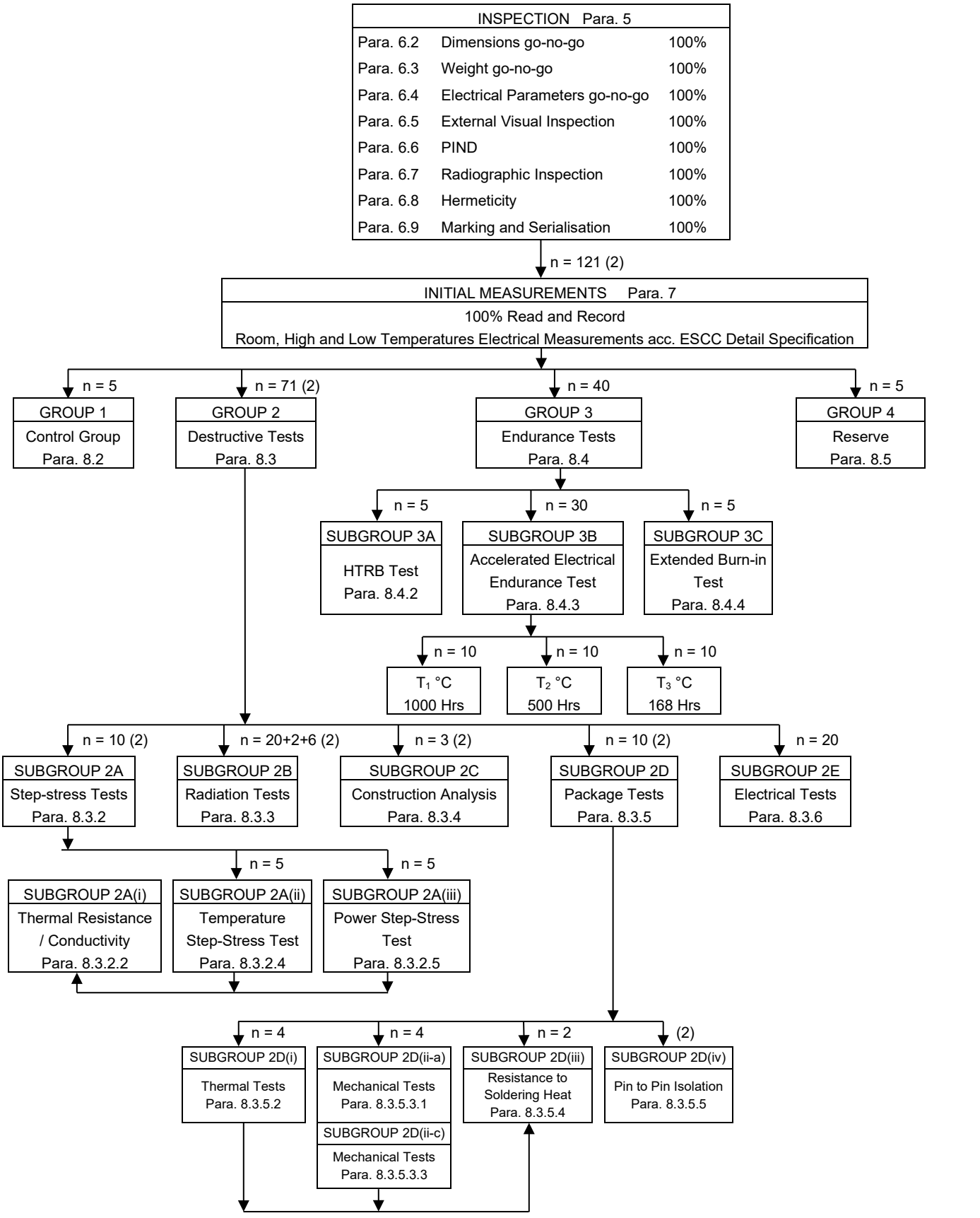
9.17 GROUP 4 - RESERVE DATA (PARA. 8.5) (IF APPLICABLE)
All data shall be recorded against serial numbers.

9.18 SUMMARY OF RESULTS AND CONCLUSIONS
The above shall be briefly reviewed, indicating the success or otherwise of the evaluation test programme.

Any production screens that need to be introduced into the PID shall be outlined.

CHART I – EVALUATION TEST PROGRAMME

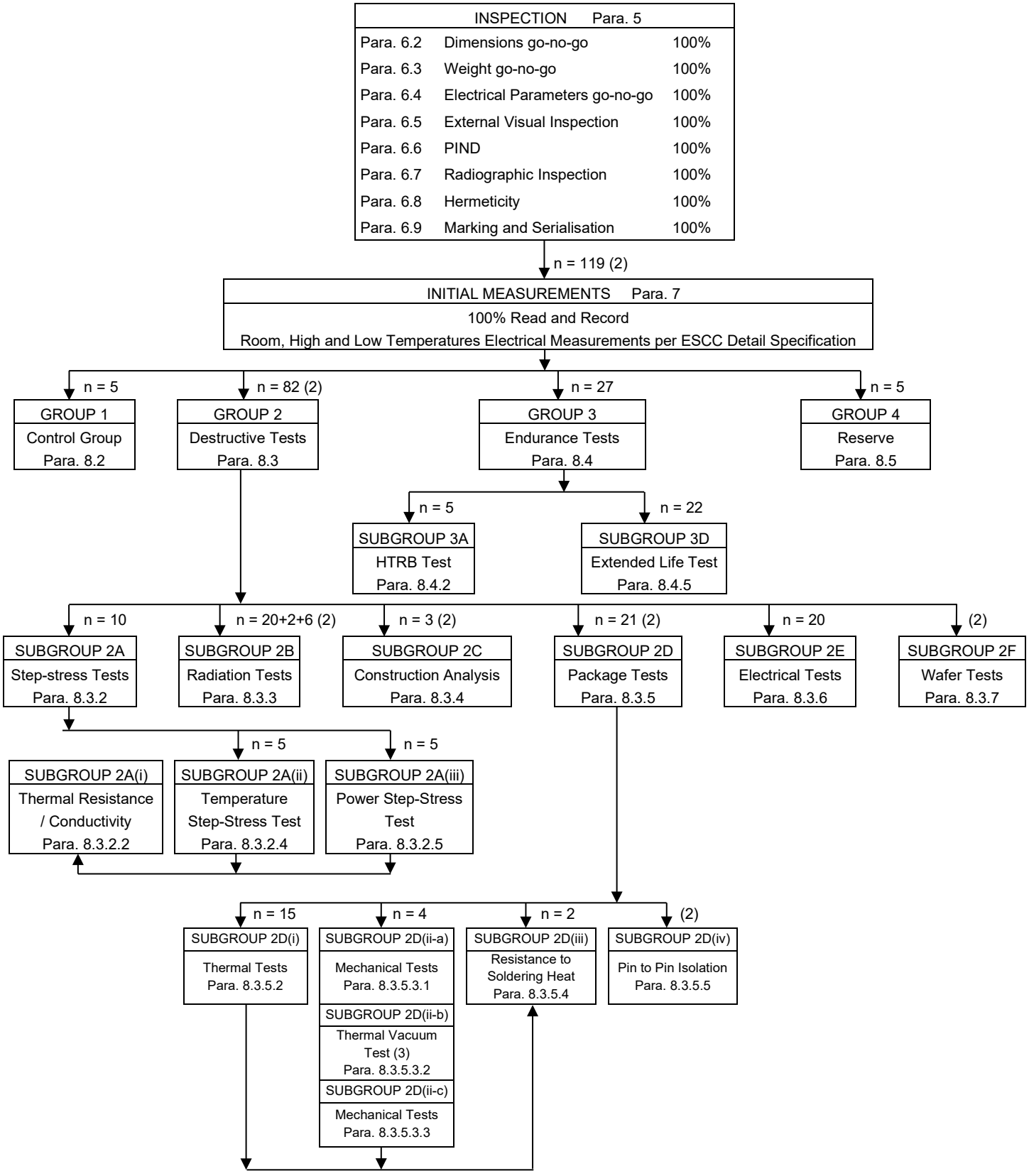
CHART IA - EVALUATION TEST PROGRAMME FOR WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. Unless otherwise specified, the quantity of components required for testing in each Group/Subgroup is indicated by the letter n.
2. Additional test components/structures/materials may also be required. See Para. 5.1 and the reference paragraph for details.

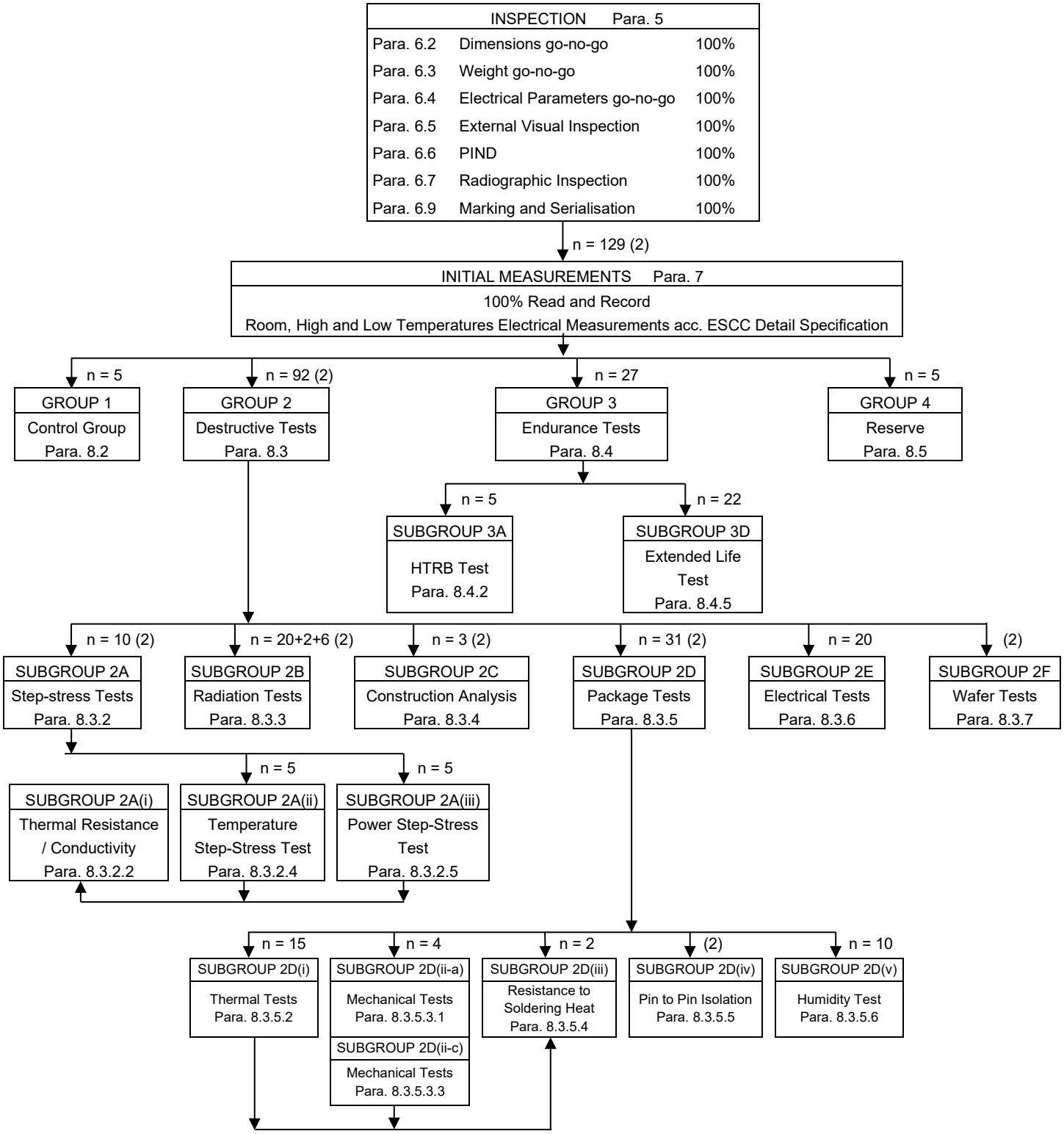
CHART IB - EVALUATION TEST PROGRAMME FOR HERMETIC FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. Unless otherwise specified, the quantity of components required for testing in each Group/Subgroup is indicated by the letter n.
2. Additional test components/structures/materials may also be required. See Para. 5.1 and the reference paragraph for details.
3. Thermal Vacuum Test shall only be performed on components which have thermal interface material between the die and the lid / heat-spreader.

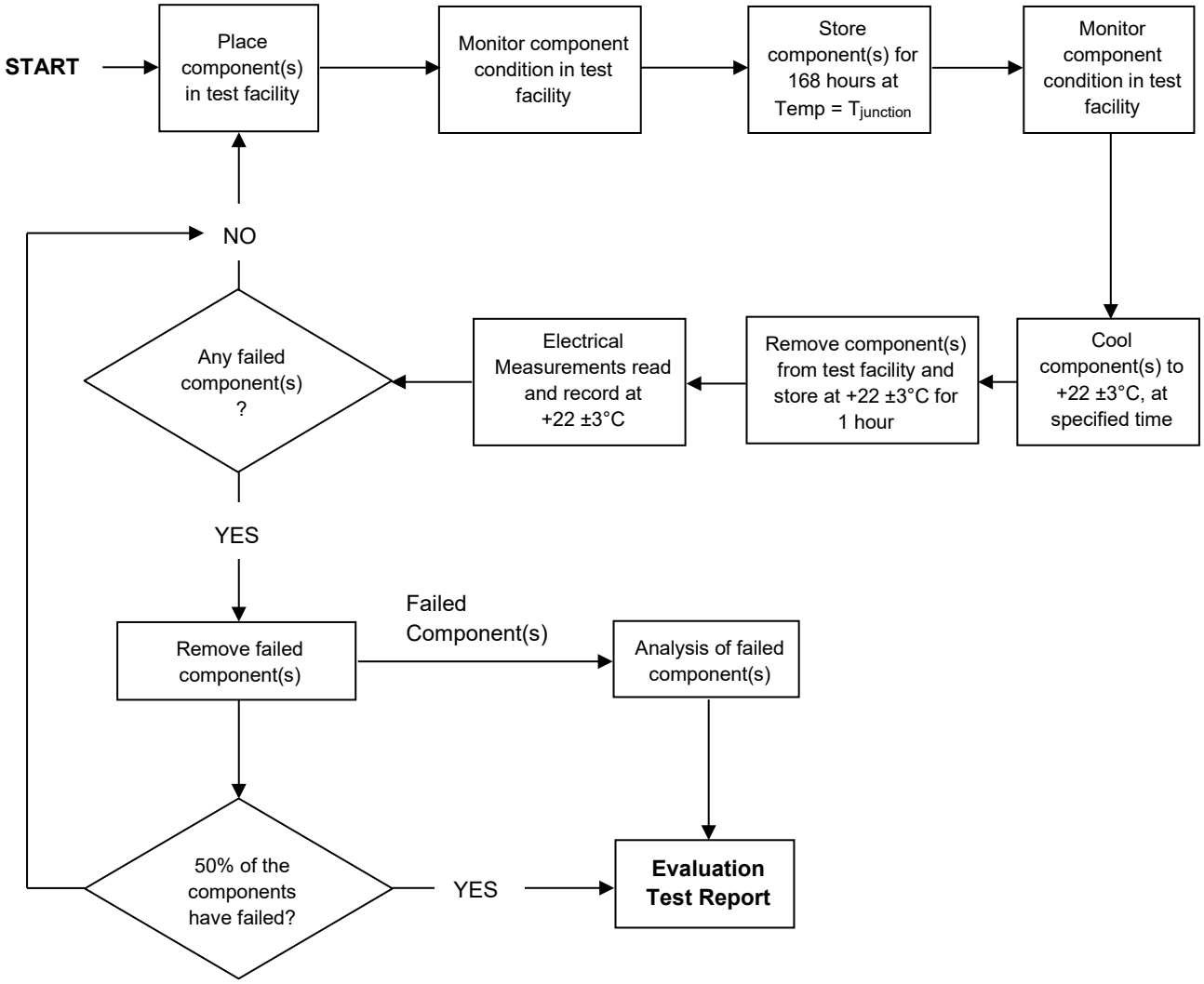
CHART IC - EVALUATION TEST PROGRAMME FOR NON-HERMETIC FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. Unless otherwise specified, the quantity of components required for testing in each Group/Subgroup is indicated by the letter n.
2. Additional test components/structures/materials may also be required. See Para. 5.1 and the reference paragraph for details.

CHART II – TEMPERATURE STEP-STRESS SEQUENCE (SEE PARA. 8.3.2.4)



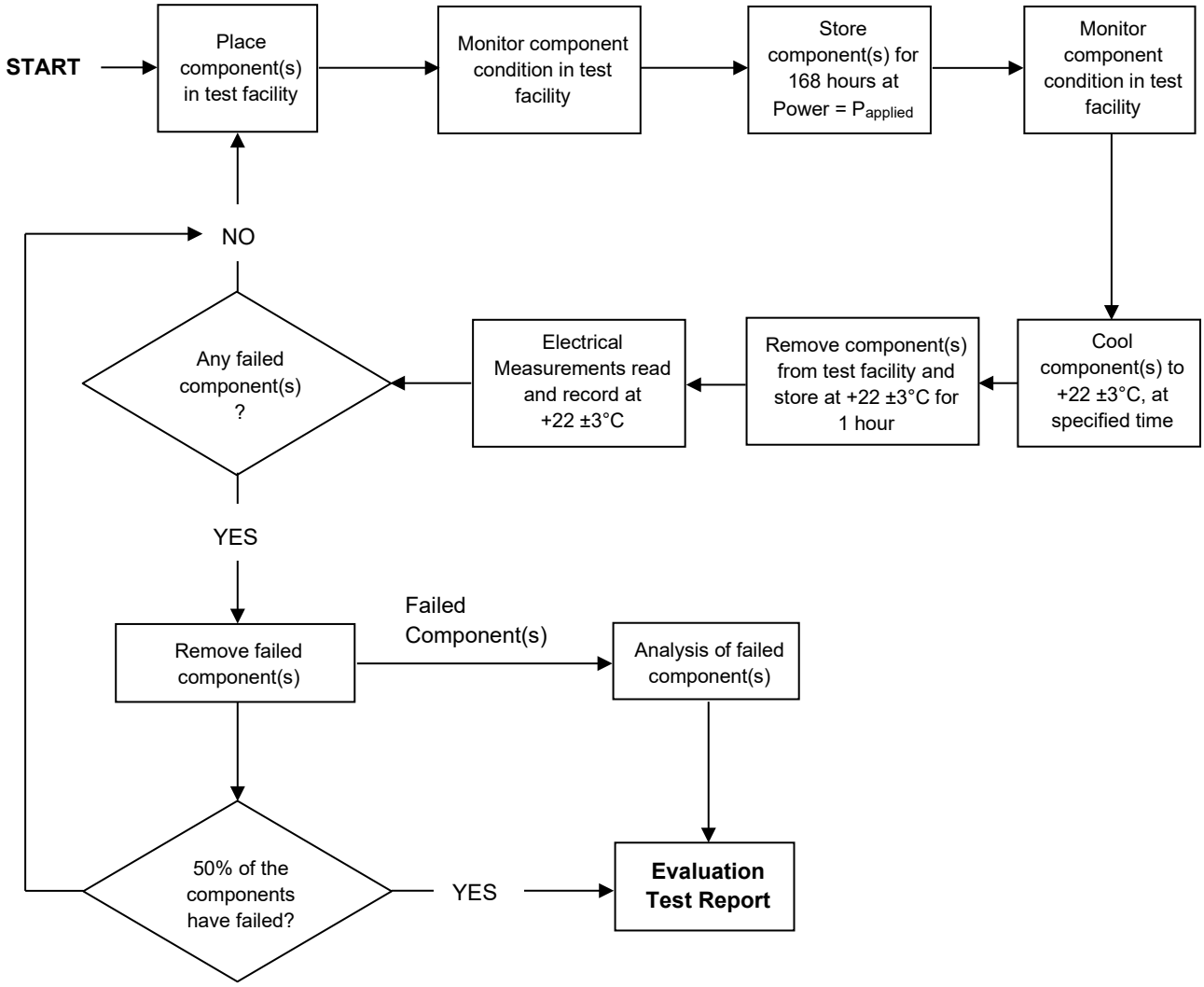
NOTES

1. Temperature steps with $T_{junction}$:

First step:	T_0	(°C)
	T_1	(°C)
	T_2	(°C)
Last step:	T_n	(°C)

with (T_n > … T_2 > T_1 > T_0)

CHART III - POWER STEP-STRESS SEQUENCE (SEE PARA. 8.3.2.5)



NOTES

1. Power steps with $P_{applied}$:

First step:	P_0	(W)
	P_1	(W)
	P_2	(W)
Last step:	P_n	(W)

with (P_n > … P_2 > P_1 > P_0)

CHART IV – ACCELERATED ELECTRICAL ENDURANCE TEST (SEE PARA. 8.4.3)

