DIODE, SILICON, SWITCHING

BASED ON TYPE 1N6640U

ESCC Detail Specification No. 5101/027

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DCR No.	CHANGE DESCRIPTION
1696	Specification updated to incorporate changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 510102707

- Detail Specification Reference: 5101027
- Component Type Variant Number: 07

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Breakdown Voltage $V_{(BR)}$ (V)	Working Peak Reverse Voltage V_{RWM} (V)	Terminal Finish (Note 1)	Weight max g
07	1N6640U	LCC2D	75	50	2 (Note 2)	0.12
08	1N6640U	LCC2D	75	50	4	0.12

NOTES:

1. The terminal finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. With electrolytic nickel underplating.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Forward Surge Current	I_{FSM}	2	A	Notes 1, 2
Working Peak Reverse Voltage	V_{RWM}	Note 3	V	
Average Output Rectified Current	I_O	300	mA	Note 4
Operating Temperature Range (Case Temperature)	T_{op}	-65 to +175	°C	Note 5
Junction Temperature	T_j	+175	°C	
Storage Temperature Range	T_{stg}	-65 to +175	°C	Note 5
Soldering Temperature	T_{sol}	+245	°C	Note 6
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	60	°C/W	Note 7
Thermal Resistance, Junction to Ambient	$R_{th(j-a)}$	280	°C/W	

NOTES:

1. Sinusoidal pulse of 8.3ms duration.
2. At $T_{amb} \leq +25$ºC.
3. See Para. 1.4.2 for V_{RWM} value.
4. At $T_{case} \geq +155$ºC, derate linearly to 0A at +175ºC.
5. For Variants with hot solder dip lead finish, all testing and any handling performed at $T_{amb} > +125$ºC shall be carried out in a 100% inert atmosphere.
6. Duration 5s maximum and the same package shall not be resoldered until 3 minutes have elapsed.
7. Package mounted on an infinite heat sink.

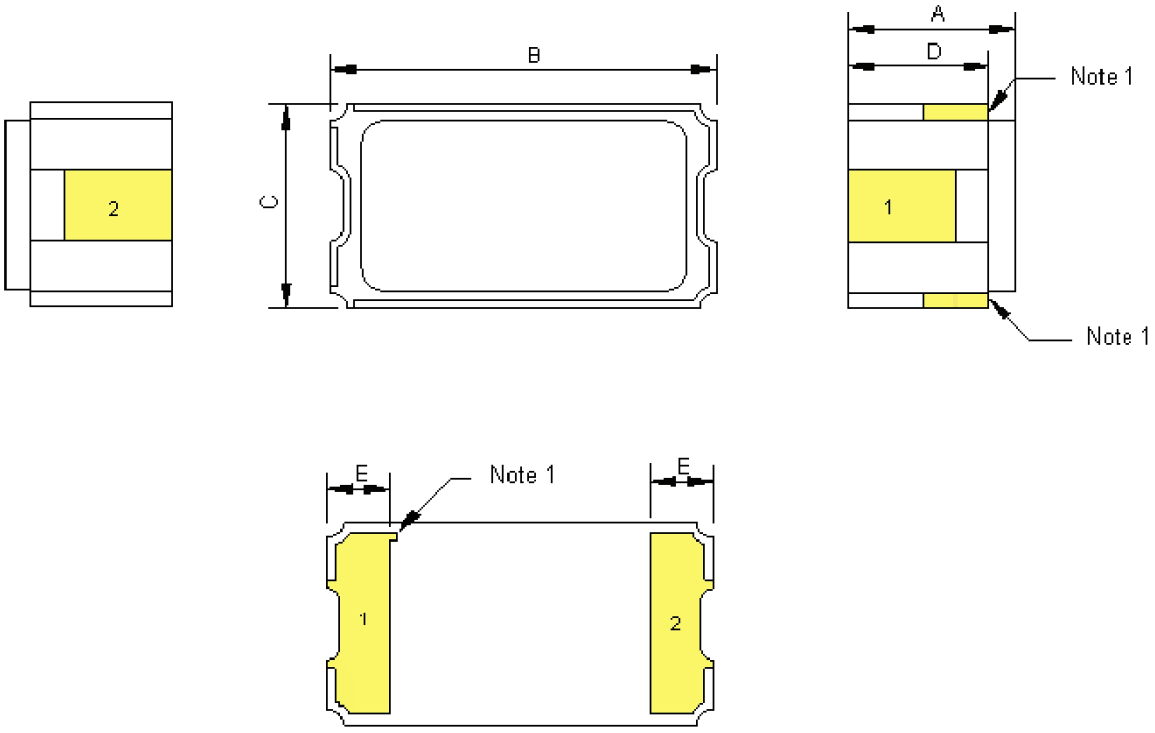
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 5800 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Leadless Chip Carrier Package (LCC2D) - 2 Terminal

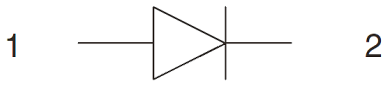


Symbols	Dimensions mm		Notes
	Min	Max	
A	1.86	2.2	2
B	4.44	4.77	
C	1.84	2.1	
D	1.53	1.87	
E	0.48	0.71	

NOTES:
1. Terminal identification: The anode is identified by metallisation in the two castellations and by the index mark on the bottom metallisation.
2. For Variant 08, dimension limits apply prior to solder coating of terminals.

1.8 FUNCTIONAL DIAGRAM

Terminal 1: Anode
Terminal 2: Cathode



NOTES
1. For LCC2D, the lid is not connected to any terminal.

1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

(a) Case
The case shall be hermetically sealed and have an Aluminium Nitride body with a Kovar lid.

(b) Terminal Finish
As specified in Para. 1.4.2.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Qualification and Periodic Tests – Chart F4

(a) Internal Gas Analysis: Shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal Identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables; see Para. 2.3.3.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3ºC.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Forward Voltage 1	V_{F1}	4011	Pulse Method I_F = 1mA, Note 1	0.54	0.63	V
Forward Voltage 2	V_{F2}	4011	Pulse Method I_F = 50mA, Note 1	0.76	0.89	V

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Forward Voltage 3	V_{F3}	4011	Pulse Method I_F = 100mA, Note 1	0.82	0.98	V
Forward Voltage 4	V_{F4}	4011	Pulse Method I_F = 200mA, Note 1	0.87	1.1	V
Reverse Current 1	I_{R1}	4016	DC Method $V_R = V_{RWM}$, Note 2	-	40	nA
Reverse Current 2 (Breakdown Voltage)	I_{R2}	4016	DC Method $V_R = V_{(BR)}$, Note 2	-	50	nA
Capacitance	C	4001	V_R = 0V V_{sig} = 50mV (p-p) max f = 1MHz Note 3	-	3	pF
Reverse Recovery Time 1	t_{rr1}	4031	Test Condition A $I_F = I_R$ = 10mA I_{rr} = 1mA Note 4	-	9	ns
Reverse Recovery Time 2	t_{rr2}	4031	Test Condition A I_F = 1A, V_R = 30V dI/dt = -15A/µs Note 3	-	20	ns
Forward Recovery Time	t_{fr}	4026	I_F = 200mA $V_{fr} = 1.1V_F$ Note 3	-	20	ns
Forward Recovery Voltage	V_{fr}	4026	I_F = 200mA $V_{fr} = 1.1V_F$ Note 3	-	5	V
Thermal Impedance, Junction to Ambient	$Z_{th(j-a)}$	3101	I_H = 0.1A to 0.3A t_H = 50ms to 10s I_M = 10mA t_{MD} = 100µs Note 5	Calculate ΔV_F see Note 6		°C/W

2.3.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 7	Limits		Units
				Min	Max	
Forward Voltage 4	V_{F4}	4011	T_{amb} = -55 (+5 -0)°C Pulse Method I_F = 200mA, Note 1	-	1.2	V
Reverse Current 1	I_{R1}	4016	T_{amb} = +150 (+0 -5)°C DC Method $V_R = V_{RWM}$, Note 2	-	30	µA

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 7	Limits		Units
				Min	Max	
Reverse Current 2 (Breakdown Voltage)	I_{R2}	4016	T_{amb} = -55 (+5 -0)°C DC Method $V_R = V_{(BR)}$, Note 2	-	40	µA

2.3.3 Notes to Electrical Measurements Tables

1. Pulse Width ≤ 680µs, Duty Cycle ≤ 2%.
2. See Para. 1.4.2 for V_{RWM} and $V_{(BR)}$ values.
3. Read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
4. Guaranteed by t_{rr2} but not tested.
5. Performed only during Screening Tests Parameter Drift Values (Initial Measurements), go-no-go.
6. The limits for ΔV_F shall be defined by the Manufacturer on every lot in accordance with MIL-STD-750 Method 3101 and shall guarantee the R_{th} limits specified in Para. 1.5 Maximum Ratings.
7. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3ºC.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Forward Voltage 4	V_{F4}	±0.03	-	1.1	V
Reverse Current 1	I_{R1}	±10 or (1) ±100%	-	40	nA

NOTES:

1. Whichever is the greater referred to the initial value.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3ºC.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits		Units
		Min	Max	
Forward Voltage 4	V_{F2}	0.87	1.1	V
Reverse Current 1	I_{R1}	-	40	nA
Reverse Current 2 (Breakdown Voltage)	I_{R2}	-	50	nA

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Limits	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	ºC
Reverse Voltage	V_R	0.8 x $V_{(BR)}$ (Note 1)	V
Duration	t	≥ 48	hours

NOTES:

1. See Para. 1.4.2 for $V_{(BR)}$ value.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	ºC
Junction Temperature	T_J	+175 (+0 -5)	ºC
Average Output Rectified Current	I_O	Note 1	mA

NOTES:

1. The output current may be adjusted, within the given limit range, to attain the specified junction temperature.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in; see Para. 2.7.

APPENDIX A
AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1 Deviations from the Generic Specification: Para. 8, Test Methods and Procedures	For qualification and qualification maintenance, or procurement of qualified or unqualified components, the following replacement test method specifications shall be used instead of the following ESCC Basic Specifications: • No. 20400, Internal Visual Inspection: replaced by MIL-STD-750 Test Method 2078. • No. 20500, External Visual Inspection: replaced by MIL-STD-750 Test Method 2071. • No. 20900, Radiographic Inspection of Electronic Components: replaced by MIL-STD-750 Test Method 2076.
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Special In-Process Controls - Chart F2	Internal Visual Inspection. Wedge bonds equal to 1.1 wire diameters are acceptable for bonding with a V-Groove tool.
	Internal Visual Inspection. For CCP packages, the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics control plans internal procedure as specified in the PID.
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.
Para. 2.3.1 Room Temperature Electrical Measurements	All AC characteristics (C, t_{rr}, t_{fr}, V_{fr}) may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics “Acceptation wafers” internal procedure as specified in the PID, which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Para. 2.3.2 High and Low Temperatures Electrical Measurements	Low temperature characteristic I_{R2} may be considered guaranteed but not tested if successful pilot lot testing has been performed in accordance with STMicroelectronics “Acceptation wafers” internal procedure, on the wafer lot as specified in the PID, which includes low temperature characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.