



**CAPACITORS, MICROWAVE, SILICON, MOS, DIE  
BASED ON TYPES 101M, 201M, 400M AND 401M**

**ESCC Detail Specification No. 5711/002**

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DCR No.	CHANGE DESCRIPTION
1571, 1594	Specification upissued to incorporate changes per DCR.

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**1 GENERAL**

**1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

**1.2 APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. [5010](#)
- (b) [MIL-STD-750](#), Test Methods and Procedures for Semiconductor Devices

**1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. [21300](#) shall apply.

**1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS**

**1.4.1 The ESCC Component Number**

The ESCC Component Number shall be constituted as follows:

Example: 5711002012C2KG

- Detail Specification Reference: 5711002
- Component Type Variant Number: 01 (as required)
- Characteristic code: Capacitance Value (2.2pF): 2C2 (as required)
- Characteristic code: Tolerance ( $\pm 10\%$ ): K (as required)
- Rating code: Rated Voltage (200V): G (as required)

**1.4.1.1 Characteristics and Ratings Codes**

Characteristics and ratings to be codified as part of the ESCC Component Number shall be as follows:

- (a) Rated Capacitance Value  $C_n$  expressed by means of the following codes in accordance with ESCC Basic Specification No. [21700](#). The unit quantity shall be picofarads (pF):

Capacitance Value $C_n$ (pF)	Code
0.XX	CXX
X.X	XCX
XX	XX0
XX10 <sup>1</sup>	XX1

- (b) Capacitance Tolerance expressed by the following codes in accordance with ESCC Basic Specification No. [21700](#):

Tolerance ( $\pm \%$ )	Code Letter
10	K
20	M

(c) Rated Voltage expressed by the following codes:

Rated Voltage $U_R$ (V)	Code Letter
40	B
100	E
200	G
400	K

1.4.2 Component Type Variants and Range of Components

The component type variants and the associated range of components applicable to this specification are as follows:

Variant Number	Based on Type	Capacitance Values $C_n$ (pF)	Capacitance Tolerance ( $\pm$ %)	Rated Voltage $U_R$ (V)
01	201M106C	2.2, 2.7, 3.3	10, 20	200
02	101M106C	3.9, 4.7, 5.6, 6.8	10, 20	100
03	400M106C	8.2, 10, 12, 15	10, 20	40
04	201M107C	3.9, 4.7, 5.6, 6.8, 8.2	10, 20	200
05	101M107C	10, 12, 15	10, 20	100
06	400M107C	18, 22, 27, 33, 39	10, 20	40
07	201M108C	10, 12, 15, 18	10, 20	200
08	101M108C	22, 27, 33, 39	10, 20	100
09	400M108C	47, 56, 68	10, 20	40
10	400M110C	82, 100	10, 20	40
11	201M106A	0.22, 0.27, 0.33, 0.39, 0.47, 0.56, 0.68, 0.82, 1, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3	10, 20	200
12	101M106A	3.9, 4.7, 5.6, 6.8	10, 20	100
13	400M106A	8.2, 10, 12, 15	10, 20	40
14	201M104A	3.9, 4.7, 5.6, 6.8	10, 20	200
15	101M104A	10, 12	10, 20	100
16	400M104A	18, 22, 27	10, 20	40
17	201M107A	8.2	10, 20	200
18	101M107A	15	10, 20	100
19	400M107A	33, 39	10, 20	40
20	201M108A	10, 12, 15, 18	10, 20	200
21	101M108A	22, 27, 33, 39	10, 20	100
22	400M108A	47, 56, 68	10, 20	40
23	400M110A	82, 100	10, 20	40
24	401M111J	0.125 (Note 1)	10, 20	200 (2)
25	201M111J	0.25 (Note 1)	10, 20	200

Variant Number	Based on Type	Capacitance Values $C_n$ (pF)	Capacitance Tolerance ( $\pm$ %)	Rated Voltage $U_R$ (V)
26	101M111J	0.5 (Note 1)	10, 20	100
27	401M112J	0.2 (Note 1)	10, 20	200 (2)
28	201M112J	0.4 (Note 1)	10, 20	200
29	101M112J	0.8 (Note 1)	10, 20	100
30	400M113J	10 (Note 1)	10, 20	40
31	400M114J	10 (Note 1)	10, 20	40

**NOTES:**

1. Capacitor arrays with several bond pads. The capacitance value refers to  $C_n$ , the smallest individual rated capacitance value available on the die. Multiples of  $C_n$  also available on the die shall be as specified in Para. 1.7 for the particular Variant.
2. Oxide Nominal Rated Voltage = 400V, and Oxide Breakdown Voltage = 600V, tested only during wafer fabrication.

1.5 **MAXIMUM RATINGS**

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Rated Voltage	$U_R$	See Para. 1.4.2	V	
Breakdown Voltage	$V_{BR}$	$1.5U_R$	V	Minimum
Operating Temperature Range	$T_{op}$	-55 to +150	°C	$T_{amb}$
Storage Temperature Range	$T_{stg}$	-55 to +175	°C	
Die Attach Temperature	$T_{die}$	+320	°C	Note 1

**NOTES:**

1. Duration 30 seconds maximum.

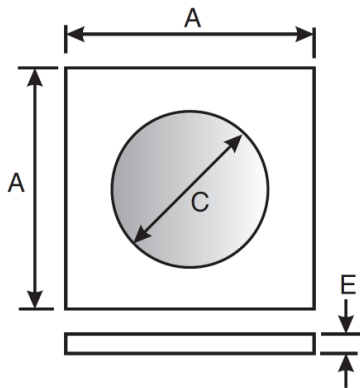
1.6 **HANDLING PRECAUTIONS**

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 1000V.

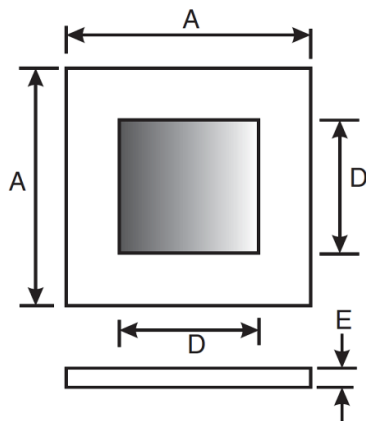
1.7 PHYSICAL DIMENSIONS

1.7.1 Variants 01 to 10



Symbols	Dimensions mm		Variant Number
	Min	Max	
A	0.34	0.4	01, 02, 03
	0.54	0.6	04, 05, 06
	0.74	0.8	07, 08, 09
	0.94	1	10
ØC	0.145	0.31	01, 02, 03
	0.31	0.49	04, 05, 06
	0.54	0.66	07, 08, 09
	0.72	0.78	10
E	0.16	0.22	All

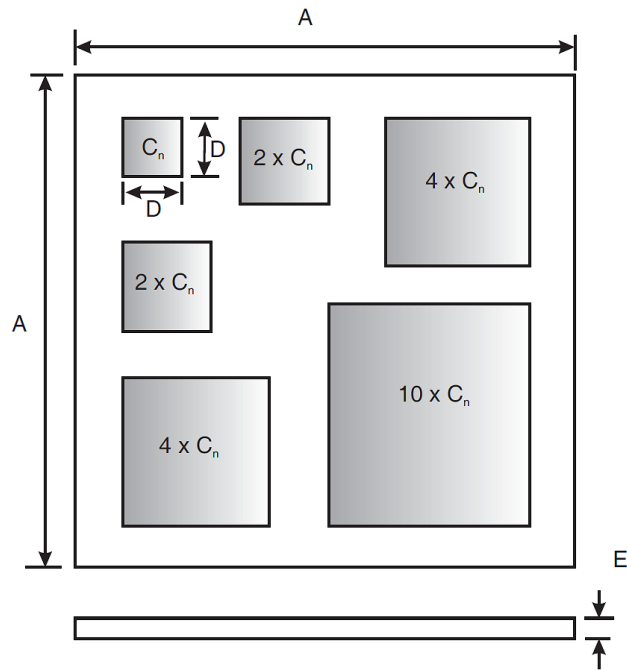
1.7.2 Variants 11 to 23



Symbols	Dimensions mm		Variant Number
	Min	Max	
A	0.3	0.4	11, 12, 13
	0.44	0.54	14, 15, 16
	0.5	0.6	17, 18, 19
	0.7	0.8	20, 21, 22
	0.9	1	23
D	0.22	0.28	11, 12, 13
	0.34	0.38	14, 15, 16
	0.4	0.44	17, 18, 19
	0.54	0.64	20, 21, 22
	0.68	0.78	23
E	0.16	0.22	All



1.7.3 Variants 24, 25, 26

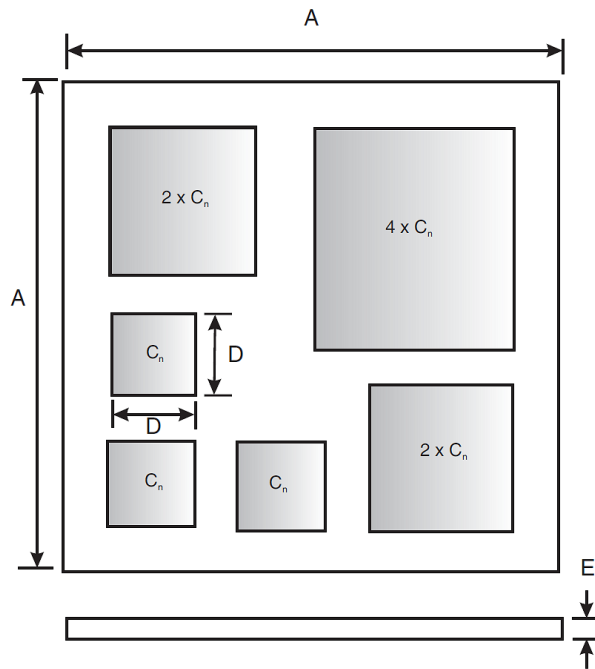


Symbols	Dimensions mm		Notes
	Min	Max	
A	0.4	0.5	
D	0.06	0.08	1
E	0.16	0.22	

**NOTES:**

1. Dimension of the smallest bond pad area, specified for bonding purposes.

1.7.4 Variants 27, 28 and 29

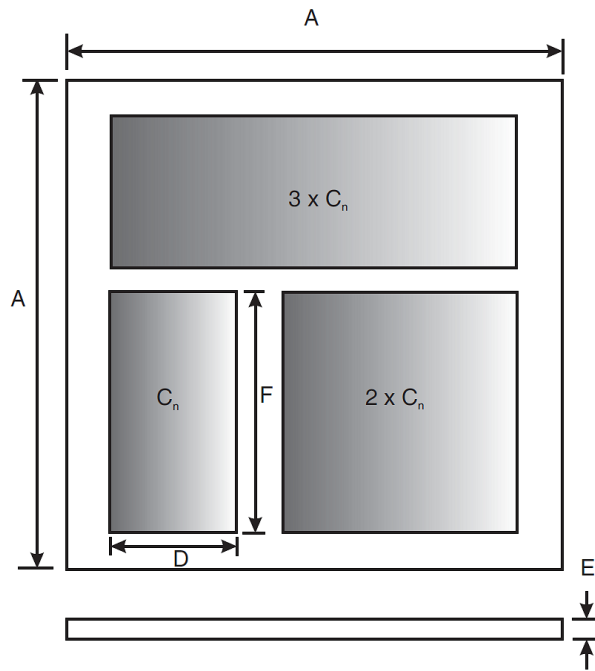


Symbols	Dimensions mm		Notes
	Min	Max	
A	0.4	0.5	
D	0.08	0.1	1
E	0.16	0.22	

**NOTES:**

1. Dimension of the smallest bond pad area, specified for bonding purposes.

1.7.5 Variant 30

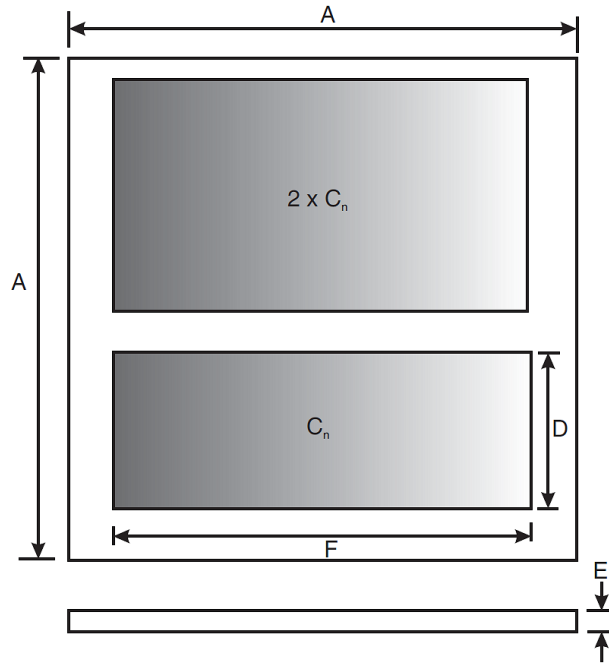


Symbols	Dimensions mm		Notes
	Min	Max	
A	0.65	0.75	
D	0.17	0.19	1
E	0.16	0.22	
F	0.26	0.28	1

**NOTES:**

1. Dimension of the smallest bond pad area, specified for bonding purposes.

1.7.6 Variant 31

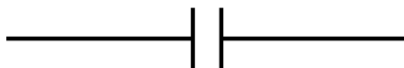


Symbols	Dimensions mm		Notes
	Min	Max	
A	0.45	0.55	
D	0.1	0.12	1
E	0.16	0.22	
F	0.39	0.41	1

**NOTES:**

1. Dimension of the smallest bond pad area, specified for bonding purposes.

1.8 FUNCTIONAL DIAGRAM



1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

- (a) **Bond Pad**  
The bond pad metallisation shall be TiAu with a layer of vacuum-deposited gold, thickness  $\geq 0.25\mu\text{m}$  and a final layer of electrolytic gold, thickness  $\geq 2.7\mu\text{m}$ .
- (b) **Die Backface**  
The die backface metallisation shall be TiAu with a layer of gold, thickness  $\geq 0.5\mu\text{m}$ .
- (c) **Glassivation**  
The material of the capacitor dielectric shall be oxide. The thickness of the oxide varies as required for each component's  $C_n$  and  $U_R$ .

## 2 REQUIREMENTS

### 2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

#### 2.1.1 Deviations from the Generic Specification

##### 2.1.1.1 *Deviations from Production Control - Chart F2*

- (a) A Metallisation Adhesion test shall be performed on a randomly selected sample of 5 die from each wafer lot, after Die Visual Inspection during Wafer Lot Acceptance.

Samples shall be subjected to a high temperature bake of +320 (+5 -0)°C for a period of 5 minutes minimum. The samples shall then be visually inspected.

Any evidence of lifting or peeling metallisation shall be cause for wafer lot failure.

This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

##### 2.1.1.2 *Deviations from Screening Tests for Die Components – Chart F3B*

- (a) Burn-in 1: Not applicable.  
(b) Parameter Drift Values  $\Delta 1$ : Not applicable.  
(c) Check for Lot Failure for Burn-in 1: Not applicable.

### 2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. [21700](#).

The information to be marked on the primary package and the order of precedence shall be as follows:

- (a) The ESCC qualified components symbol (for ESCC qualified components only).  
(b) The ESCC Component Number (see Para. 1.4.1).  
(c) Traceability information.

### 2.3 DIE SHEAR

In those cases where package clearances are such that a die shear test is not practicable, the die shall be pushed away with a suitable tool. The force required to remove the die need not be recorded. The die attachment area shall be inspected and the component shall be considered acceptable if more than 50% of the semiconductor material remains.

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

2.4.1 Room Temperature Electrical Measurements

The measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}\text{C}$ .

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Tolerance ( $\pm$ %)	Limits		Units
					Min	Max	
Capacitance	C	4001	$V_T = 0\text{V}$ , $f = 1\text{MHz}$	10 20	$0.9C_n$ $0.8C_n$	$1.1C_n$ $1.2C_n$	pF
Leakage Current	$I_{L1}$	4016	$V_T = U_R$	All	-	50	nA
Voltage Proof Leakage Current	$I_{L2}$	4016	$V_T = 1.5U_R$	All	-	100	nA

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Leakage Current	$I_{L1}$	4016	$T_{amb} = +150 (+0 -3)^{\circ}\text{C}$ $V_T = U_R$	-	100	nA

**NOTES:**

1. Measurements shall be performed on a sample basis as specified in the Generic Specification.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units	
		Drift Value $\Delta$	Absolute		
			Min		Max
Capacitance	C	$\pm 0.2$ or (1) $\pm 2\%$	Note 2		pF
Leakage Current	$I_{L1}$	$\pm 5$ or (1) $\pm 100\%$	-	50	nA

**NOTES:**

1. Whichever is the greater referred to the initial value.
2. As specified in Para. 2.4.1.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Capacitance	C	Note 1		pF
Leakage Current	$I_{L1}$	-	50	nA
Voltage Proof Leakage Current	$I_{L2}$	-	100	nA

**NOTES:**

1. As specified in Para. 2.4.1.

2.7 BURN-IN 2 CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+150 (+0 -3)	°C
Test Voltage	$V_T$	$U_R$	V

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.7.



**APPENDIX A**  
**AGREED DEVIATIONS FOR EXENS SOLUTIONS (F)**

Items Affected	Description of Deviations
Para. 2.1.1.1, Deviations from Production Control – Chart F2	<p>Assembly (Assembly of the Packaged Test Sublot for Naked Die Components): A minimum of 5 dice per wafer and 20 dice per wafer lot shall be assembled to make up the Packaged Test Sublot.</p> <p>Encapsulation: Encapsulation of the Packaged Test Sublot samples is optional at the Manufacturer's discretion.</p>