TRANSISTORS, POWER, MOSFET, N-CHANNEL, RAD-HARD

BASED ON TYPES BUY65CS08J-01 AND BUY65CS28A-01

ESCC Detail Specification No. 5205/033

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices
(c) MIL-STD-883, Test Method Standard Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520503301R

- Detail Specification Reference: 5205033
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	I_{DS} @ T_{case} ≤ +25°C max (A) (Note 1)	I_{DS} @ T_{case} = +100°C max (A) (Note 1)	$r_{DS(on)}$ @ T_{amb} = +25°C max (mΩ) (Note 2)	Case (Note 3)	Terminal Material and Finish (Note 4)	Weight max (g)	Total Dose Radiation Level Letter (Note 5)
01	BUY65CS08J-01	8	5	450	SMD0.5	Q14	1.1	R [100kRAD(Si)]
02	BUY65CS28A-01	28	18	150	SMD2	Q14	3.3	R [100kRAD(Si)]

NOTES:

1. See Para. 1.5.
2. See Para. 2.4.1.
3. See Para. 1.7.
4. The lead material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
5. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

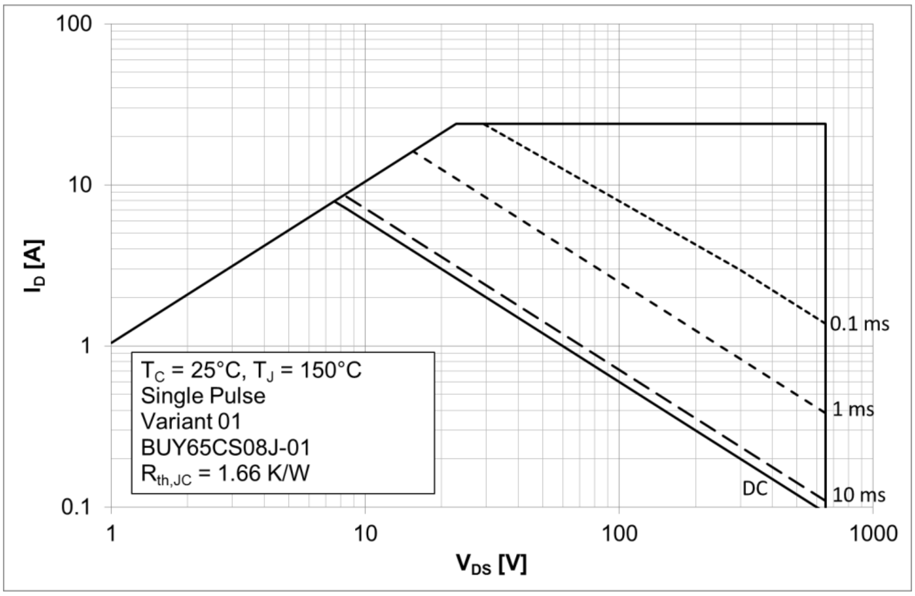
The maximum ratings shall not be exceeded at any time during use or storage.

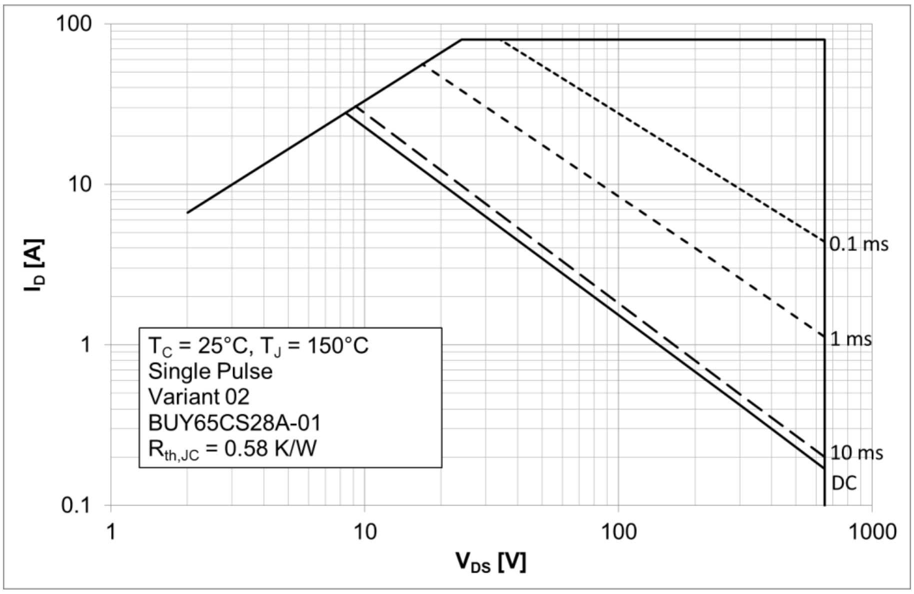
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Drain-Source Voltage	V_{DS}	650	V	Note 1
Gate-Source Voltage	V_{GS}	±20	V	
Drain Current (Continuous)	I_{DS}	Note 2	A	At T_{case} ≤ +25°C Notes 1, 3, 4
		Note 2	A	At T_{case} = +100°C Notes 3, 4
Drain Current (Pulsed) Variant 01: Variant 02:	I_{DM}	 24 80	Apk	At T_{case} ≤ +25°C Notes 1, 3
Power Dissipation Variant 01: Variant 02:	P_{tot}	 75 215	W	Note 5
Avalanche Energy (Single Pulse) Variant 01: Variant 02:	E_{AS}	 100 200	mJ	
Operating Temperature Range	T_{op}	-55 to +150	°C	T_{amb}
Storage Temperature Range	T_{stg}	-55 to +150	°C	
Junction Temperature	T_j	+150	°C	
Soldering Temperature	T_{sol}	+250	°C	Note 6
Thermal Resistance, Junction-to-Case Variant 01: Variant 02:	$R_{th(j-c)}$	 1.66 0.58	°C/W	

NOTES:

1. Safe Operating Area applies as follows:





2. See Para. 1.4.2 for I_{DS} value.
3. T_{case} is measured on the PCB at the soldering point to the Drain terminal.
4. For T_{case} > +25°C, derate as follows:

$$I_{DS} = \sqrt{\frac{T_{jmax} - T_{case}}{(R_{th(j\text{-}c)}) \times (r_{DS(on)} \text{at } T_{jmax})}}$$

where ($r_{DS(on)}$ at T_{jmax}) =
- Variant 01: 950mΩ
- Variant 02: 280mΩ

5. For T_{case} > +25°C, derate linearly to 0W at T_{case} = +150°C.
6. Duration 10 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

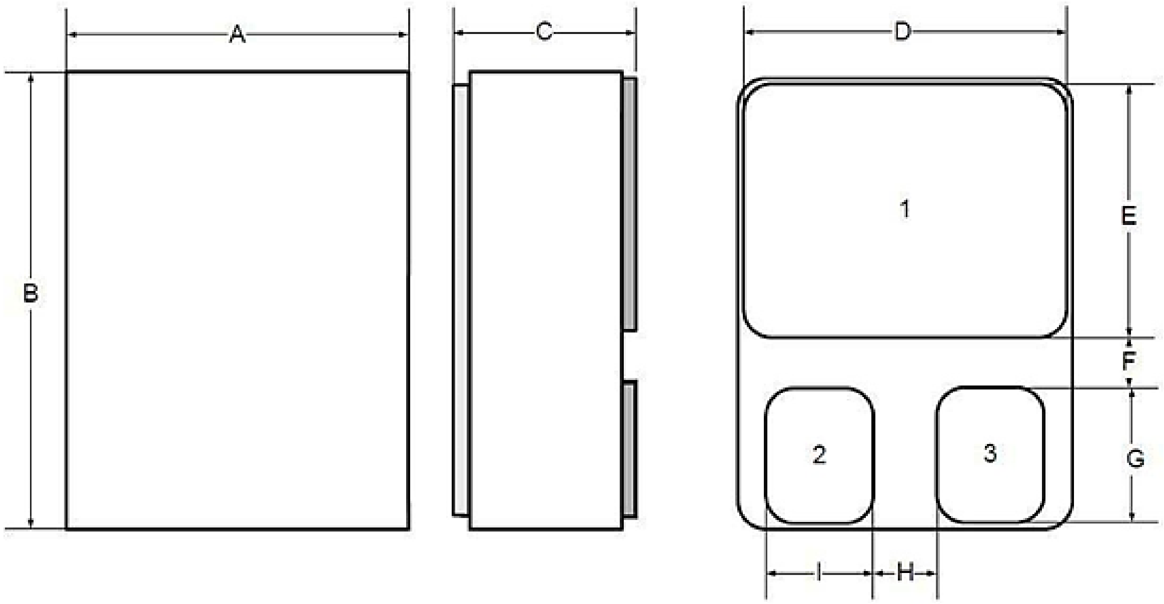
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000V.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Leadless Chip Carrier Package (SMD0.5 and SMD2) – 3 Terminals

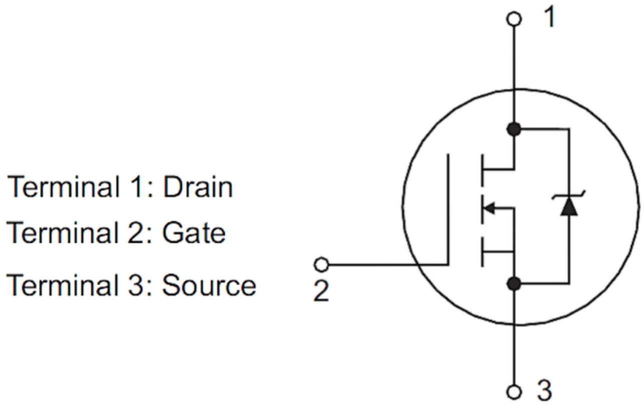


Symbols	Dimensions (mm)			
	Variant 01 (SMD0.5)		Variant 02 (SMD2)	
	Min	Max	Min	Max
A	7.35	7.69	13.14	13.54
B	9.97	10.41	17.3	17.75
C	-	3.3	-	3.75
D	7.14	7.39	11.05	11.3
E	5.59	5.84	11.94	12.19
F	0.76	-	0.89	-
G	2.92	3.18	3.86	4.11
H	0.76	-	1.27	-
I	2.29	2.54	3.43	3.68

NOTES:

1. The terminal identification is specified by the component’s geometry. The terminal identification shall be: terminal 1 = Drain, terminal 2 = Gate, terminal 3 = Source.

1.8 FUNCTIONAL DIAGRAM



NOTES:

1. The case is not connected to any terminal.

1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

(a) Case
The case shall be hermetically sealed and have a ceramic/metal body.

(b) Terminals
As specified in Para. 1.4.2 Component Type Variants.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) Verification of Safe Operating Area: The Safe Operating Area shall be verified by performing the Thermal Impedance ($Z_{th(j-c)}$) ΔV_{SD} test specified in Para. 2.4.1 Room Temperature Electrical Measurements.

(b) Particle Impact Noise Detection may be performed at any point after Temperature Cycling, prior to Seal.

(c) Power Burn-in: A high temperature steady-state gate bias test (HTGB; see Para. 2.8) shall be performed instead of Power Burn-in.

2.1.1.2 Deviations from Qualification and Periodic Tests - Chart F4

(a) Terminal Strength is not applicable.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) The ESCC Qualified Component symbol (for ESCC qualified components only).
(b) The ESCC Component Number (see Para. 1.4.1).
(c) Traceability information.

2.3 WAFER LOT ACCEPTANCE

A SEM inspection shall be performed as specified in the ESCC Generic Specification.

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables (see Para. 2.4.3).

2.4.1 Room Temperature Electrical Measurements

Unless otherwise specified, the measurements shall be performed at T_{amb} = +25 ±3°C.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	3407	V_{GS} = 0V, I_D = 0.25mA Bias condition C	650	-	V
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$, I_D = 1mA	2	4	V
Gate-to-Source Leakage Current	I_{GSS}	3411	V_{GS} = ±20V, V_{DS} = 0V Bias condition C	-100	+100	nA
Drain Current	I_{DSS}	3413	V_{GS} = 0V, V_{DS} = 520V Bias condition C	-	25	µA
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	V_{GS} = 10V Variant 01: I_D = 5A: Variant 02: I_D = 18A: Note 1	- -	450 150	mΩ
Source-to-Drain Diode Forward Voltage	V_{SD}	4011	V_{GS} = 0V Variant 01: I_{SD} = 8A: Variant 02: I_{SD} = 28A: Note 1	- -	1.2 1.2	V
Thermal Impedance	$Z_{th(j-c)}$	3161	Note 2 Variant 01: I_H = 1.19A: Variant 02: I_H = 2.37A:	- -	1.15 0.56	ºC/W
Turn-on Delay Time	$t_{d(on)}$	3472	V_{GS} = 10V, R_G = 4.7Ω, V_{DS} = 325V Variant 01: I_D = 5A: Variant 02: I_D = 18A: Note 3	- -	15 28	ns
Rise Time	t_r	3472	V_{GS} = 10V, R_G = 4.7Ω, V_{DS} = 325V Variant 01: I_D = 5A: Variant 02: I_D = 18A: Note 3	- -	10 20	ns

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Turn-off Delay Time	$t_{d(off)}$	3472	V_{GS} = 10V, R_G = 4.7Ω, V_{DS} = 325V			ns
			Variant 01: I_D = 5A:	-	45	
			Variant 02: I_D = 18A:	-	80	
			Note 3			
Fall Time	t_f	3472	V_{GS} = 10V, R_G = 4.7Ω, V_{DS} = 325V			ns
			Variant 01: I_D = 5A:	-	20	
			Variant 02: I_D = 18A:	-	15	
			Note 3			
Reverse Recovery Time	t_{rr}	3473	$V_{DD} \leq$ 50V, di/dt = 100A/µs			ns
			Variant 01: I_{SD} = 8A:	-	700	
			Variant 02: I_{SD} = 28A:	-	1080	
			Note 3			
Input Capacitance	C_{iss}	3431	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz			nF
			Variant 01:	1.3	1.7	
			Variant 02:	4.1	5.5	
			Note 3			
Output Capacitance	C_{oss}	3453	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz			pF
			Variant 01:	40	60	
			Variant 02:	120	170	
			Note 3			
Reverse Transfer Capacitance	C_{rss}	3433	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz			pF
			Variant 01:	3	6	
			Variant 02:	5	17	
			Note 3			
Total Gate Charge	Q_g	3471	V_{GS} = 10V, V_{DS} = 325V			nC
			Variant 01: I_{SD} = 8A:	-	30	
			Variant 02: I_{SD} = 28A:	-	85	
			Note 3			
Gate-to-Source Charge	Q_{gs}	3471	V_{GS} = 10V, V_{DS} = 325V			nC
			Variant 01: I_{SD} = 8A:	-	10	
			Variant 02: I_{SD} = 28A:	-	30	
			Note 3			
Gate-to-Drain Charge	Q_{gd}	3471	V_{GS} = 10V, V_{DS} = 325V			nC
			Variant 01: I_{SD} = 8A:	-	8	
			Variant 02: I_{SD} = 28A:	-	25	
			Note 3			

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions (Note 4)	Limits		Units
				Min	Max	
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	T_{amb} = +125 (+0 -5)°C $V_{DS} \geq V_{GS}$, I_D = 1mA	1.5	-	V
			T_{amb} = -55 (+5 -0) °C $V_{DS} \geq V_{GS}$, I_D = 1mA	-	5	V
Gate-to-Source Leakage Current	I_{GSS}	3411	T_{amb} = +125 (+0 -5)°C V_{GS} = ±20V, V_{DS} = 0V Bias condition C	-200	+200	nA
Drain Current	I_{DSS}	3413	T_{amb} = +125 (+0 -5)°C V_{GS} = 0V, V_{DS} = 520V Bias condition C	-	250	µA
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	T_{amb} = +125 (+0 -5)°C V_{GS} = 10V Variant 01: I_D = 5A: Variant 02: I_D = 18A: Note 1	- -	900 260	mΩ

2.4.3 Notes to Room, High and Low Temperatures Electrical Measurements

1. Pulsed measurement: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
2. The $Z_{th(j-c)}$ limit is guaranteed by performing a ΔV_{SD} (go-no-go) test. The following test conditions and limits shall also apply:
    - V_{DS} = 20V
    - t_M < 75µs
    - I_M = 10mA
    - t_H = 25ms
    - V_{SD} = 40mV minimum, 60mV maximum
3. Read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
4. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +25 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	±20%	2	4	V
Gate-to-Source Leakage Current	I_{GSS}	±20 or (1) ±100%	-100	+100	nA
Drain Current	I_{DSS}	±10 or (1) ±100%	-	25	µA
Static Drain-to-Source On Resistance (Note 2)	$r_{DS(on)}$				mΩ
Variant 01:		±20% (3)	-	450	
Variant 02:		±20% (3)	-	150	

NOTES:

1. Whichever is the greater.
2. Measured only prior to HTRB Burn-in and after HTGB Burn-in.
3. Referred to the measurement prior to HTRB Burn-in.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +25 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	±20%	2	4	V
Gate-to-Source Leakage Current	I_{GSS}	±20 or (1) ±100%	-100	+100	nA
Drain Current	I_{DSS}	±10 or (1) ±100%	-	25	µA
Static Drain-to-Source On Resistance	$r_{DS(on)}$				mΩ
Variant 01:		±20%	-	450	
Variant 02:		±20%	-	150	

NOTES:

1. Whichever is greater.

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

HTRB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition A with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	520 (Note 1)	V
Gate-to-Source Voltage	V_{GS}	0	V
Duration	t	240 minimum	Hours

NOTES:

1. Voltage may be switched off during cool down.

2.8 HIGH TEMPERATURE STEADY-STATE GATE BIAS BURN-IN CONDITIONS

HTGB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition B with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	0	V
Gate-to-Source Voltage	V_{GS}	16	V
Duration	t	48 minimum	Hours

2.9 OPERATING LIFE CONDITIONS

Operating Life shall consist of High Temperature Reverse Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition A, followed by High Temperature Steady-State Gate Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition B. The test conditions are as follows:

High Temperature Reverse Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	520 (Note 1)	V
Gate-to-Source Voltage	V_{GS}	0	V
Duration	t	1000 minimum	Hours

High Temperature Steady State Gate Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	0	V
Gate-to-Source Voltage	V_{GS}	16	V
Duration	t	1000 minimum	Hours

NOTES:

1. Voltage may be switched off during cool down.

2.10 TOTAL DOSE RADIATION TESTING

2.10.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

The following bias condition shall be used during irradiation testing:

- V_{GS} = +15V
- V_{DS} = 0V

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

2.10.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Para. 2.4.1 Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +25 ±3°C.

Unless otherwise specified the test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The parameters to be measured during irradiation testing and on completion of irradiation testing are shown below:

Characteristics	Symbols	Limits			Units
		Drift Values (Δ)	Absolute		
			Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	±20%	650	-	V
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	+10%, -50%	2	4	V
Gate-to-Source Leakage Current	I_{GSS}	±20	-100	+100	nA
Drain Current	I_{DSS}	-	-	25	µA
Static Drain-to-Source On Resistance	$r_{DS(on)}$				mΩ
Variant 01:		±20%	-	450	
Variant 02:		±20%	-	150	
Source-to-Drain Diode Forward Voltage	V_{SD}				V
Variant 01:		±10%	-	1.2	
Variant 02:		±10%	-	1.2	

APPENDIX ‘A’
AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Production Control - Chart F2	The 3 component sample Dimension Check need only be performed once on each component package production lot.
Para. 2.1.1.1 Deviations from Screening Tests - Chart F3	Temperature Cycling: shall be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C, 20 cycles at maximum storage temperature rating specified in the Detail Specification.
	High and Low Temperatures Electrical Measurements: may be performed at any point after High Temperature Steady-State Gate Bias Burn-in, prior to Seal, but shall still count towards Check for Lot Failure.
	Seal, Fine Leak: shall be performed in accordance with MIL-STD-883, Test Method 1014, Test Condition A1 or A2.
	Radiographic Inspection: is not applicable.
	Solderability: is not applicable unless otherwise stipulated in the Purchase Order.
Para. 2.1.1.2 Deviations from Qualification and Periodic Tests - Chart F4	Temperature Cycling: shall be performed in accordance with MIL- STD-883, Test Method 1010, Test Condition C, 100 cycles at maximum storage temperature rating specified in the Detail Specification.
	Seal, Fine Leak: shall be performed in accordance with MIL-STD-883, Test Method 1014, Test Condition A1 or A2.
Para. 2.2 Marking	For the purposes of marking of the ESCC Component Number on the body of the component, the Variant Number may be marked as a single digit (e.g. 1 for Variant 01).
Para. 2.4.1 Room Temperature Electrical Measurements	The read and record 32 component sample electrical measurements for characteristics $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, t_{rr}, C_{iss}, C_{oss}, C_{rss}, Q_g, Q_{gs} and Q_{gd} need only be performed once on each wafer lot used to supply components to this specification. Any failure shall result in rejection of the wafer lot. The sample measurement may be performed at any time during production.

ADDITIONAL DATA – INFINEON TECHNOLOGIES (D)

(a) Derating for Space Application

These components are susceptible to Single Event Gate Rupture if operated in a space environment unless the following derating is applied:

Single Event Safe Operating Area