INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS ANALOGUE MULTIPLEXER/DEMULTIPLEXER (SINGLE 16-CHANNEL)

BASED ON TYPE 4067B

ESCC Detail Specification No. 9408/009

Issue 4	November 2014

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
882	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 940800901

- Detail Specification Reference: 9408009
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and/or Finish	Weight max g
01	4067B	FP	G2	1.7
02	4067B	FP	G4	1.7
03	4067B	DIP	G2	5.2
04	4067B	DIP	G4	5.2
07	4067B	CCP	2	0.9
08	4067B	SO	G2	1.1
09	4067B	SO	G4	1.1

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 18	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	Notes 1, 2 Power on
Input Current	I_{IN}	±10	mA	-
Device Power Dissipation (Continuous)	P_D	200	mW	-
Power Dissipation per Output	P_{DSO}	100	mW	-
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	-
Soldering Temperature For FP, DIP and SO For CCP	T_{sol}	 +265 +245	^oC	 Note 3 Note 4

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$ with reference to V_{SS}.
2. To avoid draining V_{DD} supply current into the ON Channel when current flows from CHn to COM the voltage drop across the ON Channel shall not exceed 0.4V.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

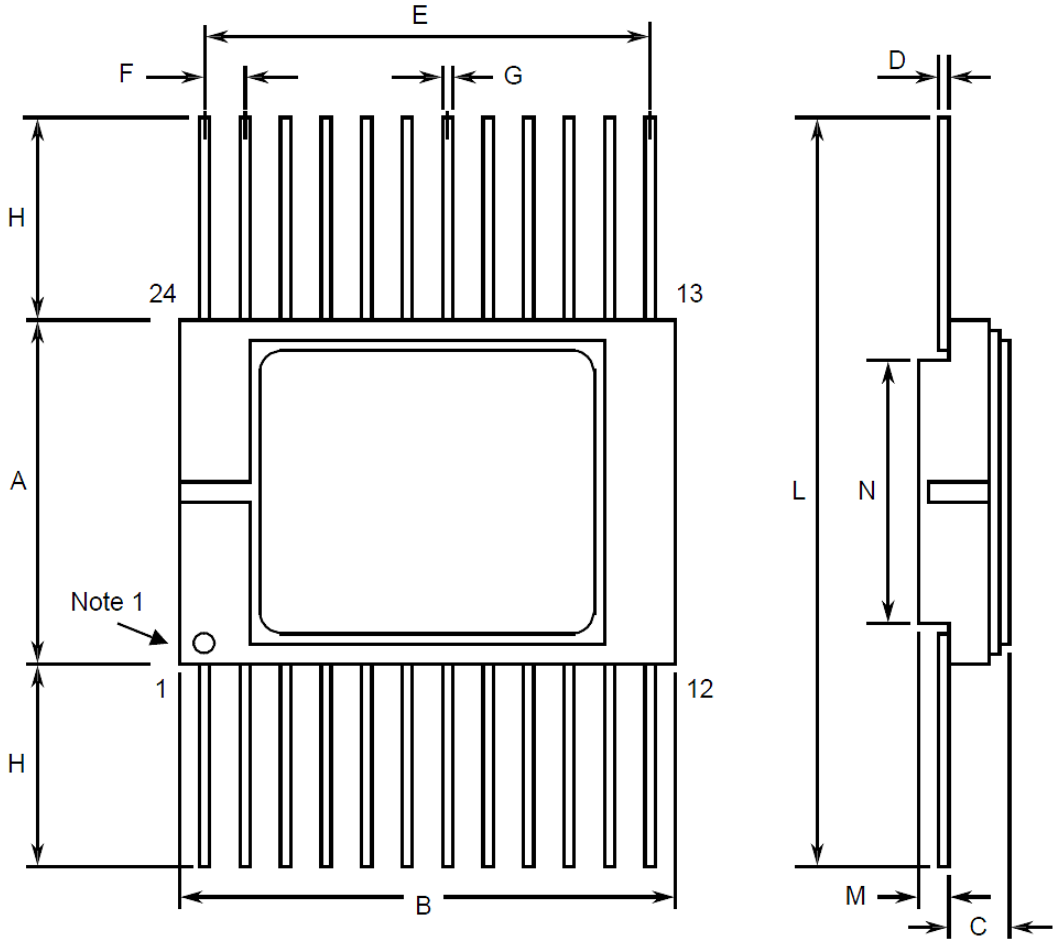
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

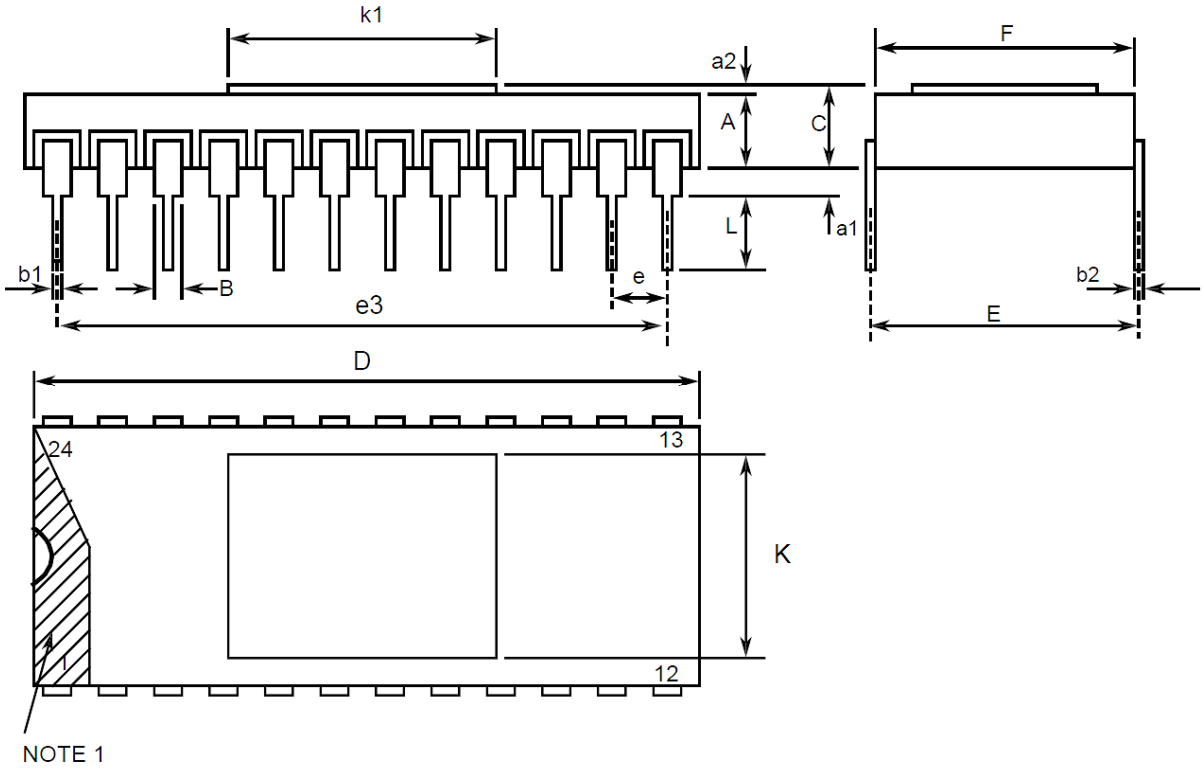
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 24 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	10.7	11.3	
B	15.3	15.7	
C	1.45	1.9	
D	0.23	0.3	5
E	13.84	14.1	
F	1.22	1.32	3, 6
G	0.45	0.55	5
H	7.25	8.25	5
L	25	28	
M	0.45	0.55	
N	7 TYPICAL		

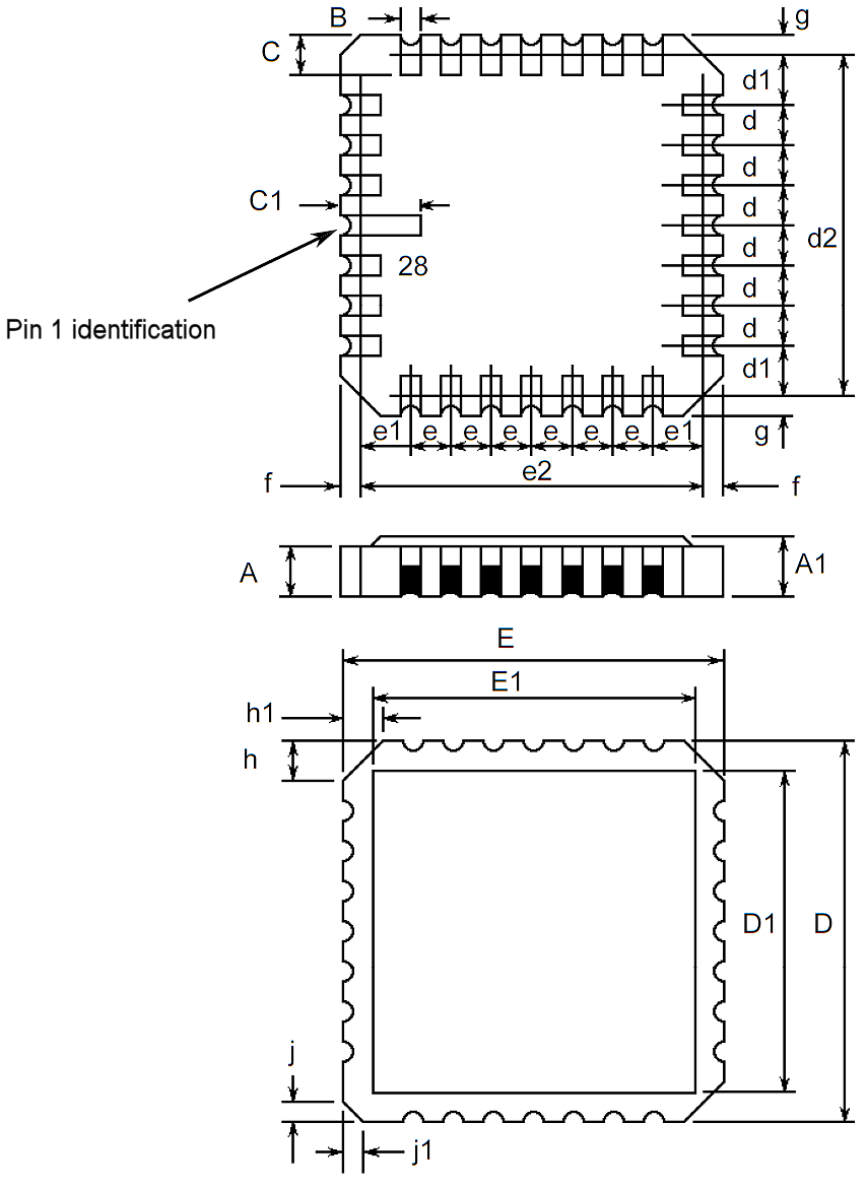
1.7.2 Dual-in-line Package (DIP) - 24 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.931	2.387	
a1	1.016	1.524	2
a2	0.274	0.34	
B	1.274 TYPICAL		5
b1	0.407	0.507	5
b2	0.229	0.304	5
C	2.205	2.727	
D	30.176	30.784	
E	14.986	15.494	
e	2.413	2.667	4
e3	27.813	28.067	
F	14.859	15.367	
L	3	3.8	
K	12.6	13	

Symbols	Dimensions mm		Notes
	Min	Max	
k1	12.6	13	

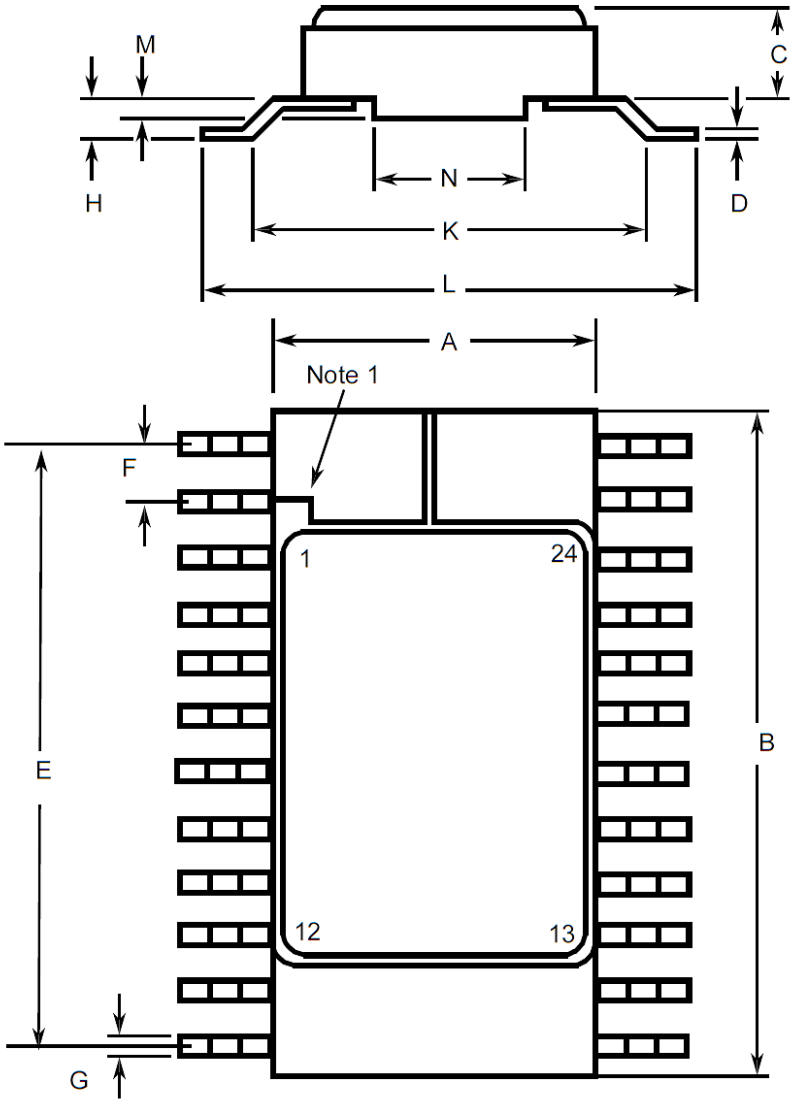
1.7.3 Chip Carrier Package (CCP) - 28 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5

Symbols	Dimensions mm		Notes
	Min	Max	
C	1.06	1.47	5
C1	1.91	2.41	
D	11.23	11.63	
D1	9.4	9.78	
d, d1	1.27 BSC		3
d2	10.16 BSC		
E	11.23	11.63	
E1	9.4	9.78	
e, e1	1.27 BSC		3
e2	10.16 BSC		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 24 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	7.3	7.6	
B	15.2	15.6	
C	1.58	1.88	
D	0.17	0.23	5
E	13.82	14.12	
F	1.27 BSC		3, 6
G	0.37	0.47	5
H	0.6	0.9	5

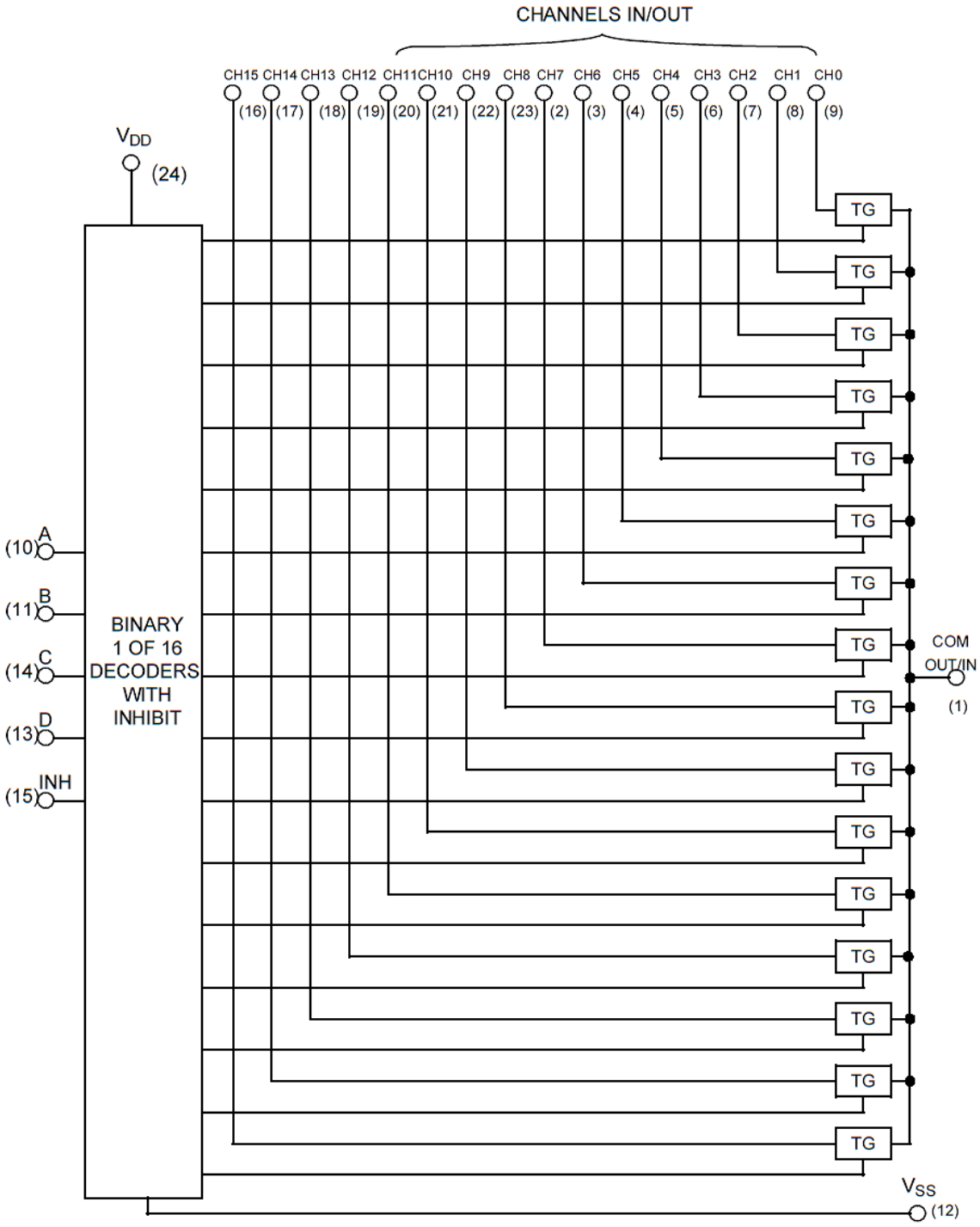
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.55 TYPICAL		
N	4.7 TYPICAL		

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 22 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	COM Output/Input (Common)	COM Output/Input (Common)	15	INH Input (Inhibit)	D Input (Select)
2	CH7 Input/Output (Channel)	CH7 Input/Output (Channel)	16	CH15 Input/Output (Channel)	C Input (Select)
3	CH6 Input/Output (Channel)	CH6 Input/Output (Channel)	17	CH14 Input/Output (Channel)	INH Input (Inhibit)
4	CH5 Input/Output (Channel)	-	18	CH13 Input/Output (Channel)	-
5	CH4 Input/Output (Channel)	CH5 Input/Output (Channel)	19	CH12 Input/Output (Channel)	CH15 Input/Output (Channel)
6	CH3 Input/Output (Channel)	CH4 Input/Output (Channel)	20	CH11 Input/Output (Channel)	CH14 Input/Output (Channel)
7	CH2 Input/Output (Channel)	CH3 Input/Output (Channel)	21	CH10 Input/Output (Channel)	CH13 Input/Output (Channel)
8	CH1 Input/Output (Channel)	CH2 Input/Output (Channel)	22	CH9 Input/Output (Channel)	CH12 Input/Output (Channel)
9	CH0 Input/Output (Channel)	CH1 Input/Output (Channel)	23	CH8 Input/Output (Channel)	CH11 Input/Output (Channel)
10	A Input (Select)	CH0 Input/Output (Channel)	24	V_{DD}	CH10 Input/Output (Channel)
11	B Input (Select)	-	25	-	-
12	V_{SS}	A Input (Select)	26	-	CH9 Input/Output (Channel)
13	D Input (Select)	B Input (Select)	27	-	CH8 Input/Output (Channel)
14	C Input (Select)	V_{SS}	28	-	V_{DD}

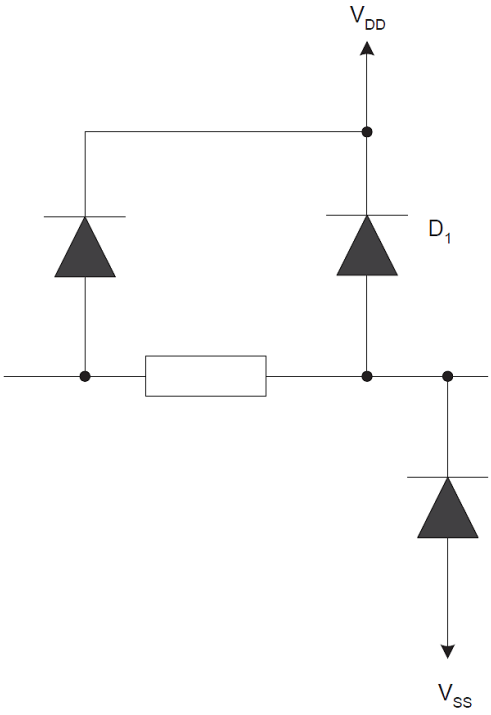
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.

CONTROL INPUTS					ON CHANNEL
INH	SELECT				
	D	C	B	A	
L	L	L	L	L	0 (CH0 to COM, COM to CH0)
L	L	L	L	H	1 (CH1 to COM, COM to CH1)
L	L	L	H	L	2 (CH2 to COM, COM to CH2)
L	L	L	H	H	3 (CH3 to COM, COM to CH3)
L	L	H	L	L	4 (CH4 to COM, COM to CH4)
L	L	H	L	H	5 (CH5 to COM, COM to CH5)
L	L	H	H	L	6 (CH6 to COM, COM to CH6)
L	L	H	H	H	7 (CH7 to COM, COM to CH7)
L	H	L	L	L	8 (CH8 to COM, COM to CH8)
L	H	L	L	H	9 (CH9 to COM, COM to CH9)
L	H	L	H	L	10 (CH10 to COM, COM to CH10)
L	H	L	H	H	11 (CH11 to COM, COM to CH11)
L	H	H	L	L	12 (CH12 to COM, COM to CH12)
L	H	H	L	H	13 (CH13 to COM, COM to CH13)
L	H	H	H	L	14 (CH14 to COM, COM to CH14)
L	H	H	H	H	15 (CH15 to COM, COM to CH15)
H	X	X	X	X	NONE (High Impedance)

1.11 INPUT PROTECTION NETWORK

CONTROL INPUTS



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3 ºC.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table V_{IL} = 0V, V_{IH} = 3V V_{DD} = 3V, V_{SS} = 0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 3	-	500	nA
Low Level Input Current, Control Inputs	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{DD} = 15V, V_{SS} = 0V	-	-50	nA
High Level Input Current, Control Inputs	I_{IH}	3010	V_{IN} (Under Test) = 15V V_{DD} = 15V, V_{SS} = 0V	-	50	nA
Channel OFF Leakage Current 1, Any Channel CHn	I_{OFF1}	-	Channel Under Test V_{IN} (CH) = 15V V_{IN} (COM) = 0V All other Channels Open V_{DD} = 15V, V_{SS} = 0V	-	-100	nA
Channel OFF Leakage Current 2, Any Channel CHn	I_{OFF2}	-	Channel Under Test V_{IN} (CH) = 0V V_{IN} (COM) = 15V All other Channels Open V_{DD} = 15V, V_{SS} = 0V	-	100	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Channel OFF Leakage Current 3, All Channels Tested Together	I_{OFF3}	-	V_{IN} (CH) = 0V V_{IN} (COM) = 15V V_{DD} = 15V, V_{SS} = 0V	-	100	nA
Channel OFF Leakage Current 4, All Channels Tested Together	I_{OFF4}	-	V_{IN} (CH) = 15V V_{IN} (COM) = 0V V_{DD} = 15V, V_{SS} = 0V	-	-100	nA
Channel ON Resistance 1	R_{ON1}	-	V_{IL} = 0V, V_{IH} = 5V R_L = 10kΩ V_{DD} = 5V, V_{SS} = 0V Note 4	-	1050	Ω
Channel ON Resistance 2	R_{ON2}	-	V_{IL} = 0V, V_{IH} = 15V R_L = 10kΩ V_{DD} = 15V, V_{SS} = 0V Note 4	-	240	Ω
Low Level Input Voltage 1 (Noise Immunity) (Functional Test)	V_{IL1}	-	Verify Truth Table V_{DD} = 5V, V_{SS} = 0V Note 5	-	1.5	V
Low Level Input Voltage 2 (Noise Immunity) (Functional Test)	V_{IL2}	-	Verify Truth Table V_{DD} = 15V, V_{SS} = 0V Note 5	-	4	V
High Level Input Voltage 1 (Noise Immunity) (Functional Test)	V_{IH1}	-	Verify Truth Table V_{DD} = 5V, V_{SS} = 0V Note 5	3.5	-	V
High Level Input Voltage 2 (Noise Immunity) (Functional Test)	V_{IH2}	-	Verify Truth Table V_{DD} = 15V, V_{SS} = 0V Note 5	11	-	V
Threshold Voltage N-Channel	V_{THN}	-	INH Input at Ground All Other Inputs: V_{IN} = 5V V_{DD} = 5V, I_{SS} = -10µA	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	-	INH Input at Ground All Other Inputs: V_{IN} = -5V V_{SS} = -5V, I_{DD} = 10µA	0.7	3	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input Clamp Voltage 1, to V_{SS}, Control Inputs	V_{IC1}	-	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open	-	-2	V
Input Clamp Voltage 2, to V_{DD}, Control Inputs	V_{IC2}	-	V_{IN} (Under Test) = 6V R = 30kΩ, V_{SS} = Open All Other Pins Open Note 6	3	-	V
Input Capacitance, Control Inputs	C_{IN}	3012	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V f = 100kHz to 1MHz Note 7	-	7.5	pF
Channel Capacitance, CHn	C_{CH}	3012	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V f = 100kHz to 1MHz Note 7	-	7.5	pF
Channel Capacitance, COM	C_{COM}	3012	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V f = 100kHz to 1MHz Note 7	-	120	pF
Propagation Delay Low to High, CH0 to COM	t_{PLH}	3003	V_{IN}(CH) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, R_L = 200kΩ V_{DD} = 5V, V_{SS} = 0V Note 8	-	60	ns
Propagation Delay High to Low, CH0 to COM	t_{PHL}	3003	V_{IN}(CH) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, R_L = 200kΩ V_{DD} = 5V, V_{SS} = 0V Note 8	-	60	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Enable Time High Impedance to High Output 1, A to COM	t_{PZH1}	3003	V_{IN}(A) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V V_{IN}(CH) = 5V and Open R_L = 10kΩ V_{DD} = 5V, V_{SS} = 0V Note 8	-	650	ns
Output Disable Time High Output to High Impedance 1, A to COM	t_{PHZ1}	3003	V_{IN}(A) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V V_{IN}(CH) = 5V and Open R_L = 300Ω V_{DD} = 5V, V_{SS} = 0V Note 8	-	440	ns
Output Enable Time High Impedance to High Output 2, INH to COM	t_{PZH2}	3003	V_{IN}(INH) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{IN}(CH) = 5V, R_L = 10kΩ V_{DD} = 5V, V_{SS} = 0V Note 8	-	650	ns
Output Disable Time High Output to High Impedance 2, INH to COM	t_{PHZ2}	3003	V_{IN}(INH) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{IN}(CH) = 5V, R_L = 300Ω V_{DD} = 5V, V_{SS} = 0V Note 8	-	440	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5) ºC and T_{amb} = -55 (+5 -0) ºC.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table V_{IL} = 0V, V_{IH} = 3V V_{DD} = 3V, V_{SS} = 0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 3 T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 15 0.5	µA
Low Level Input Current, Control Inputs	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 -100 -50	nA
High Level Input Current, Control Inputs	I_{IH}	3010	V_{IN} (Under Test) = 15V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 100 50	nA
Channel OFF Leakage Current 1, Any Channel CHn	I_{OFF1}	-	Channel Under Test V_{IN} (CH) = 15V V_{IN} (COM) = 0V All other Channels Open V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 -1 -0.1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Channel OFF Leakage Current 2, Any Channel CHn	I_{OFF2}	-	Channel Under Test V_{IN} (CH) = 0V V_{IN} (COM) = 15V All other Channels Open V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 1 0.1	µA
Channel OFF Leakage Current 3, All Channels Tested Together	I_{OFF3}	-	V_{IN} (CH) = 0V V_{IN} (COM) = 15V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 1 0.1	µA
Channel OFF Leakage Current 4, All Channel Tested Together	I_{OFF4}	-	V_{IN} (CH) = 15V V_{IN} (COM) = 0V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 -1 -0.1	µA
Channel ON Resistance 1	R_{ON1}	-	V_{IL} = 0V, V_{IH} = 5V R_L = 10kΩ V_{DD} = 5V, V_{SS} = 0V Note 4 T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 1300 800	Ω
Channel ON Resistance 2	R_{ON2}	-	V_{IL} = 0V, V_{IH} = 15V R_L = 10kΩ V_{DD} = 15V, V_{SS} = 0V Note 4 T_{amb} = +125 °C T_{amb} = -55 °C	 - -	 320 200	Ω
Low Level Input Voltage 1 (Noise Immunity) (Functional Test)	V_{IL1}	-	Verify Truth Table V_{DD} = 5V, V_{SS} = 0V Note 5	-	1.5	V
Low Level Input Voltage 2 (Noise Immunity) (Functional Test)	V_{IL2}	-	Verify Truth Table V_{DD} = 15V, V_{SS} = 0V Note 5	-	4	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Voltage 1 (Noise Immunity) (Functional Test)	V_{IH1}	-	Verify Truth Table V_{DD} = 5V, V_{SS} = 0V Note 5	3.5	-	V
High Level Input Voltage 2 (Noise Immunity) (Functional Test)	V_{IH2}	-	Verify Truth Table V_{DD} = 15V, V_{SS} = 0V Note 5	11	-	V
Threshold Voltage N-Channel	V_{THN}	-	INH Input at Ground All Other Inputs: V_{IN} = 5V V_{DD} = 5V, I_{SS} = -10µA T_{amb} = +125 °C T_{amb} = -55 °C	 -0.3 -0.7	 -3.5 -3.5	V
Threshold Voltage P-Channel	V_{THP}	-	INH Input at Ground All Other Inputs: V_{IN} = -5V V_{SS} = -5V, I_{DD} = 10µA T_{amb} = +125 °C T_{amb} = -55 °C	 0.3 0.7	 3.5 3.5	V

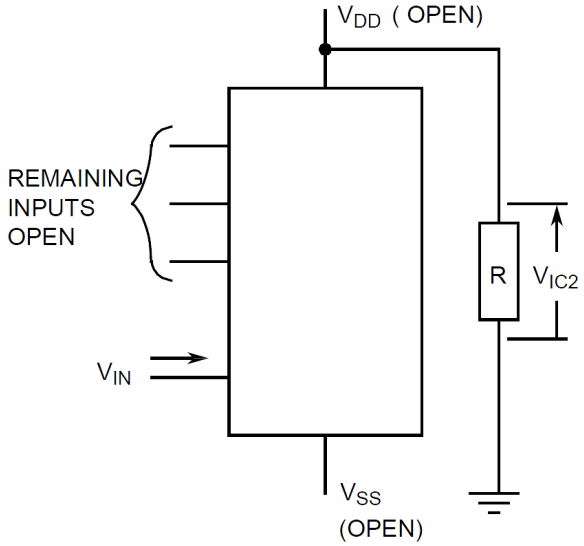
2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be V_{IN} = V_{SS} or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table. The maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions where 1 = V_{IH} and 0 = V_{IL}:

I_{DD} TEST	INPUT CONDITIONS																					
	INH	A	B	C	D	COM	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7	CH 8	CH 9	CH 10	CH 11	CH 12	CH 13	CH 14	CH 15
(a)	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(b)	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(c)	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
(d)	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(e)	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
(f)	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
(g)	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
(h)	0	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

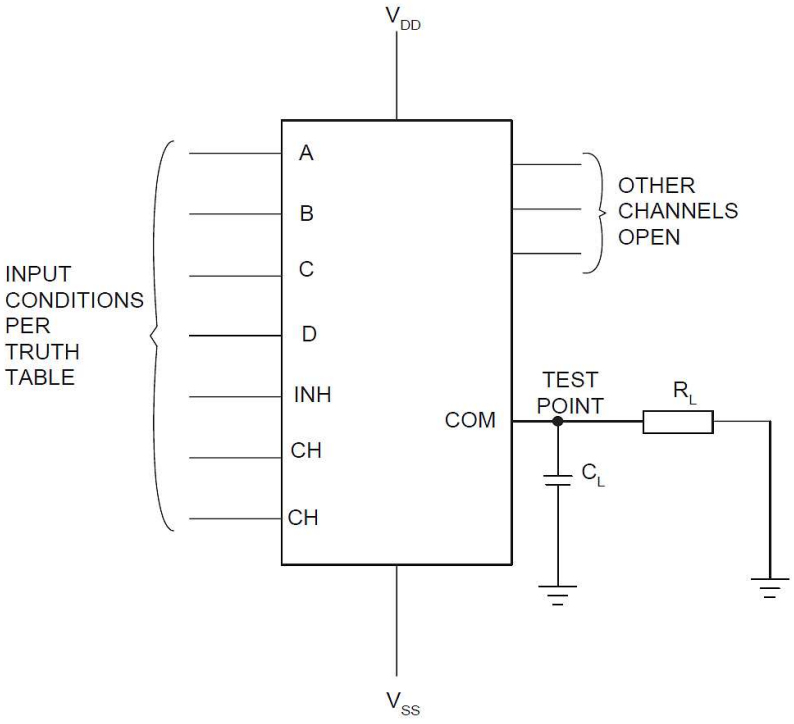
I_{DD} TEST	INPUT CONDITIONS																					
	INH	A	B	C	D	COM	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7	CH 8	CH 9	CH 10	CH 11	CH 12	CH 13	CH 14	CH 15
(i)	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
(j)	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
(k)	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
(l)	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
(m)	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
(n)	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
(o)	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
(p)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
(q)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

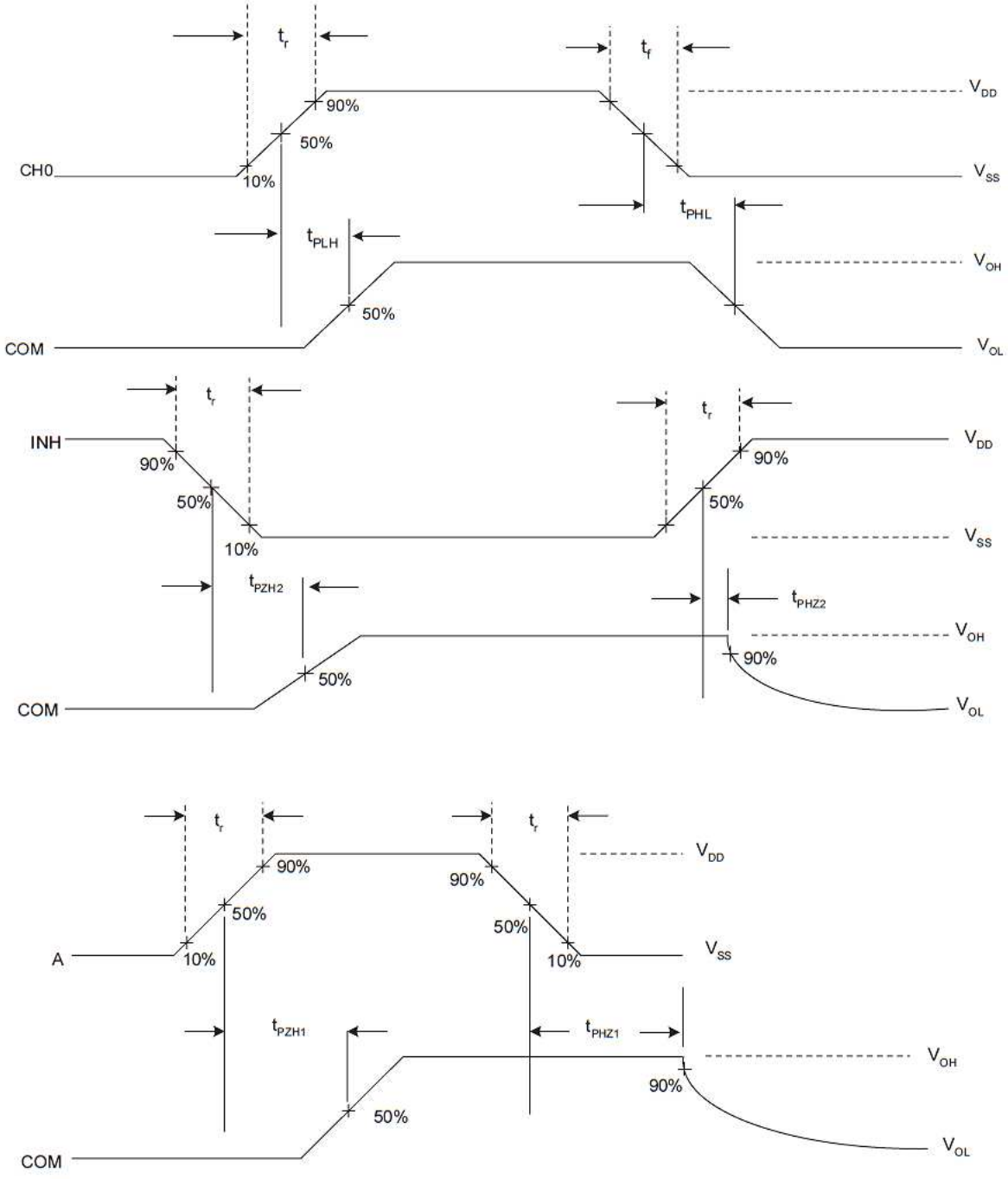
4. Channel ON Resistance shall be tested for each channel in both directions using the following input conditions:
   (a) INH = V_{IL}
   (b) A, B, C, D = V_{IL} or V_{IH} per Truth Table to select channel under test
   (c) I_{IN} (CHn or COM) = 100µA
   (d) R_{ON1} shall be tested with V_{IN} (CHn or COM) = 1.5V, 1.9V, 2.3V, 2.7V, 3.3V, 3.7V, 4.1V
   R_{ON2} shall be tested with V_{IN} (CHn or COM) = 1.5V, 1.9V, 2.3V, 2.7V, 13.3V, 13.7V, 14.1V, 14.5V
   Channel ON Resistance shall be recorded for Channel 4 (CH4 to COM, COM to CH4) at each specified V_{IN}. Other channels may be tested go-no-go.
5. Performed as a functional test to verify for all OFF channels I_{OFF} < 2µA with V_{IN}(CH) = V_{DD} through 1kΩ, COM output load resistance R_L = 1kΩ ±5%.
6. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:



7. Guaranteed but not tested.

8. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
The pulse generator shall have the following characteristics:
V_{GEN} = 0 to V_{DD}; f_{GEN} = 500kHz; t_r and t_f ≤ 15ns (10% to 90%); duty cycle = 50%; Z_{out} = 50Ω.
Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture, and output load resistance R_L = 1kΩ ±5%. Channel bias resistance R_L = as specified.
Propagation delay times shall be measured as follows:





2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	±75	-	500	nA
Channel ON Resistance 1, CH4 to COM, COM to CH4 Note 2	R_{ON1}	±50	-	1050	Ω
Channel ON Resistance 2, CH4 to COM, COM to CH4 Note 2	R_{ON2}	±15	-	240	Ω
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Channel ON Resistance shall be tested at each input voltage level specified in Room Temperature Electrical Measurements in both directions for CH4 to COM only.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	I_{DD}	±75	-	500	nA
Low Level Input Current, Control Inputs	I_{IL}	-	-	-50	nA
High Level Input Current, Control Inputs	I_{IH}	-	-	50	nA

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Channel OFF Leakage Current 1, Any Channel CHn	I_{OFF1}	-	-	-100	nA
Channel OFF Leakage Current 3, All Channels Tested Together	I_{OFF3}	-	-	100	nA
Channel ON Resistance 1	R_{ON1}	±50	-	1050	Ω
Channel ON Resistance 2	R_{ON2}	±15	-	240	Ω
Low Level Input Voltage 1, (Noise Immunity) (Functional Test)	V_{IL1}	–	-	1.5	V
High Level Input Voltage 1, (Noise Immunity) (Functional Test)	V_{IH1}	–	3.5	-	V
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Output COM	V_{OUT}	V_{SS}	V
Inputs CHn	V_{IN}	V_{DD}	V
Inputs INH, A, B, C, D	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Output COM	V_{OUT}	V_{SS}	V
Inputs CHn	V_{IN}	V_{SS}	V
Inputs INH, A, B, C, D	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Output COM	V_{OUT}	V_{SS}	V
Inputs CHn	V_{IN}	V_{DD}	V
Input A	V_{IN}	V_{GEN1}	V
Input B	V_{IN}	V_{GEN2}	V
Input C	V_{IN}	V_{GEN3}	V
Input D	V_{IN}	V_{GEN4}	V
Input INH	V_{IN}	V_{GEN5}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1} f_{GEN2} f_{GEN3} f_{GEN4} f_{GEN5}	500k 250k 125k 62.5k 31.25k 50% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255. Solderability is not applicable unless specifically stipulated in the Purchase Order.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.