# INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS ANALOGUE MULTIPLEXER/DEMULTIPLEXER (SINGLE 8-CHANNEL)

## BASED ON TYPE 4051B

## ESCC Detail Specification No. 9202/047



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|---|---|

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## DOCUMENTATION CHANGE NOTICE

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| DCR No. | CHANGE DESCRIPTION |
| --- | --- |
| 1185, 1200, 1258 | Specification upissued to incorporate changes per DCR. |

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# 1 GENERAL

## 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

## 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

## 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

## 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920204701

- Detail Specification Reference: 9202047
- Component Type Variant Number: 01 (as required)

### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and Finish | Weight max g |
|---|---|---|---|---|
| 01 | 4051B | FP | G2 | 0.7 |
| 02 | 4051B | FP | G4 | 0.7 |
| 08 | 4051B | DIP | G2 | 2.2 |
| 09 | 4051B | DIP | G4 | 2.2 |
| 12 | 4051B | Die | N/A | N/A |

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

## 1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

| Characteristics | Symbols | Maximum Ratings | Units | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to 18 | V | Note 1 |
| Supply Voltage Range | $V_{DD}$-$V_{EE}$ | -0.5 to 18 | V | Note 2 |
| Control Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 | V | Note 1<br>Power on |
| Channel Input/Output Voltage | $V_{IN}$ | $V_{EE}$-0.5 to $V_{DD}$+0.5 | V | Note 1, 3 |
| Control Input Current | $I_{IN}$ | ±10 | mA | - |
| Device Power Dissipation (Continuous) | $P_D$ | 200 | mW | - |
| Power Dissipation per Single Output | $P_{DSO}$ | 100 | mW | - |
| Operating Temperature Range | $T_{op}$ | -55 to +125 | °C | $T_{amb}$ |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C | - |
| Soldering Temperature | $T_{sol}$ | +265 | °C | Note 4 |

**NOTES:**

1. Device is functional for $3V \le V_{DD} \le 15V$ with reference to $V_{SS}$.
2. Device is functional for $3V \le V_{DD}-V_{EE} \le 15V$.
3. To avoid draining $V_{DD}$ supply current into the ON Channel when current flows from CHn to COM the voltage drop across the ON Channel shall not exceed 0.4V.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

## 1.6 HANDLING PRECAUTIONS

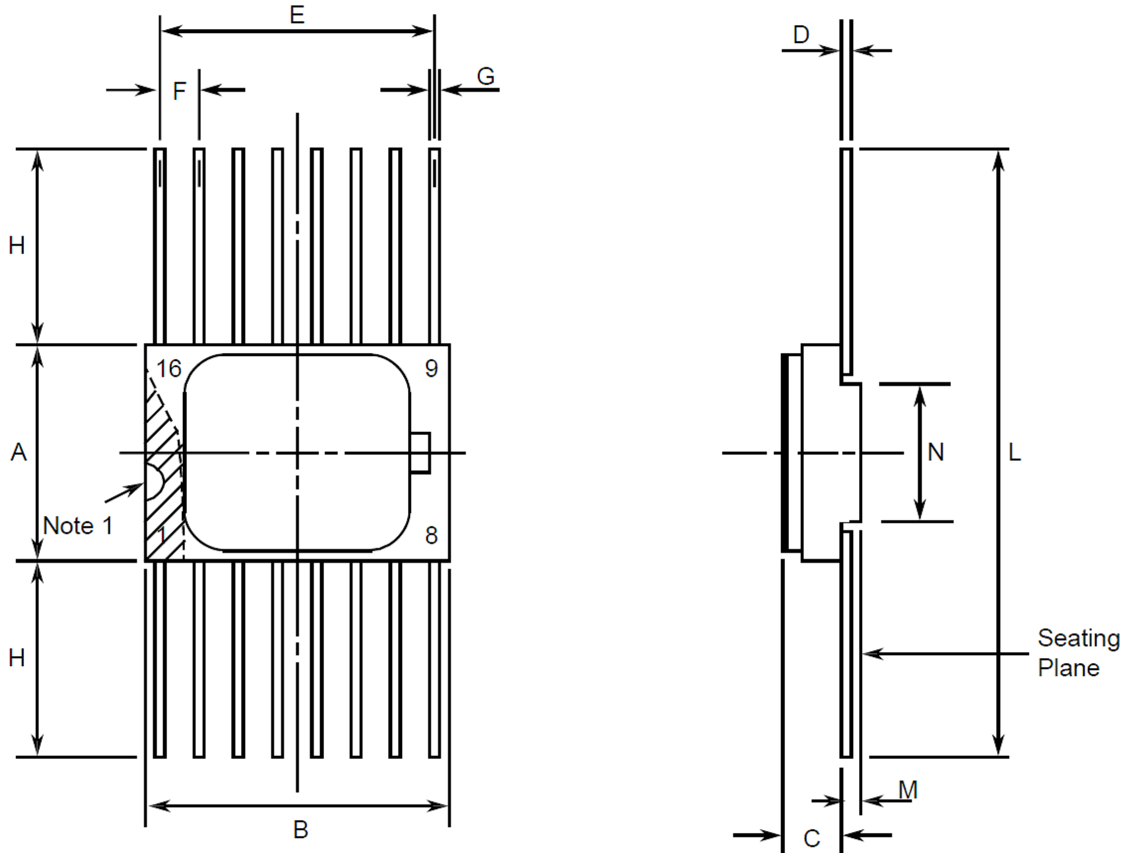
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

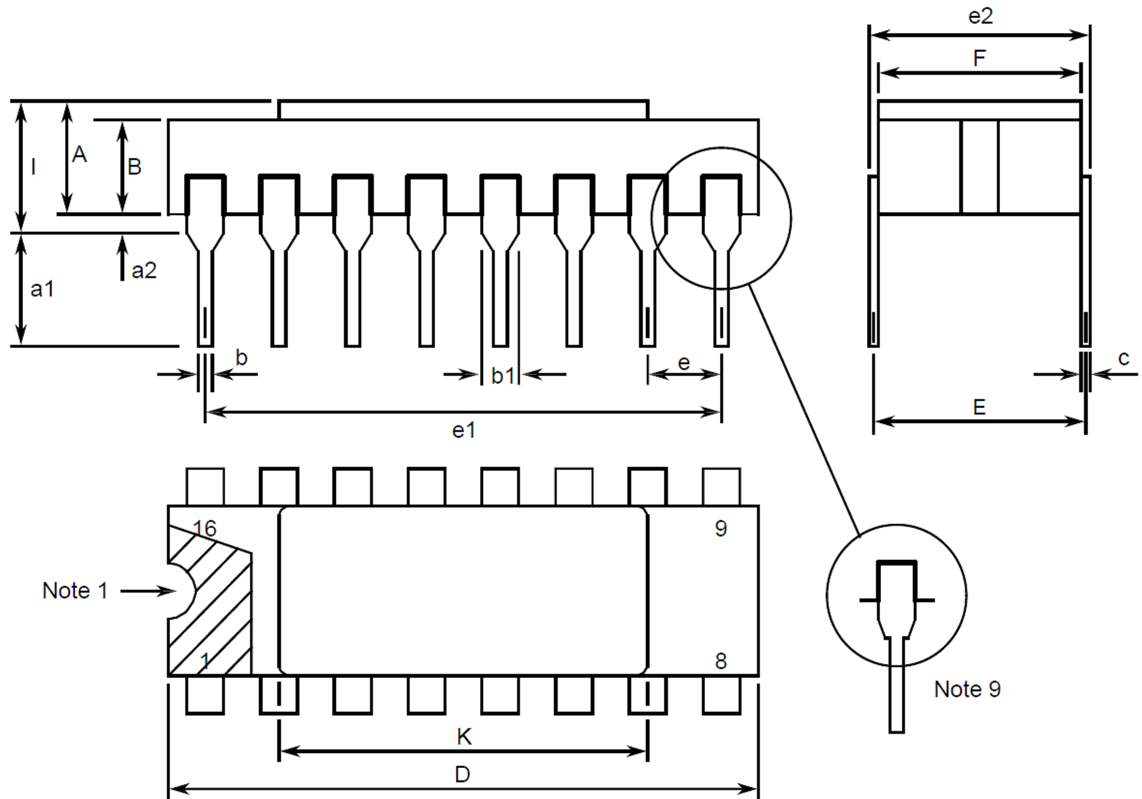
Consolidated Notes for Packaged Components are given in Para. 1.7.3.

1.7.1 Flat Package (FP) - 16 Pin (Variants 01, 02)




| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 6.75 | 7.06 | |
| B | 9.76 | 10.14 | |
| C | 1.49 | 1.95 | |
| D | 0.1 | 0.15 | 5 |
| E | 8.76 | 9.01 | |
| F | 1.27 BSC | | 3, 6 |
| G | 0.38 | 0.48 | 5 |
| H | 6 | - | 5 |
| L | 18.75 | 22 | |
| M | 0.33 | 0.43 | |
| N | 4.32 TYPICAL | | |

1.7.2 Dual-in-line Package (DIP) - 16 Pin (Variants 08, 09)



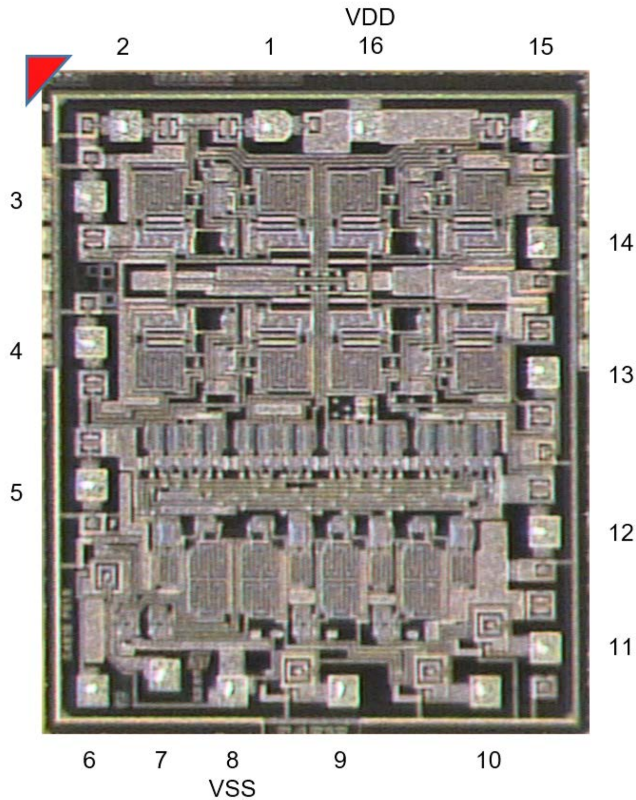

| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 2.1 | 2.71 | |
| a1 | 3 | 3.7 | |
| a2 | 0.63 | 1.14 | 2 |
| B | 1.82 | 2.39 | |
| b | 0.4 | 0.5 | 5 |
| b1 | 1.14 | 1.5 | 5 |
| c | 0.2 | 0.3 | 5 |
| D | 20.06 | 20.58 | |
| E | 7.36 | 7.87 | |
| e | 2.54 BSC | | 4, 6 |
| e1 | 17.65 | 17.9 | |
| e2 | 7.62 | 8.12 | |
| F | 7.29 | 7.7 | |
| I | - | 3.83 | |

| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| K | 10.9 | 12.1 | |

1.7.3 Notes to Physical Dimensions and Terminal Identification for Packaged Components

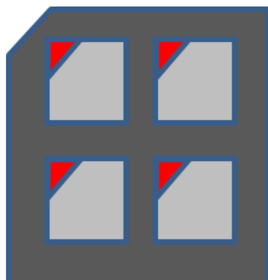
1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces.
9. For all pins, either pin shape may be supplied.

1.7.4 Die (Variant 12)



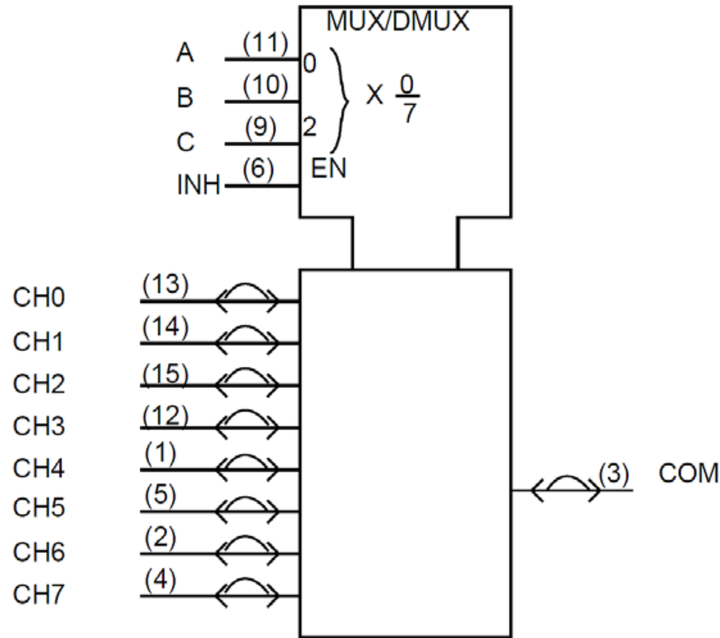

**NOTES:**

1. Die materials and dimensions:
   - Die substrate: Silicon
   - Die length and width: 1.8mm × 2.16mm
   - Die thickness: 525 ±25µm
   - Passivation: P. Vapox: 800nm ±160nm
   - Top metallisation: Al (99%)/Si (1%) with thickness: 1.1 ±0.1µm
   - Backside metallisation: N/A (i.e. bare silicon)
   - Bond pad dimensions: 90µm × 90µm (typ.)
2. Terminal identification and die orientation are indicated by the die mask (including the die reference, i.e. C4515 P51B –800A) and pad numbers as shown; see Para. 1.9.
3. Bias details: backside contact = $V_{DD}$
4. Die packaging orientation: The die corner highlighted with the red triangle is positioned in the waffle pack as follows:



1.8 FUNCTIONAL DIAGRAM

Pin/Pad numbers relate to FP, DIP packages and Die.




**NOTES:**

1. The package lid for all packages is not connected to any terminal.

1.9 PIN/PAD ASSIGNMENT

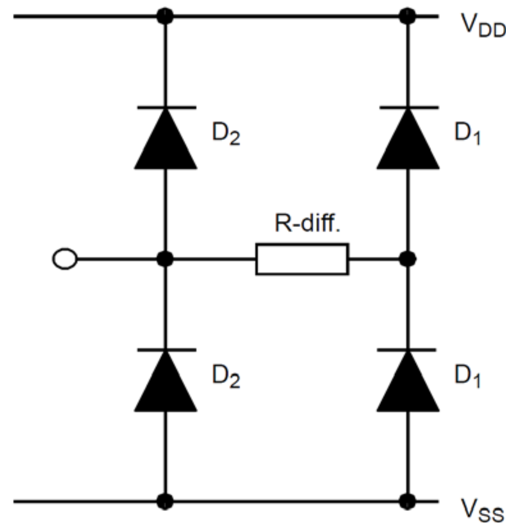
| Pin/Pad | Function | Pin/Pad | Function |
|---|---|---|---|
| 1 | CH4 Input/Output (Channel) | 9 | C Input (Select) |
| 2 | CH6 Input/Output (Channel) | 10 | B Input (Select) |
| 3 | COM Output/Input (Common) | 11 | A Input (Select) |
| 4 | CH7 Input/Output (Channel) | 12 | CH3 Input/Output (Channel) |
| 5 | CH5 Input/Output (Channel) | 13 | CH0 Input/Output (Channel) |
| 6 | INH Input (Inhibit) | 14 | CH1 Input/Output (Channel) |
| 7 | $V_{EE}$ (Analogue Negative Supply) | 15 | CH2 Input/Output (Channel) |
| 8 | $V_{SS}$ (Digital Negative Supply) | 16 | $V_{DD}$ |

1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.

| CONTROL INPUTS | | | | ON CHANNEL |
|---|---|---|---|---|
| INH | SELECT | | | |
| | C | B | A | |
| L | L | L | L | 0 (CH0 to COM, COM to CH0) |
| L | L | L | H | 1 (CH1 to COM, COM to CH1) |
| L | L | H | L | 2 (CH2 to COM, COM to CH2) |
| L | L | H | H | 3 (CH3 to COM, COM to CH3) |
| L | H | L | L | 4 (CH4 to COM, COM to CH4) |
| L | H | L | H | 5 (CH5 to COM, COM to CH5) |
| L | H | H | L | 6 (CH6 to COM, COM to CH6) |
| L | H | H | H | 7 (CH7 to COM, COM to CH7) |
| H | X | X | X | NONE (High Impedance) |

1.11 INPUT PROTECTION NETWORK
(CONTROL INPUTS)




## 2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

## 2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component or its primary package shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number (see Para 1.4.1).
(d) Traceability information.

## 2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given in Para. 2.3.3.

### 2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb}$ = +22 ±3°C.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table<br>$V_{IL}$ = 0V, $V_{IH}$ = 3V<br>$V_{DD}$ = 3V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table<br>$V_{IL}$ = 0V, $V_{IH}$ = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 2 | - | - | - |
| Quiescent Current | $I_{DD}$ | 3005 | $V_{IL}$ = 0V, $V_{IH}$ = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 3 | - | 500 | nA |
| Low Level Input Current, Control Inputs | $I_{IL}$ | 3009 | $V_{IN}$ (Under Test) = 0V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | -50 | nA |
| High Level Input Current, Control Inputs | $I_{IH}$ | 3010 | $V_{IN}$ (Under Test) = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | 50 | nA |
| Channel OFF Leakage Current 1, Any Channel CHn | $I_{OFF1}$ | - | Channel Under Test<br>$V_{IN}$ (CH) = 15V<br>$V_{IN}$ (COM) = 0V<br>All other Channels Open<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | -100 | nA |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Channel OFF Leakage Current 2, Any Channel CHn | $I_{OFF2}$ | - | Channel Under Test<br>$V_{IN}$ (CH) = 0V<br>$V_{IN}$ (COM) = 15V<br>All other Channels Open<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | 100 | nA |
| Channel OFF Leakage Current 3, All Channels Tested Together | $I_{OFF3}$ | - | $V_{IN}$ (CH) = 0V<br>$V_{IN}$ (COM) = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | 100 | nA |
| Channel OFF Leakage Current 4, All Channels Tested Together | $I_{OFF4}$ | - | $V_{IN}$ (CH) = 15V<br>$V_{IN}$ (COM) = 0V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V | - | -100 | nA |
| Channel ON Resistance 1 | $R_{ON1}$ | - | $V_{IL}$ = 0V, $V_{IH}$ = 5V<br>$R_L$ = 10kΩ $V_{DD}$ = 5V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 4 | - | 1050 | Ω |
| Channel ON Resistance 2 | $R_{ON2}$ | - | $V_{IL}$ = 0V, $V_{IH}$ = 15V<br>$R_L$ = 10kΩ<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 4 | - | 280 | Ω |
| Low Level Input Voltage 1 (Noise Immunity) (Functional Test) | $V_{IL1}$ | - | Verify Truth Table<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | - | 1.5 | V |
| Low Level Input Voltage 2 (Noise Immunity) (Functional Test) | $V_{IL2}$ | - | Verify Truth Table<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | - | 4 | V |
| High Level Input Voltage 1 (Noise Immunity) Functional Test | $V_{IH1}$ | - | Verify Truth Table<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | 3.5 | - | V |
| High Level Input Voltage 2 (Noise Immunity) Functional Test | $V_{IH2}$ | - | Verify Truth Table<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | 11 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | - | INH Input and $V_{EE}$ at Ground<br>All Other Inputs:<br>$V_{IN}$ = 5V<br>$V_{DD}$ = 5V, $I_{SS}$ = -10µA | -0.7 | -3 | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Threshold Voltage P-Channel | $V_{THP}$ | - | INH Input at Ground<br>All Other Inputs:<br>$V_{IN}$ = -5V<br>$V_{SS}$ = $V_{EE}$ = -5V,<br>$I_{DD}$ = 3.5μA | 0.7 | 3 | V |
| Input Clamp Voltage 1, to $V_{SS}$ Control Inputs | $V_{IC1}$ | - | $I_{IN}$ (Under Test) = -100μA<br>$V_{DD}$ = Open, $V_{SS}$ = 0V<br>All Other Pins Open | - | -2 | V |
| Input Clamp Voltage 2, to $V_{DD}$ Control Inputs | $V_{IC2}$ | - | $V_{IN}$ (Under Test) = 6V<br>R = 30kΩ, $V_{SS}$ = Open<br>All Other Pins Open<br>Note 6 | 3 | - | V |
| Input Capacitance, Control Inputs | $C_{IN}$ | 3012 | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD}$ = $V_{SS}$ = $V_{EE}$ = 0V<br>f = 100 kHz to 1 MHz<br>Note 7 | - | 7.5 | pF |
| Channel Capacitance, CHn | $C_{CH}$ | 3012 | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD}$ = $V_{SS}$ = $V_{EE}$ = 0V<br>f = 100 kHz to 1 MHz<br>Note 7 | - | 7.5 | pF |
| Channel Capacitance, COM | $C_{COM}$ | 3012 | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD}$ = $V_{SS}$ = $V_{EE}$ = 0V<br>f = 100 kHz to 1 MHz<br>Note 7 | - | 7.5 | pF |
| Propagation Delay Low to High, COM to CH0 | $t_{PLH}$ | 3003 | $V_{IN}$(COM) = Pulse Generator<br>$V_{IN}$ (Remaining Inputs) = Truth Table<br>$V_{IL}$ = 0V, $V_{IH}$ = 5V,<br>$R_L$ = 200kΩ,<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 8 | - | 40 | ns |
| Propagation Delay High to Low, COM to CH0 | $t_{PHL}$ | 3003 | $V_{IN}$(COM) = Pulse Generator<br>$V_{IN}$ (Remaining Inputs) = Truth Table<br>$V_{IL}$ = 0V, $V_{IH}$ = 5V,<br>$R_L$ = 200kΩ,<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 8 | - | 40 | ns |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output Enable Time High Impedance to High Output 1, A to COM | $t_{PZH1}$ | 3003 | $V_{IN}(A)$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 5V, $V_{IN}(CH)$ = 5V and Open $R_L$ = 10kΩ $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V Note 8 | - | 670 | ns |
| Output Disable Time High Output to High Impedance 1, A to COM | $t_{PHZ1}$ | 3003 | $V_{IN}(A)$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 5V, $V_{IN}(CH)$ = 5V and Open $R_L$ = 300Ω $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V Note 8 | - | 670 | ns |
| Output Enable Time High Impedance to High Output 2, INH to COM | $t_{PZH2}$ | 3003 | $V_{IN}(INH)$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 5V, $V_{IN}(CH)$ = 5V, $R_L$ = 10kΩ $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V Note 8 | - | 400 | ns |
| Output Disable Time High Output to High Impedance 2, INH to COM | $t_{PHZ2}$ | 3003 | $V_{IN}(INH)$ = Pulse Generator $V_{IN}$ (Remaining Inputs) = Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 5V, $V_{IN}(CH)$ = 5V, $R_L$ = 300Ω $V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V Note 8 | - | 400 | ns |

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{amb}$ = +125 (+0 -5)°C and $T_{amb}$ = -55 (+5 -0)°C.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 3V $V_{DD}$ = 3V, $V_{SS}$ = $V_{EE}$ = 0V Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table $V_{IL}$ = 0V, $V_{IH}$ = 15V $V_{DD}$ = 15V, $V_{SS}$= $V_{EE}$ = 0V Note 2 | - | - | - |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Quiescent Current | $I_{DD}$ | 3005 | $V_{IL}$ = 0V, $V_{IH}$ = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 3<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br>-<br>- | <br><br><br><br>15<br>0.5 | µA |
| Low Level Input Current, Control Inputs | $I_{IL}$ | 3009 | $V_{IN}$ (Under Test) = 0V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br>-<br>- | <br><br><br>-100<br>-50 | nA |
| High Level Input Current, Control Inputs | $I_{IH}$ | 3010 | $V_{IN}$ (Under Test) = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br>-<br>- | <br><br><br>100<br>50 | nA |
| Channel OFF Leakage Current 1, Any Channel CHn | $I_{OFF1}$ | - | Channel Under Test<br>$V_{IN}$ (CH) = 15V<br>$V_{IN}$ (COM) = 0V<br>All other Channels Open<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br><br><br>-<br>- | <br><br><br><br><br><br>-1<br>-0.1 | µA |
| Channel OFF Leakage Current 2, Any Channel CHn | $I_{OFF2}$ | - | Channel Under Test<br>$V_{IN}$ (CH) = 0V<br>$V_{IN}$ (COM) = 15V<br>All other Channels Open<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br><br><br>-<br>- | <br><br><br><br><br><br>1<br>0.1 | µA |
| Channel OFF Leakage Current 3, All Channels Tested Together | $I_{OFF3}$ | - | $V_{IN}$ (CH) = 0V<br>$V_{IN}$ (COM) = 15V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br>-<br>- | <br><br><br><br>1<br>0.1 | µA |
| Channel OFF Leakage Current 4, All Channels Tested Together | $I_{OFF4}$ | - | $V_{IN}$ (CH) = 15V<br>$V_{IN}$ (COM) = 0V<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br>-<br>- | <br><br><br><br>-1<br>-0.1 | µA |
| Channel ON Resistance 1 | $R_{ON1}$ | - | $V_{IL}$ = 0V, $V_{IH}$ = 5V<br>$R_L$ = 10kΩ<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 4<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | <br><br><br><br>-<br>- | <br><br><br><br>1200<br>880 | Ω |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Channel ON Resistance 2 | $R_{ON2}$ | - | $V_{IL}$ = 0V, $V_{IH}$ = 15V<br>$R_L$ = 10kΩ<br>$V_{DD}$=15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 4<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | -<br>- | 400<br>220 | Ω |
| Low Level Input Voltage 1 (Noise Immunity) (Functional Test) | $V_{IL1}$ | - | Verify Truth Table<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | - | 1.5 | V |
| Low Level Input Voltage 2 (Noise Immunity) (Functional Test) | $V_{IL2}$ | - | Verify Truth Table<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | - | 4 | V |
| High Level Input Voltage 1 (Noise Immunity) (Functional Test) | $V_{IH1}$ | - | Verify Truth Table<br>$V_{DD}$ = 5V, $V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | 3.5 | - | V |
| High Level Input Voltage 2 (Noise Immunity) (Functional Test) | $V_{IH2}$ | - | Verify Truth Table<br>$V_{DD}$ = 15V,<br>$V_{SS}$ = $V_{EE}$ = 0V<br>Note 5 | 11 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | - | INH Input and $V_{EE}$ at Ground<br>All Other Inputs:<br>$V_{IN}$ = 5V<br>$V_{DD}$ = 5V, $I_{SS}$ = -10μA<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | -0.3<br>-0.7 | -3.5<br>-3.5 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | - | INH Input and $V_{EE}$ at Ground<br>All Other Inputs:<br>$V_{IN}$ = -5V<br>$V_{SS}$ = $V_{EE}$ = -5V,<br>$I_{DD}$ = 3.5μA<br>$T_{amb}$ = +125°C<br>$T_{amb}$ = -55°C | 0.3<br>0.7 | 3.5<br>3.5 | V |

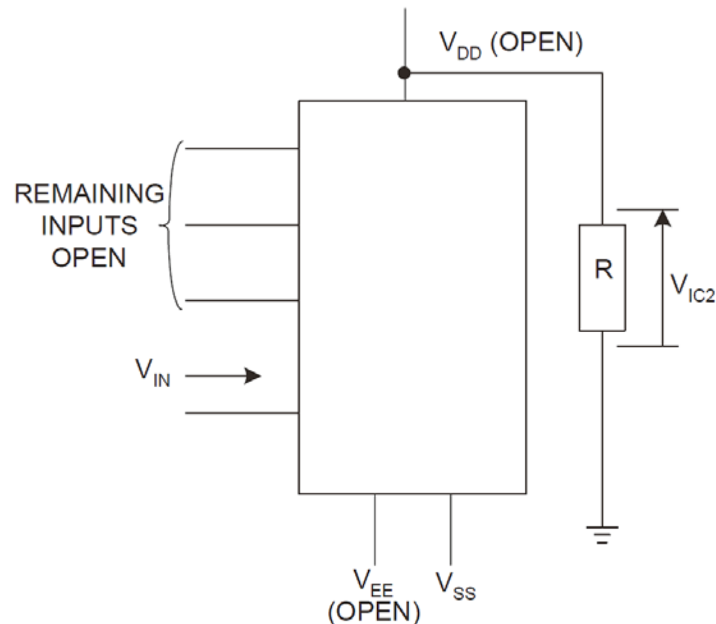
2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN}$ = $V_{SS}$ or $V_{DD}$ and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table. The maximum time to output comparator strobe = 300μs.

3. Quiescent Current shall be tested using the following input conditions where 1 = $V_{IH}$ and 0 = $V_{IL}$:

| $I_{DD}$ Test | Input Conditions | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | INH | A | B | C | COM | CH0 | CH1 | CH3 | CH4 | CH5 | CH6 | CH7 |
| (a) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (b) | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (c) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (d) | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (e) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (f) | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (g) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (h) | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (i) | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

4. Channel ON Resistance shall be tested for each channel in both directions using the following input conditions:
   (a) INH = $V_{IL}$
   (b) A, B, C = $V_{IL}$ or $V_{IH}$ per Truth Table to select channel under test
   (c) $I_{IN}$ (CHn or COM) = 100µA
   (d) $R_{ON1}$ shall be tested with $V_{IN}$ (CHn or COM) = 1.5V, 1.9V, 2.3V, 2.7V, 3.3V, 3.7V, 4.1V
   $R_{ON2}$ shall be tested with $V_{IN}$ (CHn or COM) = 1.5V, 1.9V, 2.3V, 2.7V, 13.3V, 13.7V, 14.1V, 14.5V
   Channel ON Resistance shall be recorded for Channel 4 (CH4 to COM, COM to CH4) at each specified $V_{IN}$. Other channels may be tested go-no-go.
5. Performed as a functional test to verify for all OFF channels $I_{OFF}$ < 2µA with $V_{IN}$ (CH) = $V_{DD}$ through 1kΩ, COM output load resistance $R_L$ = 1kΩ ±5%.
6. Input Clamp Voltage 2 to $V_{DD}$, $V_{IC2}$, shall be tested on each input as follows:




7. Guaranteed but not tested.

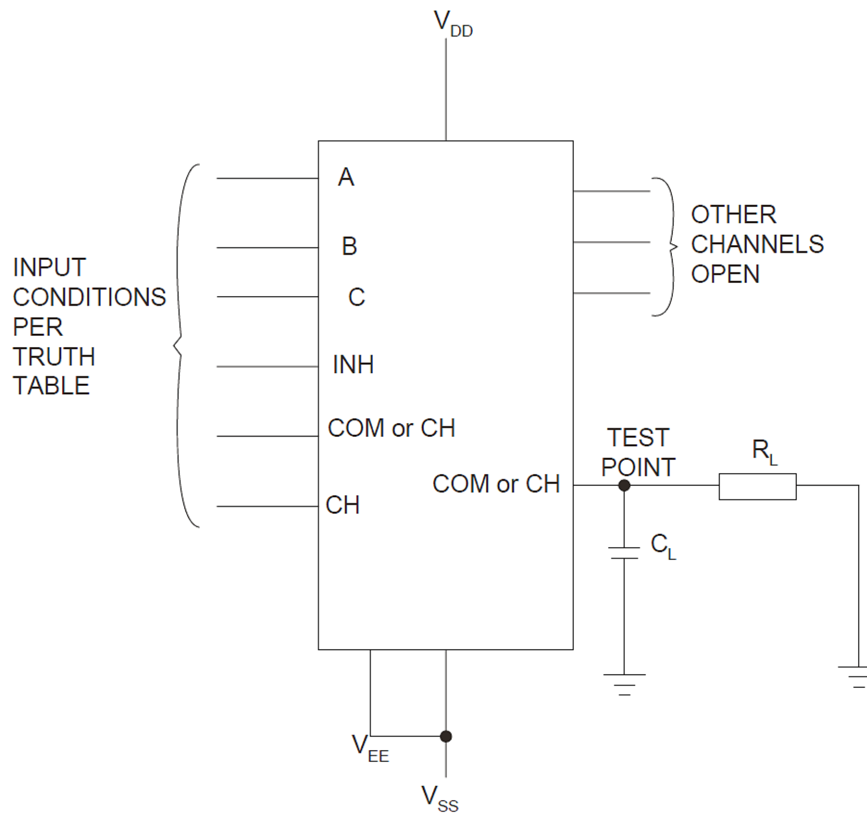
8. For Packaged Components (Variants 01, 02, 08, 09), read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.

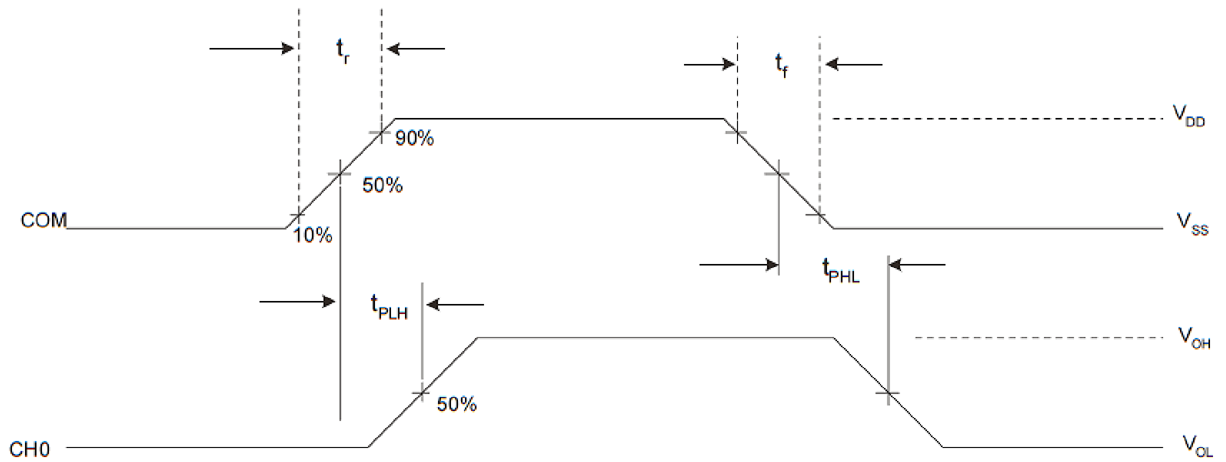
For Die Components (Variant 12), read and record measurements shall be performed on a sample of 32 components or 100% of the Packaged Test Sublot, whichever is less, with 0 failures permitted.

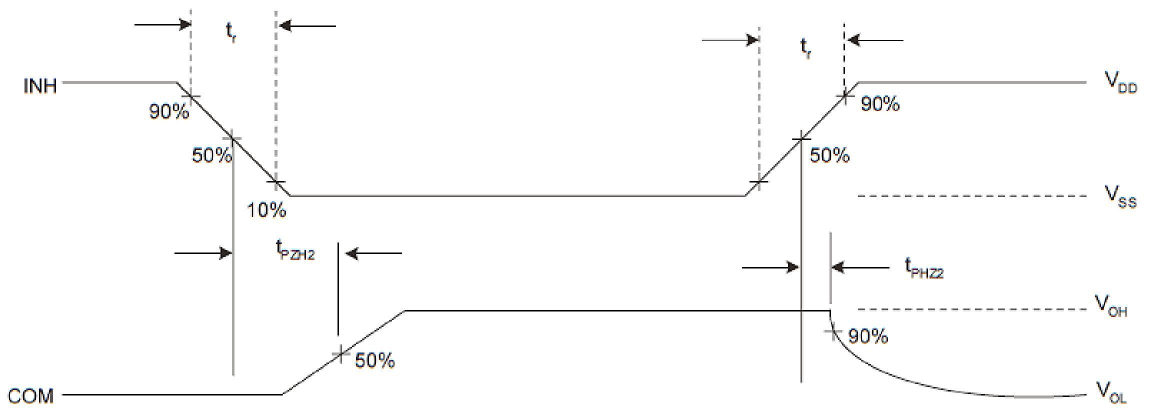
The pulse generator shall have the following characteristics:

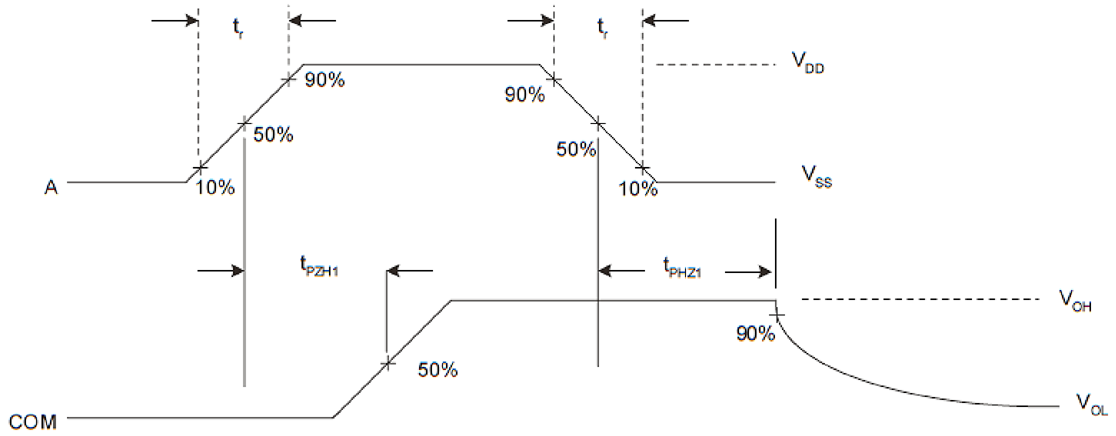
$V_{GEN}$ = 0 to $V_{DD}$; $f_{GEN}$ = 500kHz; $t_r$ and $t_f$ ≤ 15ns (10% to 90%); duty cycle = 50%; $Z_{out}$ = 50Ω. Output load capacitance $C_L$ = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture. Channel bias resistance $R_L$ = as specified.

Propagation delay times shall be measured as follows:




t_r
t_f
V_DD
90%
50%
COM
10%
V_SS
t_PHL
t_PLH
V_OH
50%
CH0
V_OL


t_r
t_r
INH
V_DD
90%
90%
50%
50%
10%
V_SS
t_PZH2
t_PHZ2
V_OH
90%
50%
COM
V_OL


t_r
t_r
V_DD
90%
90%
50%
50%
A
10%
10%
V_SS
t_PZH1
t_PHZ1
V_OH
90%
50%
COM
V_OL

## 2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb}$ = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Quiescent Current | $I_{DD}$ | ±75 | - | 500 | nA |
| Channel ON Resistance 1, CH4 to COM, COM to CH4 Note 2 | $R_{ON1}$ | ±50 | - | 1050 | Ω |
| Channel ON Resistance 2, CH4 to COM, COM to CH4 Note 2 | $R_{ON2}$ | ±15 | - | 280 | Ω |
| Threshold Voltage N-Channel | $V_{THN}$ | ±0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | ±0.3 | 0.7 | 3 | V |

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Channel ON Resistance shall be tested at each input voltage level specified in Para. 2.3.1, Room Temperature Electrical Measurements in both directions for CH4 to COM only.

## 2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb}$ = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Functional Test 1 | - | - | - | - | - |
| Quiescent Current | $I_{DD}$ | ±75 | - | 500 | nA |
| Low Level Input Current, Control Inputs | $I_{IL}$ | - | - | -50 | nA |
| High Level Input Current, Control Inputs | $I_{IH}$ | - | - | 50 | nA |

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Channel OFF Leakage Current 1, Any Channel CHn | $I_{OFF1}$ | - | - | -100 | nA |
| Channel OFF Leakage Current 3, All Channels Tested Together | $I_{OFF3}$ | - | - | 100 | nA |
| Channel ON Resistance 1 | $R_{ON1}$ | ±50 | - | 1050 | Ω |
| Channel ON Resistance 2 | $R_{ON2}$ | ±15 | | 280 | Ω |
| Low Level Input Voltage 1, (Noise Immunity) (Functional Test) | $V_{IL1}$ | - | - | 1.5 | V |
| High Level Input Voltage 1, (Noise Immunity) (Functional Test) | $V_{IH1}$ | - | 3.5 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | ±0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | ±0.3 | 0.7 | 3 | V |

**NOTES:**
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.

## 2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

### 2.6.1 N-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | °C |
| Output COM | $V_{OUT}$ | $V_{SS}$ | V |
| Inputs CHn | $V_{IN}$ | $V_{DD}$ | V |
| Inputs INH, A, B, C | $V_{IN}$ | $V_{DD}$ | V |
| Positive Supply Voltage | $V_{DD}$ | 15 (+0 -0.5) | V |
| Digital Negative Supply Voltage | $V_{SS}$ | 0 | V |
| Analogue Negative Supply Voltage | $V_{EE}$ | 0 | V |
| Duration | t | 72 | Hours |

**NOTES:**
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | °C |
| Output COM | $V_{OUT}$ | $V_{SS}$ | V |
| Inputs CHn | $V_{IN}$ | $V_{SS}$ | V |
| Inputs INH, A, B, C | $V_{IN}$ | $V_{DD}$ | V |
| Positive Supply Voltage | $V_{DD}$ | 15 (+0 -0.5) | V |
| Digital Negative Supply Voltage | $V_{SS}$ | 0 | V |
| Analogue Negative Supply Voltage | $V_{EE}$ | 0 | V |
| Duration | t | 72 | Hours |

**NOTES:**
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | °C |
| Output COM | $V_{OUT}$ | $V_{SS}$ | V |
| Inputs CHn | $V_{IN}$ | $V_{DD}$ | V |
| Input A | $V_{IN}$ | $V_{GEN1}$ | V |
| Input B | $V_{IN}$ | $V_{GEN2}$ | V |
| Input C | $V_{IN}$ | $V_{GEN3}$ | V |
| Input INH | $V_{IN}$ | $V_{GEN4}$ | V |
| Pulse Voltage | $V_{GEN}$ | 0V to $V_{DD}$ | V |
| Pulse Frequency Square Wave | $f_{GEN1}$<br>$f_{GEN2}$<br>$f_{GEN3}$<br>$f_{GEN4}$ | 500k<br>250k<br>125k<br>62.5k<br>50% Duty Cycle | Hz |
| Positive Supply Voltage | $V_{DD}$ | 15 (+0 -0.5) | V |
| Digital Negative Supply Voltage | $V_{SS}$ | 0 | V |
| Analogue Negative Supply Voltage | $V_{EE}$ | 0 | V |

**NOTES:**
1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.7, Power Burn-in Conditions.

**APPENDIX 'A'**

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Para. 2.1.1 Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3 | External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).<br>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.<br>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.<br>Solderability is not applicable unless specifically stipulated in the Purchase Order. |
| Para. 2.1.1 Deviations from the Generic Specification: Deviations from Qualification and Periodic Tests - Chart F4 | External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).<br>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. |
| Para. 2.3.1 Room Temperature Electrical Measurements | All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.<br>A summary of the pilot lot testing shall be provided if required by the Purchase Order. |
| Para. 2.3.2 High and Low Temperatures Electrical Measurements | High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.<br>A summary of the pilot lot testing shall be provided if required by the Purchase Order. |