INTEGRATED CIRCUITS, SILICON MONOLITHIC, HCMOS, QUAD 2-INPUT EXCLUSIVE-NOR GATE WITH OPEN DRAIN OUTPUTS

BASED ON TYPE 54HC266

ESCC Detail Specification No. 9201/122

Issue 4	October 2016

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1002	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920112201F

- Detail Specification Reference: 9201122
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: F (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and/or Finish	Weight max g	Total Dose Radiation Level Letter
01	54HC266	FP	G2	0.7	F [50krad(Si)]
02	54HC266	FP	G4	0.7	F [50krad(Si)]
03	54HC266	DIP	G2	2.2	F [50krad(Si)]
04	54HC266	DIP	G4	2.2	F [50krad(Si)]
05	54HC266	CCP	2	0.6	F [50krad(Si)]
10	54HC266	SO	G2	0.7	F [50krad(Si)]
11	54HC266	SO	G4	0.7	F [50krad(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	Notes 1, 2
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V	Notes 1, 3
Device Power Dissipation (Continuous)	P_D	300	mW	Note 4
Supply Current	I_{DDop}	50	mA	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Soldering Temperature For FP, DIP and SO For CCP	T_{sol}	 +265 +245	°C	 Note 5 Note 6

NOTES:

1. Device is functional for $2V \leq V_{DD} \leq 6V$.
2. Input current limited to $I_{IC} = \pm 20mA$.
3. Output current limited to $I_{OUT} = \pm 25mA$.
4. The maximum device dissipation is determined by I_{DDop} max (50mA) × 6V.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

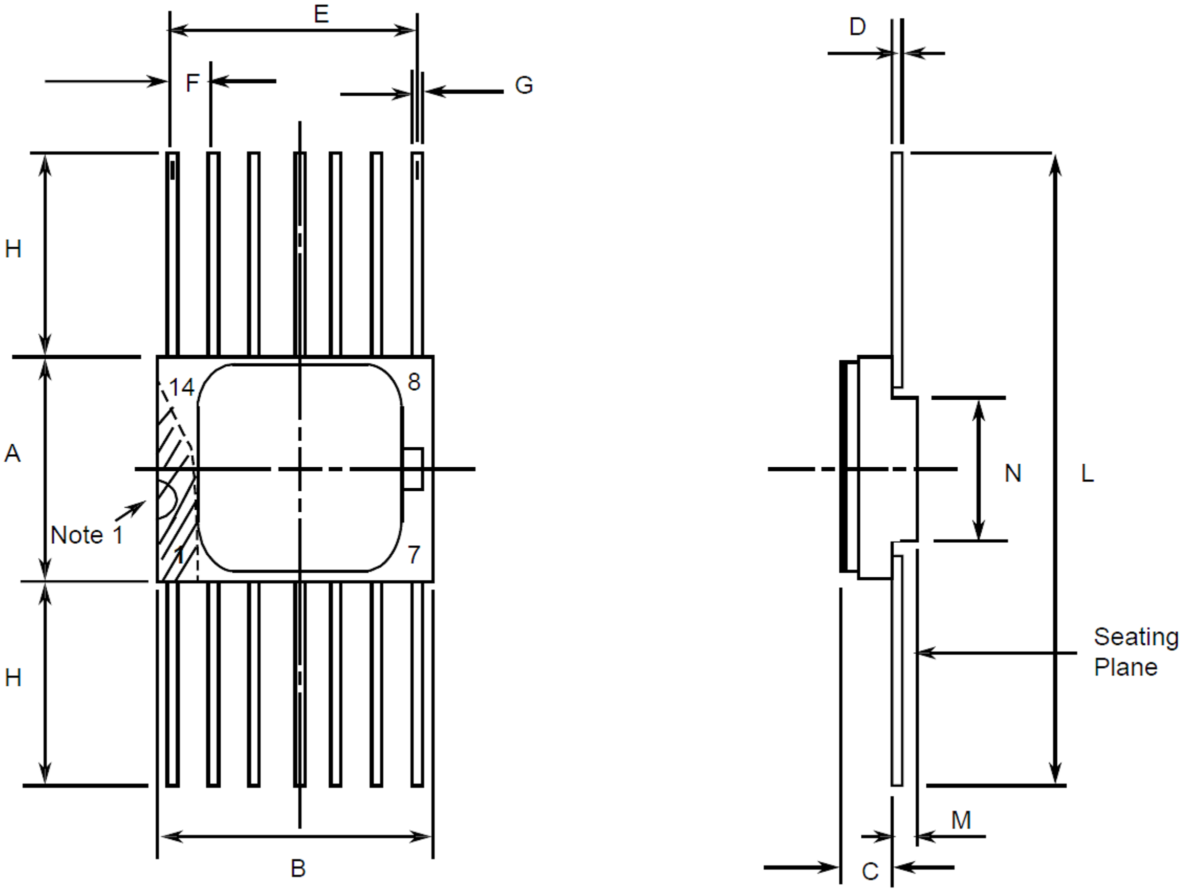
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

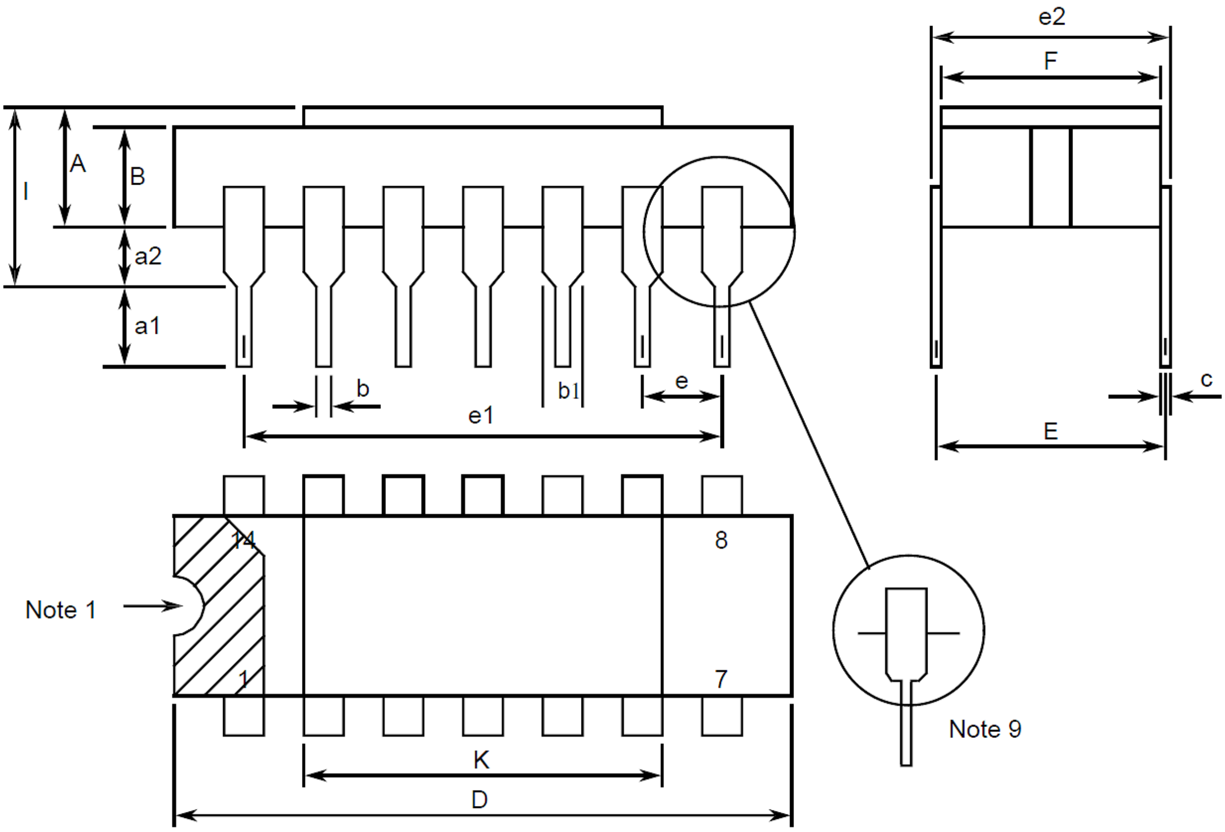
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 14 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	7.5	7.75	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

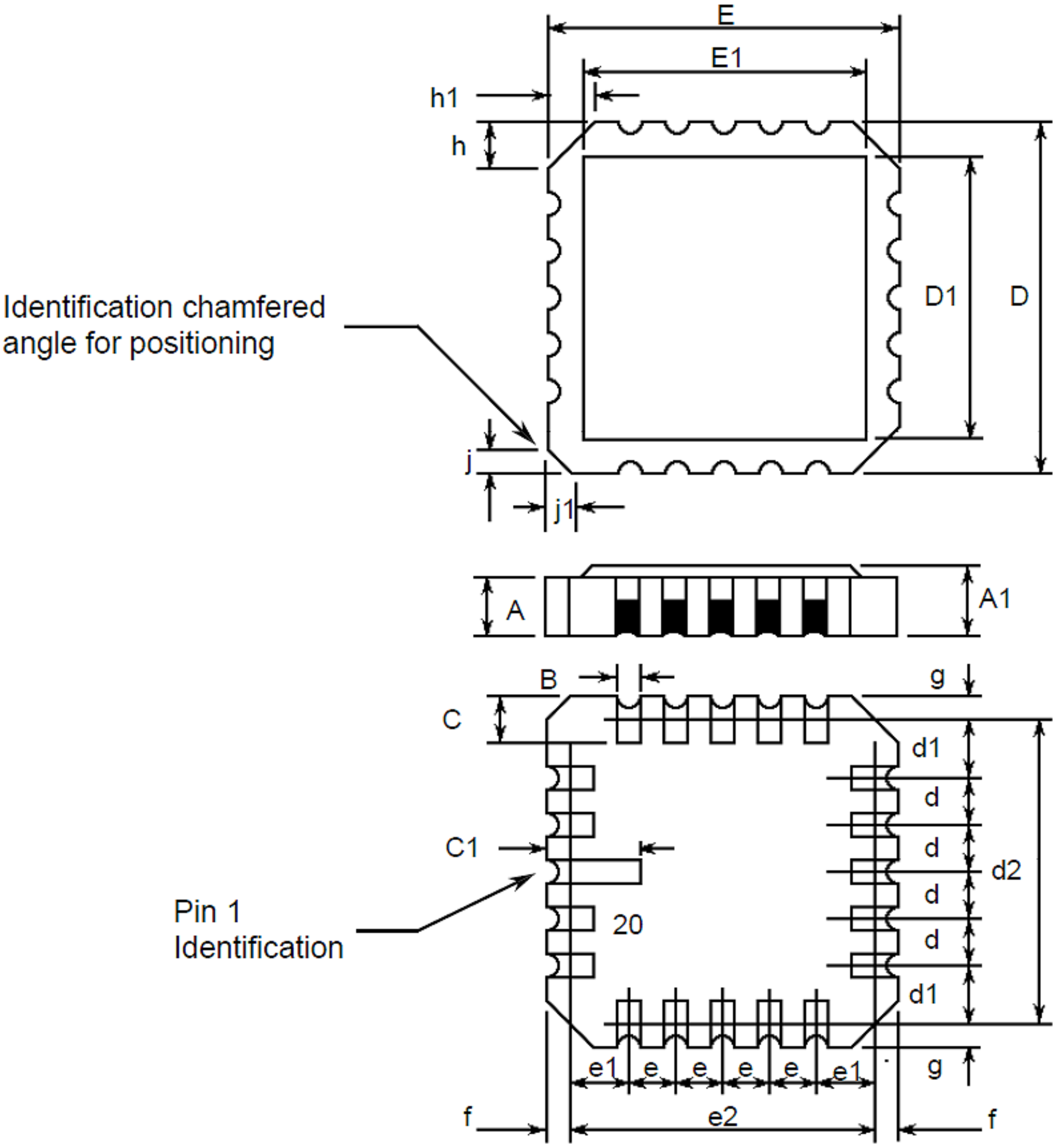
1.7.2 Dual-in-line Package (DIP) - 14 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.54	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.23	
b	0.4	0.5	5
b1	1.27 TYPICAL		5
c	0.2	0.3	5
D	18.79	19.2	
E	7.36	7.87	
e	2.54 BSC		4, 6
e1	15.11	15.37	
e2	7.62	8.12	
F	7.11	7.75	
I	-	3.7	

Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

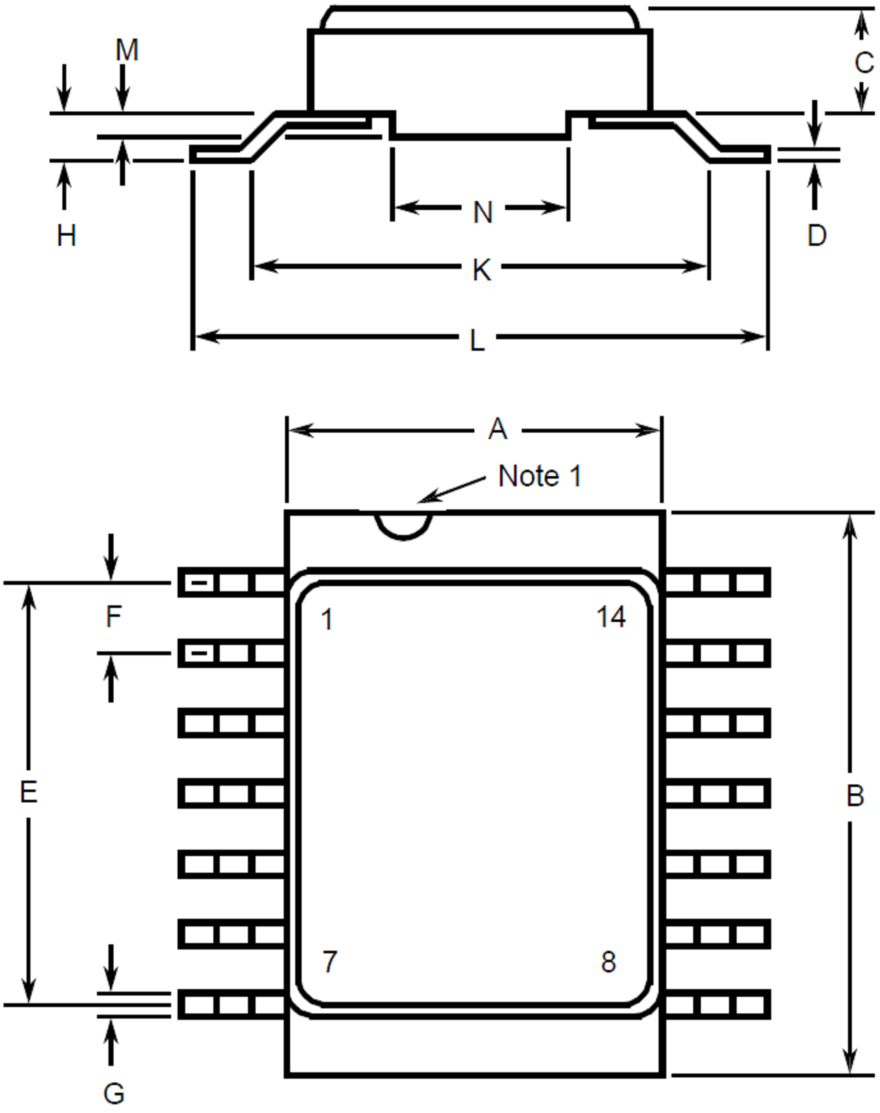
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5

Symbols	Dimensions mm		Notes
	Min	Max	
C1	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 BSC		3
d2	7.62 BSC		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 BSC		3
e2	7.62 BSC		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 14 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	7.5	7.75	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

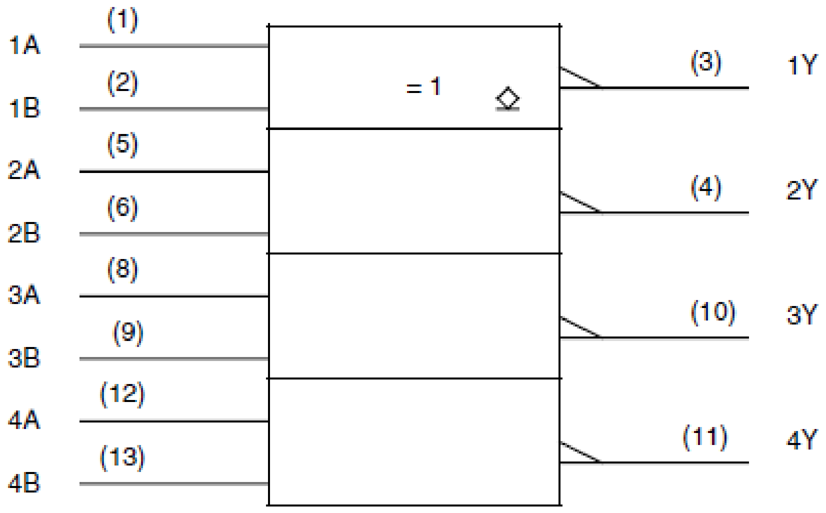
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 12 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	1A Input	-	11	4Y Output	-
2	1B Input	1A Input	12	4A Input	3A Input
3	1Y Output	1B Input	13	4B Input	3B Input
4	2Y Output	1Y Output	14	V_{DD}	3Y Output
5	2A Input	-	15	-	-
6	2B input	2Y Output	16	-	4Y Output
7	V_{SS}	-	17	-	-
8	3A Input	2A Input	18	-	4A Input
9	3B Input	2B Input	19	-	4B Input
10	3Y Output	V_{SS}	20	-	V_{DD}

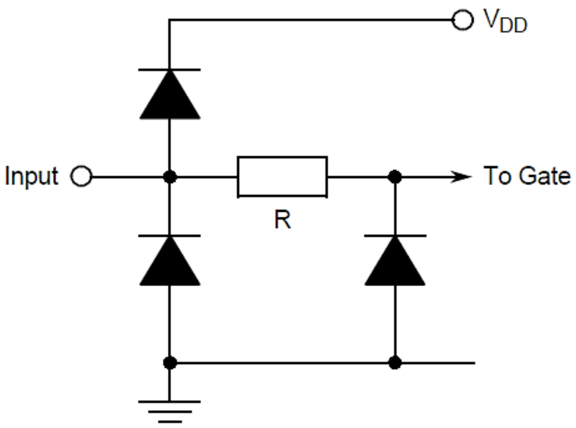
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, Z = High Impedance.
2. Positive Logic: $Y = \overline{A \oplus B}$.

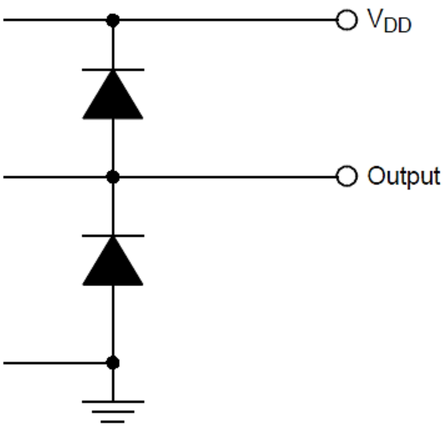
INPUTS		OUTPUT Y
A	B	
L	L	Z
L	H	L
H	L	L
H	H	Z

1.11 PROTECTION NETWORKS

INPUT PROTECTION



OUTPUT PROTECTION



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component’s reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb} = +22 \pm 3°C$.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load $V_{IL} = 0.3V$, $V_{IH} = 1.5V$ $V_{DD} = 2V$, $V_{SS} = 0V$ $t_r < 1\mu s$ Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load $V_{IL} = 0.9V$, $V_{IH} = 3.15V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ $t_r = t_f < 500ns$ Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table without Load $V_{IL} = 1.2V$, $V_{IH} = 4.2V$ $V_{DD} = 6V$, $V_{SS} = 0V$ $t_r = t_f < 400ns$ Note 2	-	-	-
Quiescent Current	I_{DD}	3005	$V_{IL} = 0V$, $V_{IH} = 6V$ $V_{DD} = 6V$, $V_{SS} = 0V$ All Outputs Open Note 3	-	100	nA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 6V $V_{DD} = 6V$, $V_{SS} = 0V$	-	-50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 6V V_{IN} (Remaining Inputs) = 0V $V_{DD} = 6V$, $V_{SS} = 0V$	-	50	nA
Low Level Output Voltage 1	V_{OL1}	3007	Gate Under Test: $V_{IN1} = 1.5V$, $V_{IN2} = 0.3V$ $I_{OL} = 20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 2V$, $V_{SS} = 0V$	-	100	mV
Low Level Output Voltage 2	V_{OL2}	3007	Gate Under Test: $V_{IN1} = 3.15V$, $V_{IN2} = 0.9V$ $I_{OL} = 20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$	-	100	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Voltage 3	V_{OL3}	3007	Gate Under Test: V_{IN1} = 4.2V, V_{IN2} = 1.2V I_{OL} = 20µA All Other Gates: V_{IN} = 0V V_{DD} = 6V, V_{SS} = 0V	-	100	mV
Low Level Output Voltage 4	V_{OL4}	3007	Gate Under Test: V_{IN1} = 3.15V, V_{IN2} = 0.9V I_{OL} = 4mA All Other Gates: V_{IN} = 0V V_{DD} = 4.5V, V_{SS} = 0V	-	260	mV
Low Level Output Voltage 5	V_{OL5}	3007	Gate Under Test: V_{IN1} = 4.2V, V_{IN2} = 1.2V I_{OL} = 5.2mA All Other Gates: V_{IN} = 0V V_{DD} = 6V, V_{SS} = 0V	-	260	mV
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	Gate Under Test: V_{IN} = 4.2V, V_{OUT} = 6V All Other Gates: V_{IN} = 0V V_{DD} = 6V, V_{SS} = 0V	-	500	nA
Threshold Voltage N-Channel	V_{THN}	-	1A Input at Ground All Other Inputs: V_{IN} = 5V V_{DD} = 5V, I_{SS} = -10µA	-0.45	-1.45	V
Threshold Voltage P-Channel	V_{THP}	-	1A and 1B Inputs at Ground All Other Inputs: V_{IN} = -5V V_{SS} = -5V, I_{DD} = 10µA	0.45	1.35	V
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open	-400	-900	mV
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	I_{IN} (Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open	400	900	mV
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V f = 100kHz to 1MHz Note 4	-	10	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Propagation Delay Low to High, 1A to 1Y	t_{PLH}	3003	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{IL} = 0V, V_{IH} = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5	-	25	ns
Propagation Delay High to Low, 1A to 1Y	t_{PHL}	3003	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{IL} = 0V, V_{IH} = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5	-	20	ns
Transition Time Low to High	t_{TLH}	3004	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{IL} = 0V, V_{IH} = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5	-	15	ns
Transition Time High to Low	t_{THL}	3004	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{IL} = 0V, V_{IH} = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5	-	15	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL} = 0.3V, V_{IH} = 1.5V V_{DD} = 2V, V_{SS} = 0V t_r < 1µs Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL} = 0.9V, V_{IH} = 3.15V V_{DD} = 4.5V, V_{SS} = 0V t_r = t_f < 500ns Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table without Load V_{IL} = 1.2V, V_{IH} = 4.2V V_{DD} = 6V, V_{SS} = 0V t_r = t_f < 400ns Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL} = 0V, V_{IH} = 6V V_{DD} = 6V, V_{SS} = 0V All Outputs Open Note 3	-	2	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 6V V_{DD} = 6V, V_{SS} = 0V	-	-1	µA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 6V V_{IN} (Remaining Inputs) = 0V V_{DD} = 6V, V_{SS} = 0V	-	1	µA
Low Level Output Voltage 1	V_{OL1}	3007	Gate Under Test: V_{IN1} = 1.5V, V_{IN2} = 0.3V I_{OL} = 20µA All Other Gates: V_{IN} = 0V V_{DD} = 2V, V_{SS} = 0V	-	100	mV
Low Level Output Voltage 2	V_{OL2}	3007	Gate Under Test: V_{IN1} = 3.15V, V_{IN2} = 0.9V I_{OL} = 20µA All Other Gates: V_{IN} = 0V V_{DD} = 4.5V, V_{SS} = 0V	-	100	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Voltage 3	V_{OL3}	3007	Gate Under Test: $V_{IN1} = 4.2V$, $V_{IN2} = 1.2V$ $I_{OL} = 20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 6V$, $V_{SS} = 0V$	-	100	mV
Low Level Output Voltage 4	V_{OL4}	3007	Gate Under Test: $V_{IN1} = 3.15V$, $V_{IN2} = 0.9V$ $I_{OL} = 4mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$	-	400	mV
Low Level Output Voltage 5	V_{OL5}	3007	Gate Under Test: $V_{IN1} = 4.2V$, $V_{IN2} = 1.2V$ $I_{OL} = 5.2mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 6V$, $V_{SS} = 0V$	-	400	mV
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	Gate Under Test: $V_{IN} = 4.2V$, $V_{OUT} = 6V$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 6V$, $V_{SS} = 0V$	-	10	µA
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test) = -100µA V_{DD} = Open, $V_{SS} = 0V$ All Other Pins Open	-0.1	-1.2	V
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	I_{IN} (Under Test) = 100µA $V_{DD} = 0V$, V_{SS} = Open All Other Pins Open	0.1	1.2	V

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed with f = 10kHz (min). The maximum time to output comparator strobe = 30µs.
3. Quiescent Current shall be tested using the following input conditions:
    (a) A inputs = V_{IH}; B inputs = V_{IL}
    (b) A inputs = V_{IL}; B inputs = V_{IH}
    (c) A inputs = B inputs = V_{IH}
    (d) A inputs = B inputs = V_{IL}
4. Guaranteed but not tested.
5. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.
    The pulse generator shall have the following characteristics:
    V_{GEN} = 0 to V_{DD}; f_{GEN} = 1MHz minimum; t_r and $t_f \leq 6ns$ (10% to 90%); duty cycle = 50%; $Z_{out} = 50\Omega$.

Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture and output load resistance R_L = 1kΩ ±5%.
Propagation delay shall be measured referenced to the 50% input and output voltages.
Transition time shall be measured referenced to the 10% and 90% output voltage.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	±30	-	100	nA
Low Level Input Current	I_{IL}	±20	-	-50	nA
High Level Input Current	I_{IH}	±20	-	50	nA
Low Level Output Voltage 4	V_{OL4}	±26	-	260	mV
Output Leakage Current Third State, High Level Applied	I_{OZH}	±200	-	500	nA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.45	-1.45	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.45	1.35	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Functional Test 2	-	-	-	-	-

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 3	-	-	-	-	-
Quiescent Current	I_{DD}	±30	-	100	nA
Low Level Input Current	I_{IL}	±20	-	-50	nA
High Level Input Current	I_{IH}	±20	-	50	nA
Low Level Output Voltage 4	V_{OL4}	±26	-	260	mV
Low Level Output Voltage 5	V_{OL5}	±26	-	260	mV
Output Leakage Current Third State, High Level Applied	I_{OZH}	±200	-	500	nA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.45	-1.45	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.45	1.35	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Y (all gates)	V_{OUT}	Open or V_{SS}	V
Inputs A, B (all gates)	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	6 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Y (all gates)	V_{OUT}	Open or V_{DD}	V
Inputs A, B (all gates)	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	6 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Y (all gates)	V_{OUT}	V_{DD}	V
Inputs 1A, 2B, 3B, 4A	V_{IN}	V_{DD}	V
Inputs 1B, 2A, 3A, 4B	V_{IN}	V_{GEN}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	100k ±10% 50 ±15% Duty Cycle $t_r = t_f \leq 400$ns	Hz
Positive Supply Voltage	V_{DD}	6 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	°C
Outputs Y (all gates)	V_{OUT}	Open	V
Inputs A (all gates)	V_{IN}	V_{SS}	V
Inputs B (all gates)	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	6 ±0.3	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = 680Ω min to 47kΩ max.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	-	-	10	μA
Threshold Voltage N-Channel	V_{THN}	±0.6	-0.4	-1.5	V
Threshold Voltage P-Channel	V_{THP}	±0.6	0.4	1.4	V

APPENDIX ‘A’

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255. Solderability is not applicable unless specifically stipulated in the Purchase Order.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.