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INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DUAL COMPLEMENTARY PAIR PLUS INVERTER WITH UNBUFFERED OUTPUTS

BASED ON TYPE 4007UB

ESCC Detail Specification No. 9202/038

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DCR No.	CHANGE DESCRIPTION
125, 90	Specification up issued to incorporate editorial and technical changes per DCR.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920203801

- Detail Specification Reference: 9202038
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g
01	4007UB	FP	G2	0.7
02	4007UB	FP	G4	0.7
03	4007UB	DIP	G2	2.2
04	4007UB	DIP	G4	2.2
07	4007UB	CCP	2	0.6
08	4007UB	SO	G2	0.7
09	4007UB	SO	G4	0.7

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 18	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	Note 1 Power on
Input Current	I_{IN}	±10	mA	-
Device Power Dissipation (Continuous)	P_D	200	mW	-
Power Dissipation per Output	P_{DSO}	100	mW	-
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	-
Soldering Temperature For FP, DIP and SO For CCP	T_{sol}	 +265 +245	^oC	 Note 2 Note 3

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

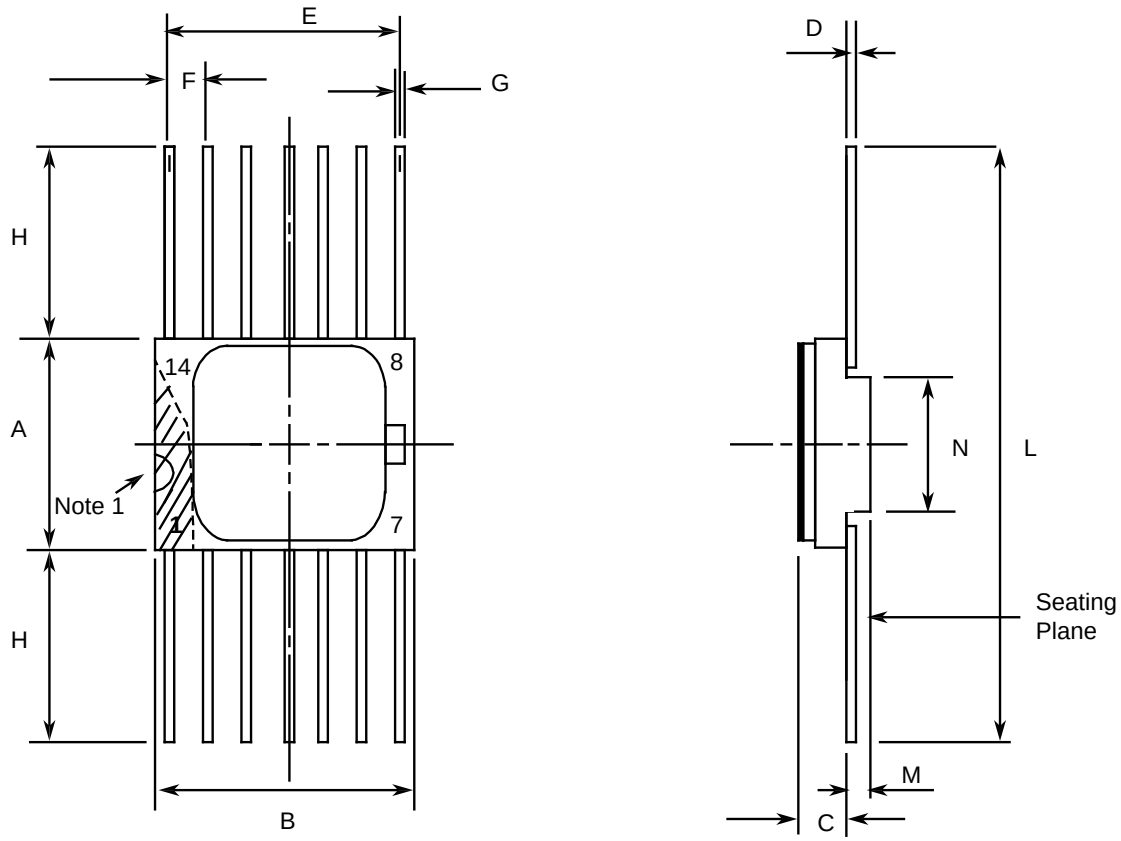
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

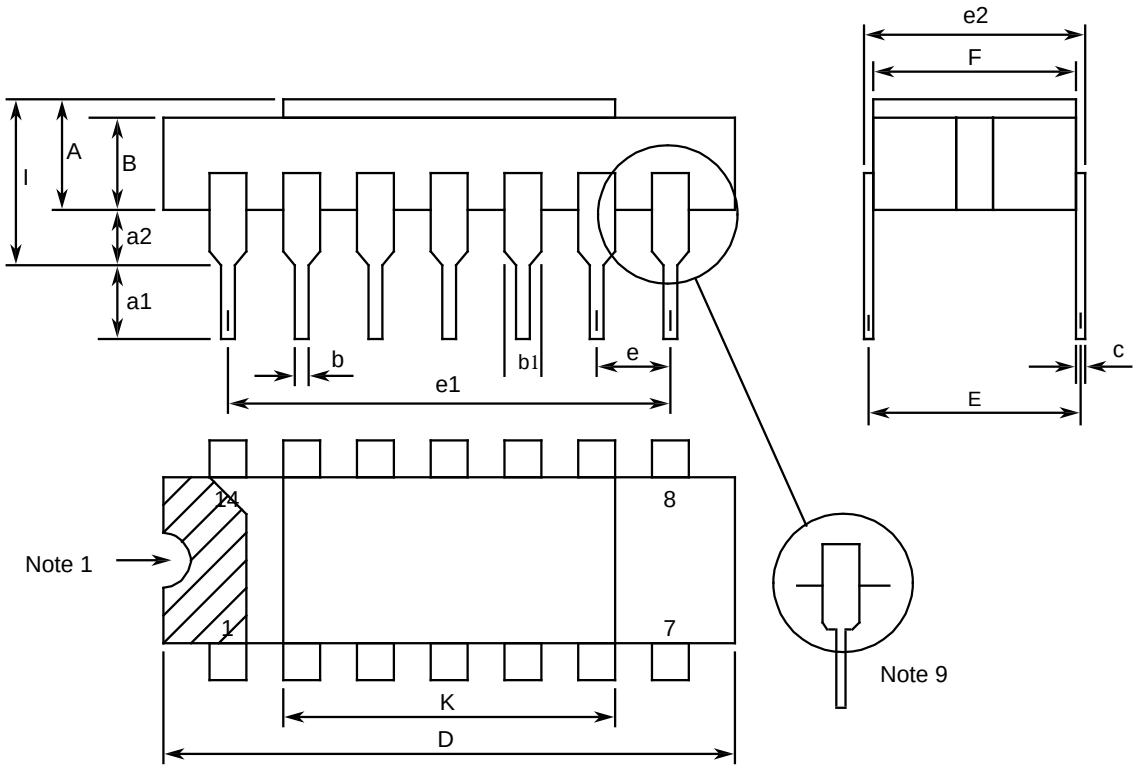
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 14 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	7.5	7.75	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

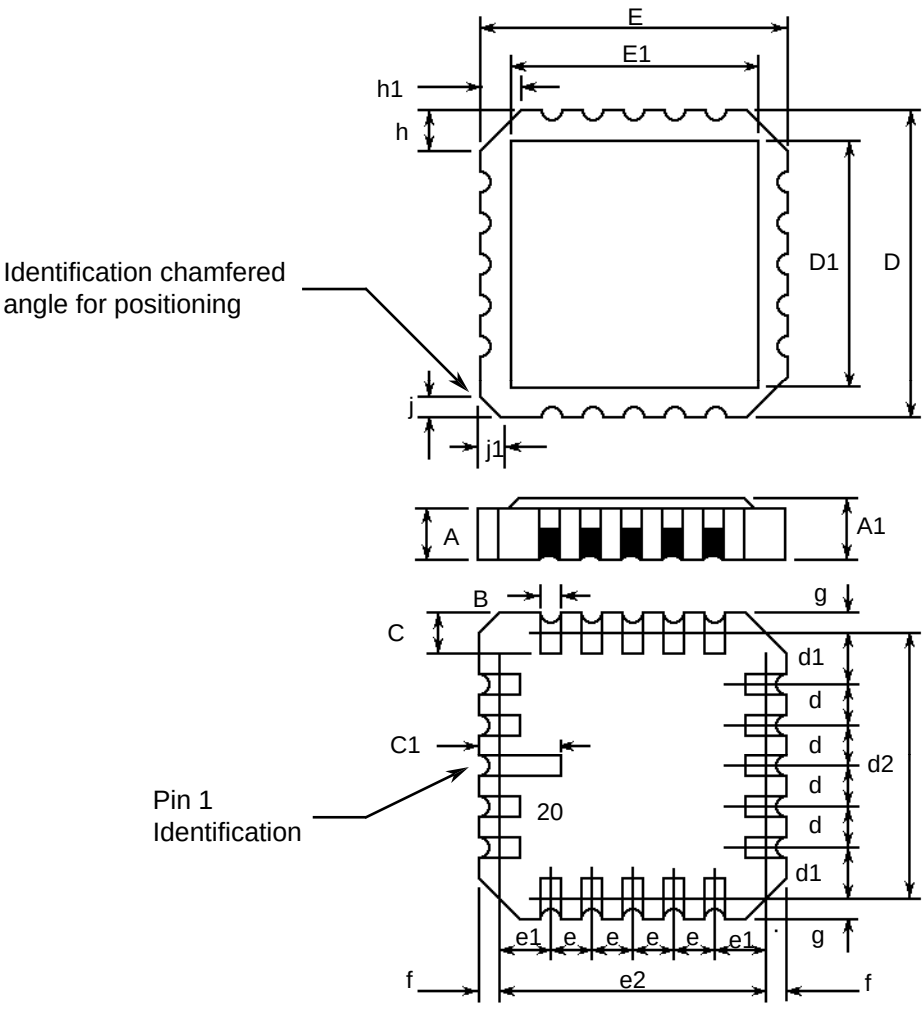
1.7.2 Dual-in-line Package (DIP) - 14 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.54	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.23	
b	0.4	0.5	5
b1	1.27 TYPICAL		5
c	0.2	0.3	5
D	18.79	19.2	
E	7.36	7.87	
e	2.54 TYPICAL		4, 6
e1	15.11	15.37	
e2	7.62	8.12	
F	7.11	7.75	
I	-	3.7	

Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

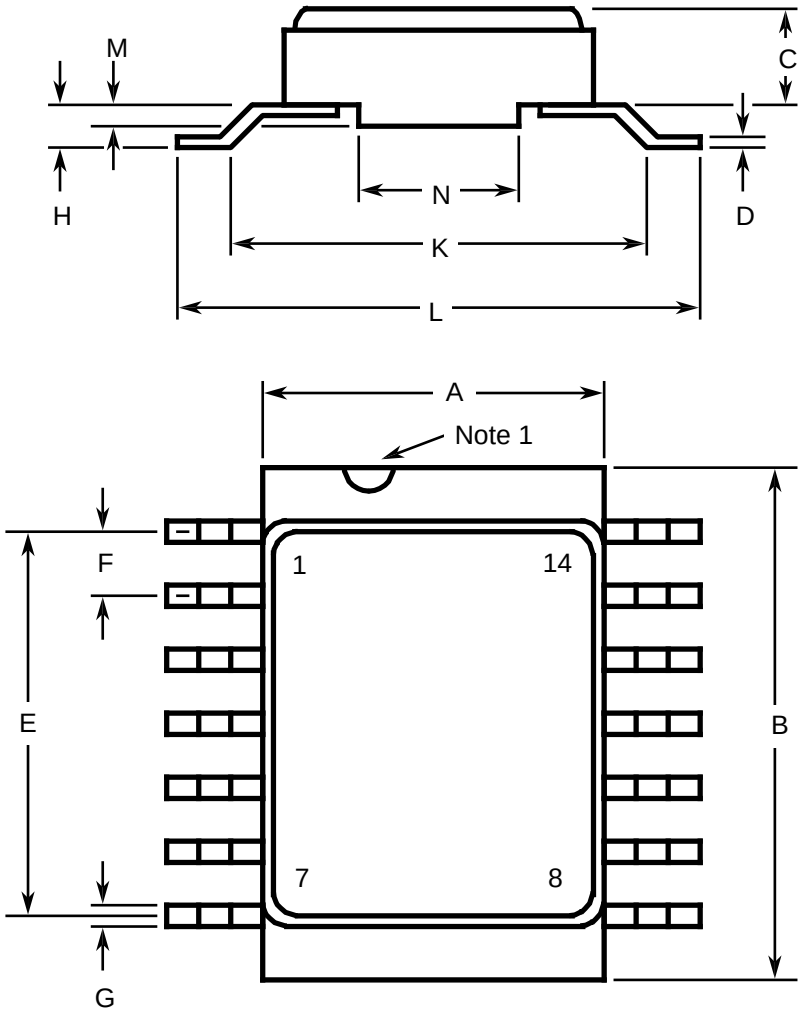
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	

Symbols	Dimensions mm		Notes
	Min	Max	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 TYPICAL		3, 6
d2	7.62 TYPICAL		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 TYPICAL		3, 6
e2	7.62 TYPICAL		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 14 Pin



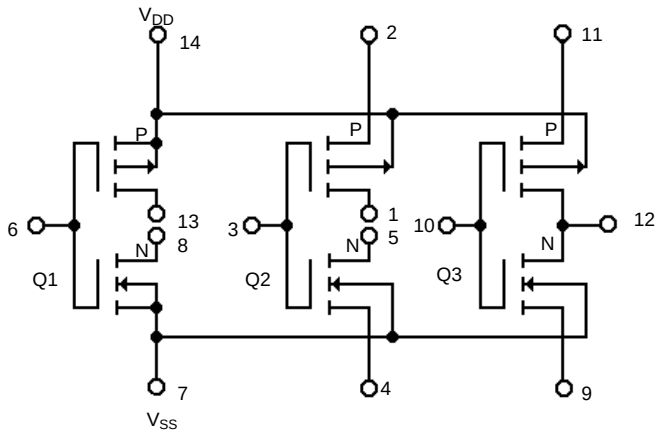
Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	7.5	7.75	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	0.6	0.9	5
K	9 TYPICAL		
L	10	10.65	

Symbols	Dimensions mm		Notes
	Min	Max	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 12 spaces for flat, dual-in-line and small outline packages.
   16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM



Pin No.	Symbol	Description	Pin No.	Symbol	Discription
1	Q2PS	Q2(P) SOURCE	8	Q1ND	Q1(N) DRAIN
2	Q2PD	Q2(P) DRAIN	9	Q3NS	Q3(N) SOURCE
3	Q2G	Q2 GATES	10	Q3G	Q3 GATES
4	Q2NS	Q2(N) SOURCE	11	Q3PD	Q3(P) DRAIN
5	Q2ND	Q2(N) DRAIN	12	Q3ND/ Q3PS	Q3(N) DRAIN, Q3(P) SOURCE
6	Q1G	Q1 GATES	13	Q1PS	Q1(P) SOURCE
7	V_{SS}	V_{SS}, Q1-Q2-Q3(N) SUBSTRATES, Q1(N) SOURCE	14	V_{DD}	V_{DD}, Q1-Q2-Q3(P) SUBSTRATES, Q1(P) DRAIN

NOTES:

1. Pin numbers relate to FP, DIP and SO packages only
2. For the purpose of testing in accordance with this specification, unless otherwise specified, the component pins shall be connected as follows to configure the component to function as a Triple Inverter (Positive Logic $Y = \overline{A}$) :

V_{DD} = Q2PD = Q3PD (Pin 14 to 2 to 11)

V_{SS} = Q2NS = Q3NS (Pin 7 to 4 to 9)

Q1ND = Q1PS (Pin 8 to 13)

Q2ND = Q2PS (Pin 5 to 1)

EACH INVERTER

1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	Q2PS Output (2Y)	-	11	Q3PD	-
2	Q2PD	Q2PS Output (2Y)	12	Q3ND/Q3PS Output (3Y)	Q1ND Output (1Y)
3	Q2G input (2A)	-	13	Q1PS Output (1Y)	-
4	Q2NS	Q2PD	14	V_{DD}	Q3NS
5	Q2ND Output (2Y)	Q2G input (2A)	15	-	Q3G Input (3A)
6	Q1G Input (1A)	Q2NS	16	-	Q3PD
7	V_{SS}	Q2ND Output (2Y)	17	-	Q3ND/Q3PS Output (3Y)
8	Q1ND Output (1Y)	-	18	-	-
9	Q3NS	Q1G Input (1A)	19	-	Q1PS Output (1Y)
10	Q3G Input (3A)	V_{SS}	20	-	V_{DD}

NOTES:

1. The definition of Input and Output pins is based on configuration of the component to function as a Triple Inverter.

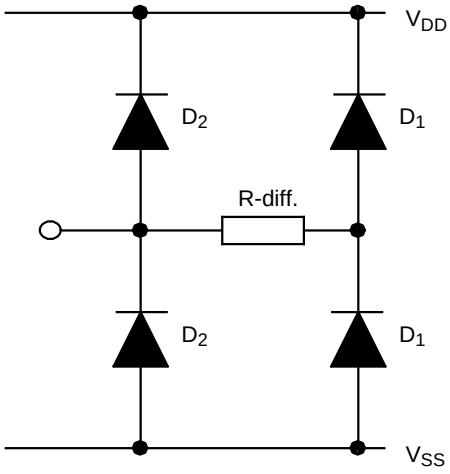
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level.
2. Positive Logic: Y = $\overline{A}$.
3. The truth table is based on configuration of the component to function as a Triple Inverter.

EACH GATE

INPUT (A)	OUTPUT (Y)
QnG	QnND/QnPS
L	H
H	L

1.11 INPUT PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3	-	100	nA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=15V,V_{SS}=0V	-	-50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=15V V_{DD}=15V,V_{SS}=0V	-	50	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0V, V_{IH}=15V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL}=1V, V_{IH}=4V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL}=2.5V, V_{IH}=12.5V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0V, V_{IH}=15V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL}=1V, V_{IH}=4V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL}=2.5V, V_{IH}=12.5V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V
Low Level Output Current 1	I_{OL1}	-	V_{IL}=0V, V_{IH}=5V, V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V Note 4	510	-	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Current 2	I_{OL2}	-	V_{IL}=0V, V_{IH}=15V, V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 4	3.4	-	mA
High Level Output Current 1	I_{OH1}	-	V_{IL}=0V, V_{IH}=5V, V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 4	-510	-	µA
High Level Output Current 2	I_{OH2}	-	V_{IL}=0V, V_{IH}=15V, V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 4	-3.4	-	mA
Threshold Voltage N-Channel	V_{THN}	-	Q3G at Ground Q2NS and Q3NS Connected to V_{SS} All Other pins: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	-	Q3G at Ground Q2PS and Q3PS Connected to V_{DD} All Other pins: V_{IN}=-5V V_{DD}=-5V, I_{SS}=10µA	0.7	3	V
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test)= -100µA V_{DD}=Open, V_{SS}=0V All Other Pins Open	-	-2	V
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	V_{IN} (Under Test)=6V R=30kΩ, V_{SS}=Open All Other Pins Open Note 5	3	-	V
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test)=0V V_{DD}= V_{SS}=0V f = 100 kHz to 1 MHz Note 6	-	7.5	pF
Propagation Delay Low to High, Q3G to Q3ND/Q3PS (3A to 3Y)	t_{PLH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	90	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Propagation Delay High to Low, Q3G to Q3ND/Q3PS (3A to 3Y)	t_{PHL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	90	ns
Transition Time Low to High, Q3ND/Q3PS (3Y)	t_{TLH}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	150	ns
Transition Time High to Low, Q3ND/Q3PS (3Y)	t_{THL}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	150	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^{o}C and T_{amb}=- 55(+5-0)^{o}C.

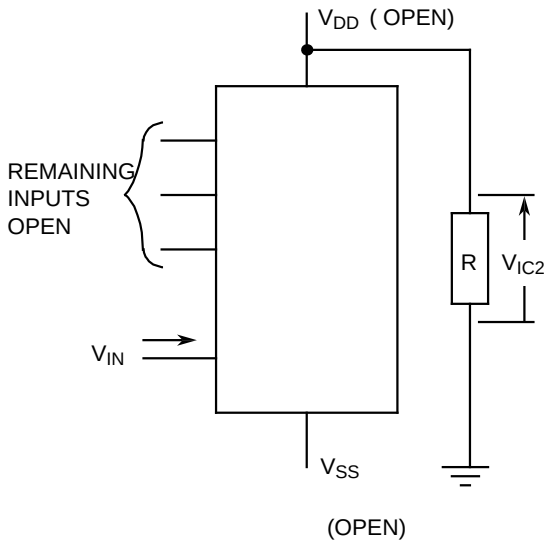
Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3 T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	- -	1 0.1	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=15V,V_{SS}=0V T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	- -	-100 -50	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=15V V_{DD}=15V,V_{SS}=0V T_{amb}=+125°C T_{amb}=- 55°C	 - -	 100 50	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0V, V_{IH}=15V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL}=1V, V_{IH}=4V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL}=2.5V, V_{IH}=12.5V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0V, V_{IH}=15V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL}=1V, V_{IH}=4V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL}=2.5V, V_{IH}=12.5V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V
Low Level Output Current 1	I_{OL1}	-	V_{IL}=0V, V_{IH}=5V, V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V Note 4 T_{amb}=+125°C T_{amb}=- 55°C	 400 800	 - -	µA
Low Level Output Current 2	I_{OL2}	-	V_{IL}=0V, V_{IH}=15V, V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 4 T_{amb}=+125°C T_{amb}=- 55°C	 3.1 5.4	 - -	mA
High Level Output Current 1	I_{OH1}	-	V_{IL}=0V, V_{IH}=5V, V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 4 T_{amb}=+125°C T_{amb}=- 55°C	 -400 -800	 - -	µA
High Level Output Current 2	I_{OH2}	-	V_{IL}=0V, V_{IH}=15V, V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 4 T_{amb}=+125°C T_{amb}=- 55°C	 -3.1 -5.4	 - -	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Threshold Voltage N-Channel	V_{THN}	-	Q3G at Ground Q2NS and Q3NS Connected to V_{SS} All Other Inputs: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA T_{amb}=+125°C T_{amb}=- 55°C	 -0.3 -0.7	 -3.5 -3.5	V
Threshold Voltage P-Channel	V_{THP}	-	Q3G at Ground Q2PS and Q3PS Connected to V_{DD} All Other Inputs: V_{IN}=-5V V_{SS}=-5V, I_{DD}=10µA T_{amb}=+125°C T_{amb}=- 55°C	 0.3 0.7	 3.5 3.5	V

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all tests shall be performed with the component configured to function as a Triple Inverter. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD}$ -0.5V, $V_{OL} \leq$ 0.5V. The Maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions:
   (a) All Inputs Q1G = Q2G = Q3G = V_{IH}.
   (b) All Inputs Q1G = Q2G = Q3G = V_{IL}.
4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:-



6. Guaranteed but not tested.
7. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
   The pulse generator shall have the following characteristics:

   V_{GEN} = 0 to V_{DD}; f = 500kHz; tr and t_f ≤15 ns (10% to 90%); duty cycle = 50%. Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture. Output load resistance R_L = 200kΩ.

   Propagation delay shall be measured referenced to the 50% input and output voltages.

   Transition time shall be measured referenced to the 10% and 90% output voltage.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	±50	-	100	nA
Low Level Output Current 1	I_{OL1}	±15% (2)	510	-	µA
High Level Output Current 1	I_{OH1}	±15% (2)	-510	-	µA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements .

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	I_{DD}	±50	-	100	nA
Low Level Input Current	I_{IL}	-	-	-50	nA
High Level Input Current	I_{IH}	-	-	50	nA
Low Level Output Voltage 1	V_{OL1}	-	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	-	-	500	mV
High Level Output Voltage 1	V_{OH1}	-	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	-	4.5	-	V
Low Level Output Current 1	I_{OL1}	±15% (3)	510	-	µA
Low Level Output Current 2	I_{OL2}	±15% (3)	3.4	-	mA
High Level Output Current 1	I_{OH1}	±15% (3)	-510	-	µA
High Level Output Current 2	I_{OH2}	±15% (3)	-3.4	-	mA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs Q1ND, Q1PS, Q2ND, Q2PS, Q3ND/Q3PS	V_{OUT}	Open	V
Inputs Q1G, Q2NS, Q3NS	V_{IN}	V_{SS}	V
Inputs Q2G, Q3G, Q2PD, Q3PD	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs Q1ND, Q1PS, Q2ND, Q2PS, Q3ND/Q3PS	V_{OUT}	Open	V
Inputs Q1G, Q2NS, Q3NS	V_{IN}	V_{DD}	V
Inputs Q2G, Q3G, Q2PD, Q3PD	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs Q1ND, Q1PS, Q2ND, Q2PS, Q3ND/Q3PS	V_{OUT}	$V_{DD}/2$	V
Inputs Q2PD, Q3PD	V_{IN}	V_{DD}	V
Inputs Q2NS, Q3NS	V_{IN}	V_{SS}	V
Inputs Q1G, Q2G, Q3G	V_{IN}	V_{GEN}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	50k ≤ f ≤ 1M 50% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.