DOCUMENT CHANGE REQUEST

DCR number 658	Changes required for: Qualification	Originator: John Wong
Date: 2011/05/27	Date sent: 2011/03/14	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Integrated Circuits, Monolithic, CMOS Silicon on Sapphire 3.5 GHz Delta-Sigma Modulated		
Number:	9202/077	Issue:	1

Other documents affected:

Page:

1.2 Applicable Documents

2.1 Deviations from Generic Specification

Paragraph:

1.2 Applicable Documents

2.1 Deviations from Generic Specification

Original wording:

Proposed wording:

Add the following deviation to 'Deviations from Screening Tests - Chart F3' (part of Appendix 'A' - Agreed Deviations for Peregrine Semiconductor Europe):

"Radiographic Inspection shall be performed in accordance with ESCC Basic Specification No. 20900. The Manufacturer may perform the inspection at any point during Screening Tests subsequent to Serialisation."

The text shall be added to the Description of Deviations column as a new item below "Room Temperature Electrical Measurements may be performed after Seal Test (Fine and Gross Leak)."

It follows that Paragraphs 1.2 (Applicable Documents) and 2.1 (Deviations from Generic Specification) are not affected.

The above change is also necessary for, and shall therefore be applied to, two other Detail Specs for components manufactured by PSE -
ESCC 9202/078 Issue 1;
ESCC 9202/079 Issue 1.

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New component will accummulate radiography inspection results.

Title:	Integrated Circuits, Monolithic, CMOS Silicon on Sapphire 3.5 GHz Delta-Sigma Modulated		
Number:	9202/077	Issue:	2

Other documents affected:

Page:

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Title:	Integrated Circuits, Monolithic, CMOS Silicon On Sapphire, 3.5GHz Integer-N PLL Frequency		
Number:	9202/078	Issue:	1

Other documents affected:

9202/079-1

Page:

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Attachments:

9202077.pdf, 20900.pdf, 2099000[1].pdf, null

Modifications:

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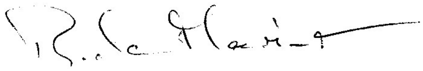
Approval signature:



Date signed:

2011-05-27

Pages 1 to 37

INTEGRATED CIRCUITS, MONOLITHIC, CMOS SILICON ON SAPPHIRE, 3.5GHZ DELTA-SIGMA MODULATED FRACTIONAL-N PLL FREQUENCY SYNTHESIZER

BASED ON TYPE PE33632

ESCC Detail Specification No. 9202/077

Issue 1	November 2010

Document Custodian: European Space Agency - see https://escies.org

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920207701R

- Detail Specification Reference: 9202077
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	PE33632	CQFPJ-68	G2	10	R [100kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Prolonged use of the device at the maximum ratings may reduce the device's overall reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage Range	V_{DD}	-0.3 to 4	V	Note 1
Input Voltage Range	V_{IN}	-0.3 to V_{DD}+0.3	V	Note 2
DC Input Current Range	I_{IN}	-10 to +10	mA	
DC Output Current Range	I_{OUT}	-90 to +110	mA	Note 3
Device Power Dissipation (Continuous)	P_D	500	mW	
Operating Temperature Range	T_{op}	-40 to +85	^{o}C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C	
Junction Temperature	T_j	+150	^{o}C	
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	15	$^{o}C/W$	
Soldering Temperature	T_{sol}	+260	^{o}C	Note 4

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional for $2.85 \le V_{DD} \le 3.45V$.
2. V_{DD} + 0.3V shall not exceed 4V.
3. The maximum output current of any single output for a maximum duration of 1 second.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

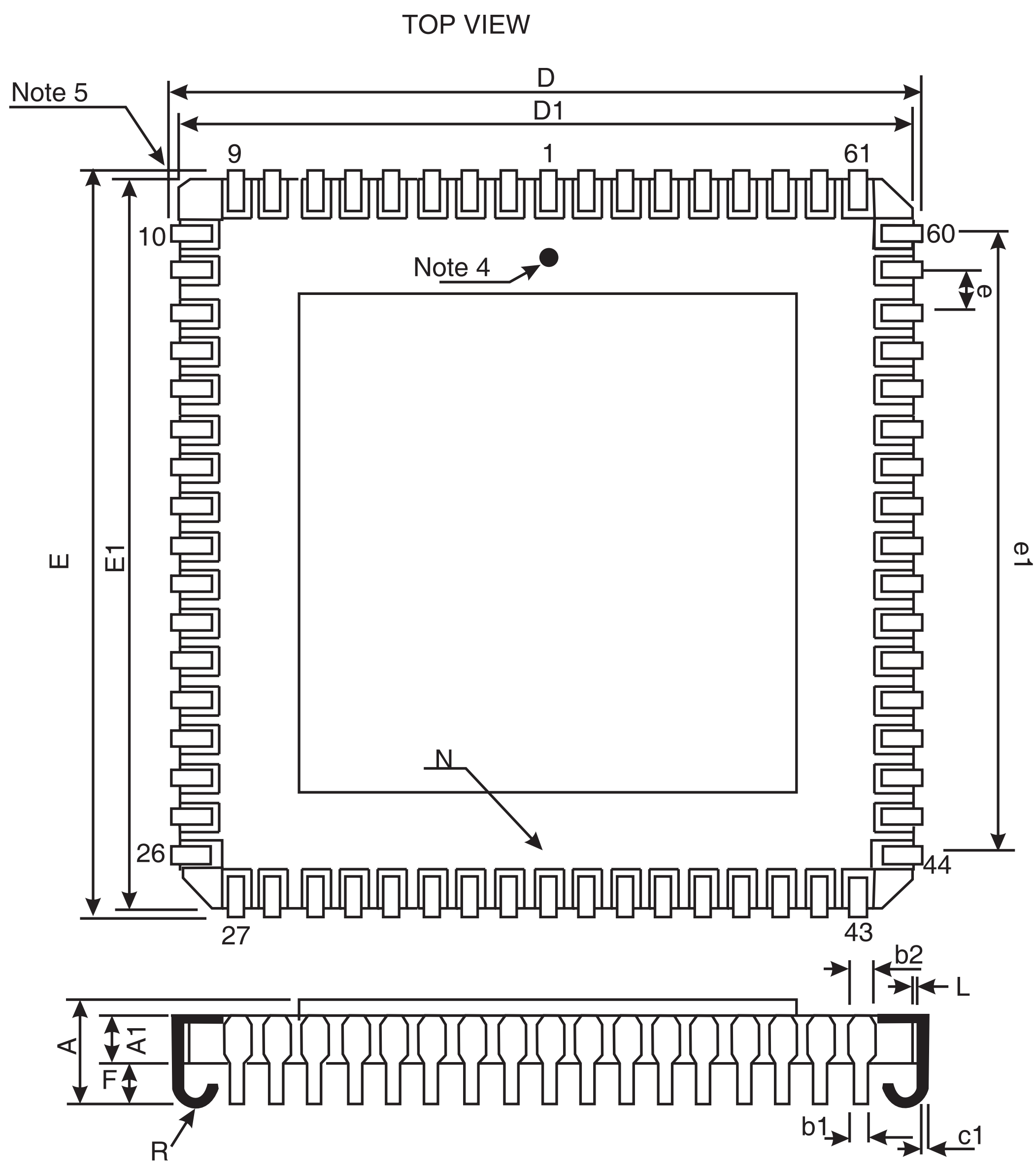
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 1000 Volts for all pins except DOUT, which has a minimum Critical Path Failure Voltage of 300 Volts. DOUT is a test pin only and does not affect functionality, operation or performance.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Ceramic Quad Flat Package J-BEND (CQFPJ-68) - 68 Terminals



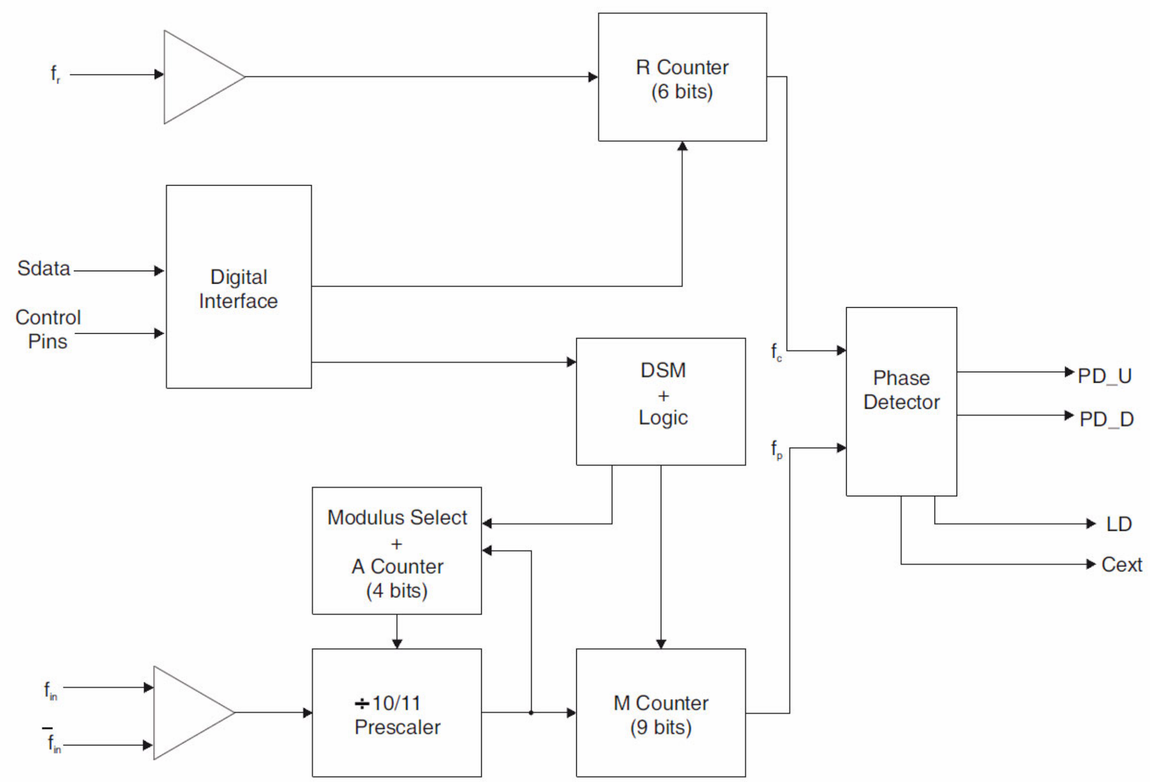
Symbols	Dimensions mm		Notes
	Min	Max	
A	3.124 TYPICAL		1
A1	1.82	2.24	
b1	0.432 TYPICAL		1
b2	0.762 TYPICAL		1
c1	0.152	0.254	1
D/E	24.89	25.4	

Symbols	Dimensions mm		Notes
	Min	Max	
D1/E1	23.82	24.44	
e	1.27 BSC		1, 2
e1	20.06	20.58	3
F	0.889 TYPICAL		1
L	0.508 TYPICAL		1
N	17 TERMINALS PER SIDE		3
R	0.762 TYPICAL		1, 6

NOTES:

1. Applies to all 68 terminals (17 per side).
2. 64 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to the package centrelines.
3. 4 places.
4. A terminal identification mark shall be located in the region of Pin 1 as shown. Terminal numbers shall increase counter clockwise when viewed as shown starting from the centre terminal (Pin 1).
5. Index corner: Terminal identification is specified by reference to the index corner as shown.
6. Radius.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

The table below describes each pin's assignment, type and standard, plus a brief description of its functionality.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
Top side					
1	R_0	Input	CMOS	Direct	R Counter, bit 0 (LSB).
2	R_1	Input	CMOS	Direct	R Counter, bit 1.
3	R_2	Input	CMOS	Direct	R Counter, bit 2.
4	R_3	Input	CMOS	Direct	R Counter, bit 3.
5	R_4	Input	CMOS	Direct	R Counter, bit 4.
6	R_5	Input	CMOS	Direct	R Counter, bit 5 (MSB).
7	K_0	Input	CMOS	Direct	K Counter, bit 0 (LSB).
8	K_1	Input	CMOS	Direct	K Counter, bit 1.
9	V_{SS}	Ground	-	-	V_{SS}
Left-hand side					
10	V_{DD}	Power	-	-	Digital core V_{DD} (Note 1).
11	K_2	Input	CMOS	Direct	K Counter, bit 2.
12	K_3	Input	CMOS	Direct	K Counter, bit 3.
13	K_4	Input	CMOS	Direct	K Counter, bit 4.
14	K_5	Input	CMOS	Direct	K Counter, bit 5.
15	K_6	Input	CMOS	Direct	K Counter, bit 6.
16	K_7	Input	CMOS	Direct	K Counter, bit 7.
17	K_8	Input	CMOS	Direct	K Counter, bit 8.
18	K_9	Input	CMOS	Direct	K Counter, bit 9.
19	K_{10}	Input	CMOS	Direct	K Counter, bit 10.
20	K_{11}	Input	CMOS	Direct	K Counter, bit 11.
21	K_{12}	Input	CMOS	Direct	K Counter, bit 12.
22	K_{13}	Input	CMOS	Direct	K Counter, bit 13.
23	K_{14}	Input	CMOS	Direct	K Counter, bit 14.
24	K_{15}	Input	CMOS	Direct	K Counter, bit 15.
25	K_{16}	Input	CMOS	Direct	K Counter, bit 16.
26	K_{17}	Input	CMOS	Direct	K Counter, bit 17 (MSB).
Bottom side					
27	V_{DD}	Power	-	-	Digital core V_{DD} (Note 1).
28	V_{SS}	Ground	-	-	V_{SS}
29	M_0	Input	CMOS	Direct	M Counter, bit 0 (LSB).

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
30	M_1	Input	CMOS	Direct	M Counter, bit 1.
31	M_2	Input	CMOS	Direct	M Counter, bit 2.
32	M_3	Input	CMOS	Direct	M Counter, bit 3.
33	M_4	Input	CMOS	Direct	M Counter, bit 4.
	S_WR			Serial	Serial load enable input. While S_WR is "low", Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR or HOP_WR rising edge.
34	M_5	Input	CMOS	Direct	M Counter, bit 5.
	SDATA			Serial	Binary serial data input. Input data entered MSB first.
35	M_6	Input	CMOS	Direct	M Counter, bit 6.
	SCLK			Serial	Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of SCLK.
36	M_7	Input	CMOS	Direct	M Counter, bit 7.
37	M_8	Input	CMOS	Direct	M Counter, bit 8 (MSB).
38	A_0	Input	CMOS	Direct	A Counter, bit 0 (LSB).
39	A_1	Input	CMOS	Direct	A Counter, bit 1.
	E_WR			Serial	Enhancement register write enable. While E_WR is "high", Sdata can be serially clocked into the enhancement register on the rising edge of SCLK.
40	A_2	Input	CMOS	Direct	A Counter, bit 2.
41	A_3	Input	CMOS	Direct	A Counter, bit 3 (MSB).
42	DIRECT	Input	CMOS	Both	Direct mode select. "high" enables direct mode, "low" enables serial mode.
43	$\overline{\text{PRE\_EN}}$	Input	CMOS	Direct	Prescaler enable, active "low". When "high", FIN bypasses the prescaler.
Right-hand side					
44	V_{DD}	Power	-	-	Digital core V_{DD} (Note 1).
45	V_{SS}	Ground	-	-	V_{SS}
46	V_{DD}	Power	-	-	Prescaler V_{DD} (Note 1).
47	FIN	Input	RF	Both	Prescaler input from the VCO. Maximum frequency 3.5GHz.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
48	$\overline{FIN}$	Input	RF	Both	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor directly to the ground plane.
49	V_{SS}	Ground	-	-	V_{SS}
50	CEXT	Output	CMOS (high resistance)	Both	Logical “NAND” of PD_U and PD_D terminated through an on-chip, 2kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Output	Open Drain	Both	Lock detect and open drain logical inversion of Cext. When the loop is in lock, LD is high impedance, otherwise LD is a logic “low” (“0”).
52	DOUT	Output	CMOS (low current)	Both	Data Out function, enabled in enhancement mode.
53	V_{DD}	Power	-	-	Output driver V_{DD} (Note 1).
54	V_{SS}	Ground	-	-	V_{SS}
55	PD_D	Output	CMOS	Both	PD_D pulses down when f_p leads f_c.
56	NC	-	-	-	Not Connected.
57	PD_U	Output	CMOS	Both	PD_U pulses down when f_c leads f_p.
58	V_{SS}	Ground	-	-	V_{SS}
59	V_{DD}	Power	-	-	Output driver V_{DD} (Note 1).
60	V_{DD}	Power	-	-	Phase detector V_{DD} (Note 1).
Top side					
61	V_{SS}	Ground	-	-	V_{SS}
62	FR	Input	CMOS	Both	Reference frequency input.
63	V_{DD}	Power	-	-	Reference V_{DD} (Note 1).
64	V_{DD}	Power	-	-	Digital core V_{DD} (Note 1).
65	$\overline{ENH}$	Input	CMOS	Both	Enhancement mode. When asserted “low” (“0”), enhancement register bit s are functional.
66	NC	-	-	-	Not Connected.
67	MS2_SEL	Input	CMOS	Both	MASH 1-1 select. “high” selects MASH 1-1 mode, “low” selects the MASH 1-1-1 mode.

Pin No.	Pin Name	Pin Type	Pin Standard	Valid Mode	Description
68	RAND_EN	Input	CMOS	Both	K register LSB toggle enable. “high” enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the Phase Detector comparison frequency / 2^{19}.

NOTES:
1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins (i.e. CMOS inputs of Group 1 below) have a 70kΩ pull-down resistor to ground.

The table below describes the pin groups to be tested.

Group No.	Type	Total No. of Pins	Pin Numbers
1	CMOS Input with Pull-down	42	1 to 8, 11 to 26, 29 to 43, 65, 67 and 68
2	CMOS Input	1	62 (FR)
3	RF Input	2	47 (FIN) and 48 ($\overline{FIN}$)
4	High Current CMOS Output	2	55 (PD_D) and 57 (PD_U)
5	Low Current CMOS Output	1	52 (DOUT)
6	High Resistance CMOS Output	1	50 (Cext)
7	Open Drain Output	1	51 (LD)
8	Power	9	10, 27, 44, 46, 53, 59, 60, 63 and 64
9	Ground	7	9, 28, 45, 49, 54, 58 and 61

1.10 FUNCTIONAL DESCRIPTION

1.10.1 Overview

The PE33632 consists of a prescaler, several counters, an 18-bit delta-sigma modulator (DSM) and a phase detector. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler outputs, respectively, by the integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The DSM modulates the A Counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via a three-wire serial bus. There are also various operational and test modes and a lock detect output.

1.10.2 Main Counter Chain

1.10.2.1 Normal Operating Mode

Setting the $\overline{PRE\_EN}$ control bit “low” enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (f_{in}) by an integer or fractional number derived from the values in the “M”, “A” Counters and the DSM input word K. The accumulator size is 18-bit, so the fractional value is fixed from the ratio $K/2^{18}$. There is an additional bit in the DSM that acts like an extra bit (19th bit). This bit is enabled by asserting the pin RAND_EN to “high”. Enabling this bit has the benefit of reducing the spurious levels. However, a small frequency offset will occur. This positive frequency offset is calculated with the following equation:

$$f_{offset} = (f_r/(R + 1))/2^{19} \qquad (1)$$

All of the following equations do not take into account this frequency offset. If this offset is important to a specific frequency plan, appropriate account needs to be taken.

In the normal mode, the output from the main counter chain (f_p) is related to the VCO frequency (f_{in}) by the following equation:

$$f_p = f_{in}/[10 \times (M + 1) + A + K/2^{18}] \qquad (2)$$

Where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, f_{in} is related to the reference frequency (f_r) by the following equation:

$$f_{in} = [10 \times (M + 1) + A + K/2^{18}] \times (f_r/(R + 1)) \qquad (3)$$

Where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that f_{in} must be greater than or equal to $90 \times (f_r / (R + 1))$ to obtain contiguous channels. The A Counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M Counter with the minimum allowed value of “1” will result in a minimum M Counter divide ratio of “2”.

1.10.2.2 Prescaler Bypass Mode

Setting the frequency control register bit $\overline{PRE\_EN}$ “high” allows f_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A Counter are powered down, and the input VCO frequency is divided by the M Counter directly. The following equation relates f_{in} to the reference frequency (f_r):

$$f_{in} = (M + 1) \times (f_r/(R + 1)) \qquad (4)$$

Where $1 \leq M \leq 511$

In this mode, neither the A Counter nor the K Counter is used and therefore only integer-N operation is possible.

1.10.3 Reference Counter Chain

The reference counter chain divides the reference frequency (f_r) down to the phase detector comparison frequency (f_c).

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r/(R + 1) \quad (5)$$

Where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (f_r) directly to the phase detector.

1.10.4 Register Programming

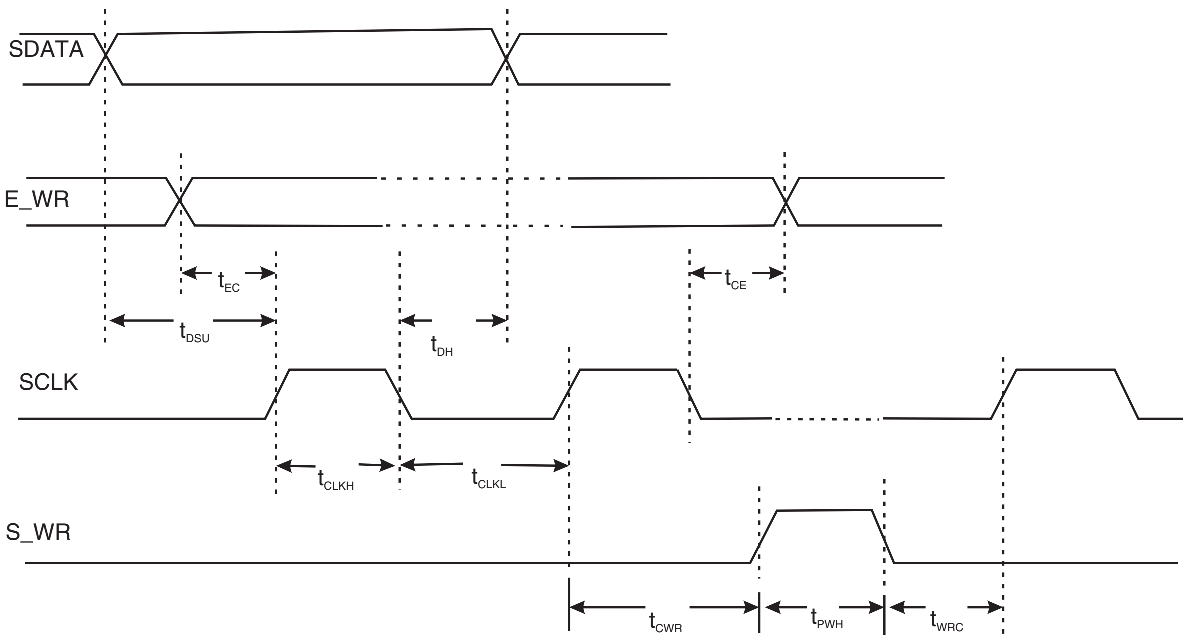
1.10.4.1 Serial Interface Mode

While the E_WR input is "low" and the S_WR input is "low", serial input data (SDATA input), B_0 to B_{20}, are clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The LSB is used as the address bit. When "0", the contents from the primary register are transferred to the secondary register on the rising edge of S_WR according to the timing chart shown below. When "1", data are transferred to the auxiliary register according to the same timing chart. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in the tables below.

While the E_WR input is "high" and the S_WR input is "low", serial input data (SDATA input), B_0 to B_7, are clocked serially to the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing chart shown below. After the falling edge of E_WR, the data provide control bits as shown in the tables below will have their bit functionality enabled by asserting the $\overline{ENH}$ input "low".

Serial Interface Timing Chart



1.10.4.2 Direct Interface Mode

Direct Interface Mode is selected by setting the DIRECT Input "high". Counter control bits are set directly at the pins as shown in the tables below.

Secondary Register Programming

Interface Mode	$\overline{ENH}$	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Address
Direct	1	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	X
Serial (1)	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	0

↑MSB (first in) LSB (last in)↑

Auxiliary Register Bit Programming

Interface Mode	$\overline{ENH}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Reserved		Address
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	X
Serial (1)	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	1

↑MSB (first in) LSB (last in) ↑

Enhancement Register Programming

Interface Mode	$\overline{ENH}$	Reserved	Reserved	FP Output	Power Down	Counter Load	MSEL Output	FC Output	LD Disable
Serial (2)	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

↑MSB (first in) LSB (last in) ↑

NOTES:

1. Serial data clocked serially on SCLK rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.
2. Serial data clocked serially on SCLK rising edge while E_WR "high" and captured in double buffer on E_WR falling edge.

1.10.4.3 Enhancement Register

The functions of the enhancement register bits are shown below with all bits active "high".

Bit Number	Bit Function	Description
0	Reserved	Reserve bit - program to 0.
1	Reserved	Reserve bit - program to 0.
2	FP Output	Drives the M Counter output onto the DOUT output.
3	Power Down	Power down of all functions except programming interface.
4	Counter Load	Immediate and continuous load of counter programming.
5	MSEL Output	Drives the internal dual modulus prescaler modulus select (MSEL) output onto the DOUT output.
6	FC Output	Drives the reference counter output onto the DOUT output.
7	LD Disable	Disables the LD pin for quieter operation.

1.10.5 Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference Counter (f_c). It has two outputs, namely PD_U and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

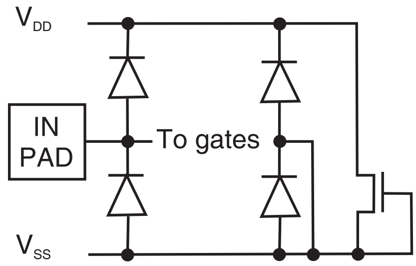
For the UP and DOWN mode, PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to $V_{DD}/2\pi$.

PD_U pulses cause an increase in VCO frequency and PD_D pulses cause a decrease in VCO frequency, for a positive Kv VCO.

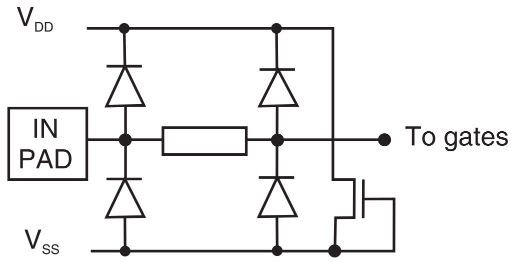
A "lock detect" output, LD, is also provided via the pin Cext. Cext is the logical "NAND" of PD_U and PD_D waveforms, which is driven through a serial 2kΩ resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_U and PD_D.

1.11 INPUT AND OUTPUT PROTECTION NETWORKS

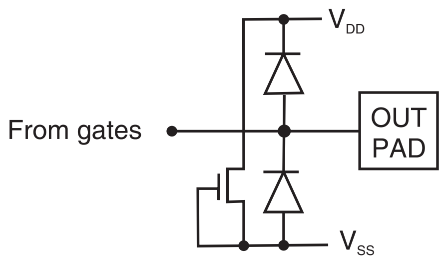
RF Inputs



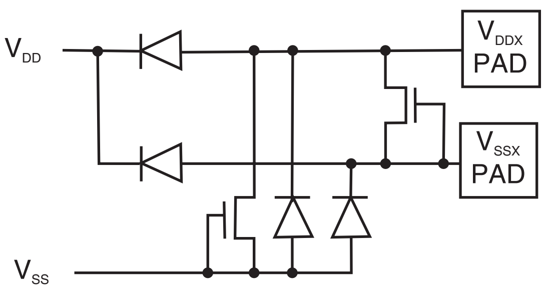
Other Inputs



Outputs



Supplies



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Input Clamp Voltage to V_{SS}	V_{ICL}	3022	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=200µA Note 1	-1.5	-	V
Input Clamp Voltage to V_{DD}	V_{ICH}	3022	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=-200µA Note 1	-	1.5	V
Shorts / Continuity Check	V_{SH}	-	Inputs: Pin Groups 1 to 3 Outputs: Pin Groups 4 to 7 V_{DD}=V_{SS}=0V I_{IN}=-200µA Note 1	-	200	mV
Standby Supply Current with Prescaler	I_{DDQ1}	3005	V_{DD}=3.45V, V_{SS}=0V Use pattern *mode*, stop at label *pdwn_sp* Note 3	-	500	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Dynamic Supply Current with Prescaler	$I_{DDOPENA}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	20	45	mA
Dynamic Supply Current without Prescaler	$I_{DDOPDIS}$	3005	V_{DD}=3.45V, V_{SS}=0V V_{IH}=3.45V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use pattern *main_pattern*@10MHz Loop from first to last vector Note 2	8	20	mA
Functional Test, Typical Voltage (Relaxed Limits)	-	3014	V_{DD}=3.3V, V_{SS}=0V V_{IH}=3.3V, V_{IL}=0V (Pin Groups 1 to 3) V_{OH}=1.8V, V_{OL}=1.3V I_{OL}=I_{OH}=0A (Pin Groups 4 to 6) I_{OL}=-0A (Pin Group 7) C_{LOAD}<62pF Use patterns *main_pattern* (between labels “main_st” and “end_u_d”) and *dsm_p1* @10MHz Note 4	Go/NoGo		-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Functional Test, Minimum Voltage (Specified Limits)	-	3014	V_{DD}=2.85V, V_{SS}=0V V_{IH}=1.98V, V_{IL}=870mV (Pin Groups 1 and 2) V_{IH}=2.85V, V_{IL}=0V (Pin Group 3) V_{OH}=2.465V, V_{OL}=385mV (Pin Groups 4 to 7) I_{OL}/ I_{OH}=-3 / +6mA (Pin Group 4) I_{OL}/ I_{OH}=±200µA (Pin Group 5) I_{OL}/ I_{OH}=±100µA (Pin Group 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use patterns *main_pattern* (between labels “main_st” and “end_u_d”) and *dsm_p1*@10MHz Note 4	Go/NoGo		-
Functional Test, Maximum Voltage (Specified Limits)	-	3014	V_{DD}=3.45V, V_{SS}=0V V_{IH}=2.4V, V_{IL}=1.05V (Pin Groups 1 and 2) V_{IH}=3.45V, V_{IL}=0V (Pin Group 3) V_{OH}=3.065V, V_{OL}=385mV (Pin Groups 4 to 7) I_{OL}/ I_{OH}=-3 / +6mA (Pin Group 4) I_{OL}/ I_{OH}=±200µA (Pin Group 5) I_{OL}/ I_{OH}=±100µA (Pin Group 6) I_{OL}=-1mA (Pin Group 7) C_{LOAD}<62pF Use patterns *main_pattern* (between labels “main_st” and “end_u_d”) and *dsm_p1*@10MHz Note 4	Go/NoGo		-
CMOS Input Voltage, Low Level (Minimum V_{DD})	V_{IL1}	-	Pin Groups 1 and 2 V_{DD}=2.85V, V_{SS}=0V Use pattern *main_pattern* Note 5	855	-	mV
CMOS Input Voltage, High Level (Minimum V_{DD})	V_{IH1}	-	Pin Groups 1 and 2 V_{DD}=2.85V, V_{SS}=0V Use pattern *main_pattern* Note 5	-	1995	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Output Voltage, Low Level (High Current Buffer at Minimum V_{DD})	V_{OL1_H}	3007	Pin Group 4 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-6mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Low Current Buffer at Minimum V_{DD})	V_{OL1_L}	3007	Pin Group 5 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-200µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Buffer with Serial Resistor at Minimum V_{DD})	V_{OL1_R}	3007	Pin Group 6 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-100µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Open Drain Buffer at Minimum V_{DD})	V_{OL1_OD}	3007	Pin Group 7 V_{DD}=2.85V, V_{SS}=0V I_{OL}=-1mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (High Current Buffer at Maximum V_{DD})	V_{OL2_H}	3007	Pin Group 4 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-6mA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Low Current Buffer at Maximum V_{DD})	V_{OL2_L}	3007	Pin Group 5 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-200µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Buffer with Serial Resistor at Maximum V_{DD})	V_{OL2_R}	3007	Pin Group 6 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-100µA Use pattern *main_pattern* Note 6	-	400	mV
CMOS Output Voltage, Low Level (Open Drain Buffer at Maximum V_{DD})	V_{OL2_OD}	3007	Pin Group 7 V_{DD}=3.45V, V_{SS}=0V I_{OL}=-1mA Use pattern *main_pattern* Note 6	-	400	mV

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Output Voltage, High Level (High Current Buffer at Minimum V_{DD})	V_{OH1_H}	3006	Pin Group 4 V_{DD}=2.85V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (Low Current Buffer at Minimum V_{DD})	V_{OH1_L}	3006	Pin Group 5 V_{DD}=2.85V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Minimum V_{DD})	V_{OH1_R}	3006	Pin Group 6 V_{DD}=2.85V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	2.25	-	V
CMOS Output Voltage, High Level (High Current Buffer at Maximum V_{DD})	V_{OH2_H}	3006	Pin Group 4 V_{DD}=3.45V, V_{SS}=0V I_{OH}=3mA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Low Current Buffer at Maximum V_{DD})	V_{OH2_L}	3006	Pin Group 5 V_{DD}=3.45V, V_{SS}=0V I_{OH}=200µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Output Voltage, High Level (Buffer with Serial Resistor at Maximum V_{DD})	V_{OH2_R}	3006	Pin Group 6 V_{DD}=3.45V, V_{SS}=0V I_{OH}=100µA Use pattern *main_pattern* Note 6	3.05	-	V
CMOS Input Leakage Current, Low Level (with Pull-down)	I_{IL_PD}	3009	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-250	250	nA
CMOS Input Leakage Current, Low Level	I_{IL}	3009	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	15	50	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CMOS Input Leakage Current, High Level (with Pull-down)	I_{IH_PD}	3010	Pin Group 1 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-75	-30	µA
CMOS Input Leakage Current, High Level	I_{IH}	3010	Pin Group 2 V_{DD}=3.45V V_{SS}=0V V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=3.45V	-50	-15	µA
High-Impedance Output Leakage Current, High Level	I_{OZH}	3021	Pin Group 7 V_{DD}=3.45V, V_{SS}=0V V_{OUT}=3.45V Use pattern *main_pattern*, stop at label “llzhh” Note 7	-	10	µA
Serial Clock Minimum Pulse Width High (Minimum V_{DD})	t_{CLKH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #35) to negedge SCLK (↓ #35) Use pattern *main_pattern* Note 10	-	30	ns
Serial Clock Minimum Pulse Width Low (Minimum V_{DD})	t_{CLKL1}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge SCLK (↓ #35) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	30	ns
Serial Data to Serial Clock Setup Time (Minimum V_{DD})	t_{DSU1}	3003	V_{DD}=2.85V, V_{SS}=0V From any edge of SDATA (#34) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	10	ns
Serial Data to Serial Clock Hold Time (Minimum V_{DD})	t_{DH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #35) to any edge of SDATA (#34) Use pattern *main_pattern* Note 10	-	10	ns
Serial Load Minimum Pulse Width High (Minimum V_{DD})	t_{PWH1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge S_WR (↑ #33) to negedge S_WR (↓ #33) Use pattern *main_pattern* Note 10	-	30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Serial Clock Rising Edge to Serial Load Rising Edge (Minimum V_{DD})	t_{CWR1}	3003	V_{DD}=2.85V, V_{SS}=0V From posedge SCLK (↑ #35) to posedge S_WR (↑ #33) Use pattern *main_pattern* Note 10	-	30	ns
Serial Clock Falling Edge to Enhancement Write Transition (Minimum V_{DD})	t_{CE1}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge SCLK (↓ #35) to any edge of E_WR (#39) Use pattern *main_pattern* Note 10	-	30	ns
Serial Load Falling Edge to Serial Clock Rising Edge (Minimum V_{DD})	t_{WRC1}	3003	V_{DD}=2.85V, V_{SS}=0V From negedge S_WR (↓ #33) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	30	ns
Enhancement Transition to Serial Clock Rising Edge (Minimum V_{DD})	t_{EC1}	3003	V_{DD}=2.85V, V_{SS}=0V From any edge of E_WR (#39) to posedge SCLK (↑ #35) Use pattern *main_pattern* Note 10	-	30	ns
Reference Clock Input Sensitivity	S_{FR}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=100MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Minimum f_{IN})	S_{FIN250}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=250MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 1 f_{IN})	S_{FIN300}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=300MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 2 f_{IN})	S_{FIN500}	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=500MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Prescaler Input Sensitivity (Medium 3 f_{IN})	$S_{FIN1000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=1000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 4 f_{IN})	$S_{FIN2000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=2000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Medium 5 f_{IN})	$S_{FIN3000}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=3000MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Maximum f_{IN})	$S_{FIN3250}$	-	V_{DD}=2.85V, V_{SS}=0V f_{IN}=3250MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	-5	dBm
Prescaler Input Sensitivity (Maximum f_{IN}, Typical V_{DD})	$S_{FIN3300}$	-	V_{DD}=3.15V, V_{SS}=0V f_{IN}=3300MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	0	dBm
Prescaler Input Sensitivity (> Maximum f_{IN}, Typical V_{DD})	$S_{FIN3550}$	-	V_{DD}=3.15V, V_{SS}=0V f_{IN}=3550MHz Use pattern *mode*, stop at label *mode_sp2* Note 11	-	0	dBm
Supply Current during Phase Noise Measurements, Typical Low V_{DD}	$I_{DDOPPN1}$	3005	V_{DD}=3V, V_{SS}=0V Note 13	5	80	mA
Supply Current during Phase Noise Measurements, Typical High V_{DD}	$I_{DDOPPN2}$	3005	V_{DD}=3.3V, V_{SS}=0V Note 13	5	80	mA
Phase Noise @ 100Hz Offset, Typical Low V_{DD}	$PN_{100}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-95	-70	dBc/Hz
Phase Noise @ 1kHz Offset, Typical Low V_{DD}	$PN_{1K}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-101	-81	dBc/Hz

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Phase Noise @ 10kHz Offset, Typical Low V_{DD}	$PN_{10K}1$	-	V_{DD}=3V, V_{SS}=0V Note 12	-107	-89	dBc/Hz
Phase Noise @ 100Hz Offset, Typical High V_{DD}	$PN_{100}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-95	-83	dBc/Hz
Phase Noise @ 1kHz Offset, Typical High V_{DD}	$PN_{1K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-101	-91	dBc/Hz
Phase Noise @ 10kHz Offset, Typical High V_{DD}	$PN_{10K}2$	-	V_{DD}=3.3V, V_{SS}=0V Note 12	-107	-96	dBc/Hz

NOTES:

1. Continuity test
   Comparison limit value, no measurement value recorded.
2. Dynamic current
   For measurement of the dynamic current, the pattern *main_pattern* is used and loops from first to last vector. Instantaneous current is measured and recorded (without any link to a specific vector number). total combined current for all V_{DD} pins. During the test, outputs are loaded with a capacitive load < 62 pF (tester load) but without active load. Comparators are disabled during this test.
3. Quiescent current
   During quiescent current test, outputs are loaded without active current load but with a capacitive load < 62 pF (tester load).
   The measurement is performed with the device having been initialised using pattern *mode*, stopped at end of vector labelled *pdwn_sp*. Total combined current of all V_{DD} pins.
   The measurement accuracy is better than 1µA.
4. Functional test
   During functional test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Output comparison is performed as “strobe comparison”. Strobe is placed 5% before the end of the period. For the open-drain output (i.e. pin 51, LD), comparison to the “High-Impedance” state may be masked for some vectors.
5. Input voltages
   During input voltage test, outputs are loaded with an active current load (when specified) and a capacitive load < 62 pF (tester load). For the active current load, the threshold load switching is set to $V_{DD}/2$.
   Measurements are performed using the test pattern *main_pattern* (between the labels “main_st” and “end_u_d”). The pattern is run with increasing or decreasing input voltage value of the pin under test until the first output fails. Remaining pins toggle with nominal input voltages.
   All the values are tested and recorded for each input.
   The measurement accuracy is better than 100mV.
6. Output voltages
   Measurements are performed using the test pattern *main_pattern*.
   The device is configured into correct state so that outputs are placed in high or low voltages. Output current is sourced/sinked and the resulting voltage is measured.
   All the values are tested and recorded for each output.
7. High impedance leakage current
   The device is configured into the correct state using the pattern *main_pattern* so that the pin under

test is in high impedance conditions (i.e. stop at label “llzhh”).
All the values are tested and recorded for each output.

8. Test patterns
Number of vectors (clock periods) for patterns used during test are:

- *main_pattern* 117065 vectors @ 1MHz (period = 1000ns) and 10MHz (period = 100ns)
- *dsm_p1* 1806 vectors @ 1MHz (period = 1000ns)
- *mode* 238 vectors @ 1 MHz (period = 1000ns)

9. Timing generators
All inputs use DATA mode timing generators (i.e. NRZ mode with zero delay) unless otherwise specified. The table below describes the timing generators. All patterns use the same set of timing

generators:

Timing Generator Number	Period (ns)	Pin Group	Delay (ns)	Width (ns)	Comp. Start (ns)	Comp. Stop (ns)	Format
0	1000	1 to 3	0	-	-	-	NRZ
		4 to 7	-	-	-	900	EDGE
1	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
2	1000	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	250	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
3	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
4	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
5	100	1 (except SCLK pin)	0	-	-	-	NRZ
		SCLK pin	25	-	-	-	NRZ
		2 and 3	10	-	-	-	NRZ
		4 to 7	-	-	-	95	EDGE
6	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
7	1000	1 and 2	0	-	-	-	NRZ
		3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
8	1000	1 (except S_WR, S_CLK and SDATA pins)	0	-	-	-	NRZ
		S_WR pin	600	-	-	-	NRZ
		SCLK pin	250	-	-	-	NRZ
		SDATA pin	100	-	-	-	NRZ
		2 and 4	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
10	1000	1	0	-	-	-	NRZ

Timing Generator Number	Period (ns)	Pin Group	Delay (ns)	Width (ns)	Comp. Start (ns)	Comp. Stop (ns)	Format
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
11	1000	1	0	-	-	-	NRZ
		2 and 3	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE
12		1 (except E_WR, S_CLK and SDATA pins)	0	-	-	-	NRZ
		E_WR pin	100	-	-	-	NRZ
		SCLK pin	150	-	-	-	NRZ
		SDATA pin	10	-	-	-	NRZ
		2 and 4	100	-	-	-	NRZ
		4 to 7	-	-	-	950	EDGE

10. Dynamic measurements
    Parameters shall be measured and recorded for each dynamic parameter to be tested. The measurement accuracy is better than 0.5ns.
11. RF measurements
    The frequency is set to the target frequency and output level at the FIN pin. The resulting output power is measured on DOUT.
    The measurement accuracy is better than 0.1dB.
12. Phase Noise measurements
    The Phase Noise measurements use a “Stack-and-Rack” solution. The parametric test settings are described hereafter:
    – f_{IN} =1920.4MHz
    – f_r = 100 MHz (0dBm)
    – f_c = 20MHz
    – Loop Bandwidth = 50kHz
    – Register M = 8
    – Register R = 4
    – Register A = 6
    – Register K = 5243
    – Modulus = 10

13. Operating current during Phase Noise measurement
    The parametric test settings are described in Note 12 above.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+85 (+0 -5)°C and T_{amb}=- 40(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements, except as follows:

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Standby Supply Current with Prescaler	I_{DDQ1}	3005	V_{DD}=3.45V, V_{SS}=0V Use pattern *mode*, stop at label *pdwn_sp*	-	1000	µA

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ± 3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current during Phase Noise Measurements, Typical High V_{DD}	$I_{DDOPPN2}$	±10%	5	80	mA
CMOS Output Voltage, Low Level (High Current Buffer at Minimum V_{DD})	V_{OL1_H}	±50	-	400	mV
CMOS Output Voltage, High Level (High Current Buffer at Minimum V_{DD})	V_{OH1_H}	±0.1	2.25	-	V
Prescaler Input Sensitivity (Medium 1 f_{IN})	S_{FIN300}	±2	-	-5	dBm

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

2.6.1 Electrical Test Conditions

Electrical test conditions shall be in accordance with the table below:

Characteristics	Symbols	Test Conditions	Units
Core Supply Voltage	V1	3.45 (+0 -5%)	V
Output Bias Voltage	V2	1.725 (±5%)	V
Input Voltage (Digital Inputs)	V_{IN}	0 to V1	V
Vector Length	t_O	1	µs

2.6.2 Environmental Test Conditions

Environmental test conditions shall be in accordance with the table below:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C

2.6.3 Burn-in Stimulus

The device shall be burned-in using "functional" vectors.

The Burn-in stimulus shall be made with vectors looping indefinitely. Each vector shall be made with thirteen (13) drivers. Each driver uses DATA mode, i.e. Non Return to Zero (NRZ) mode with toggling at the beginning of the vector. Looping this burn-in pattern exercises the PLL and PD_U/PD_D outputs toggle.

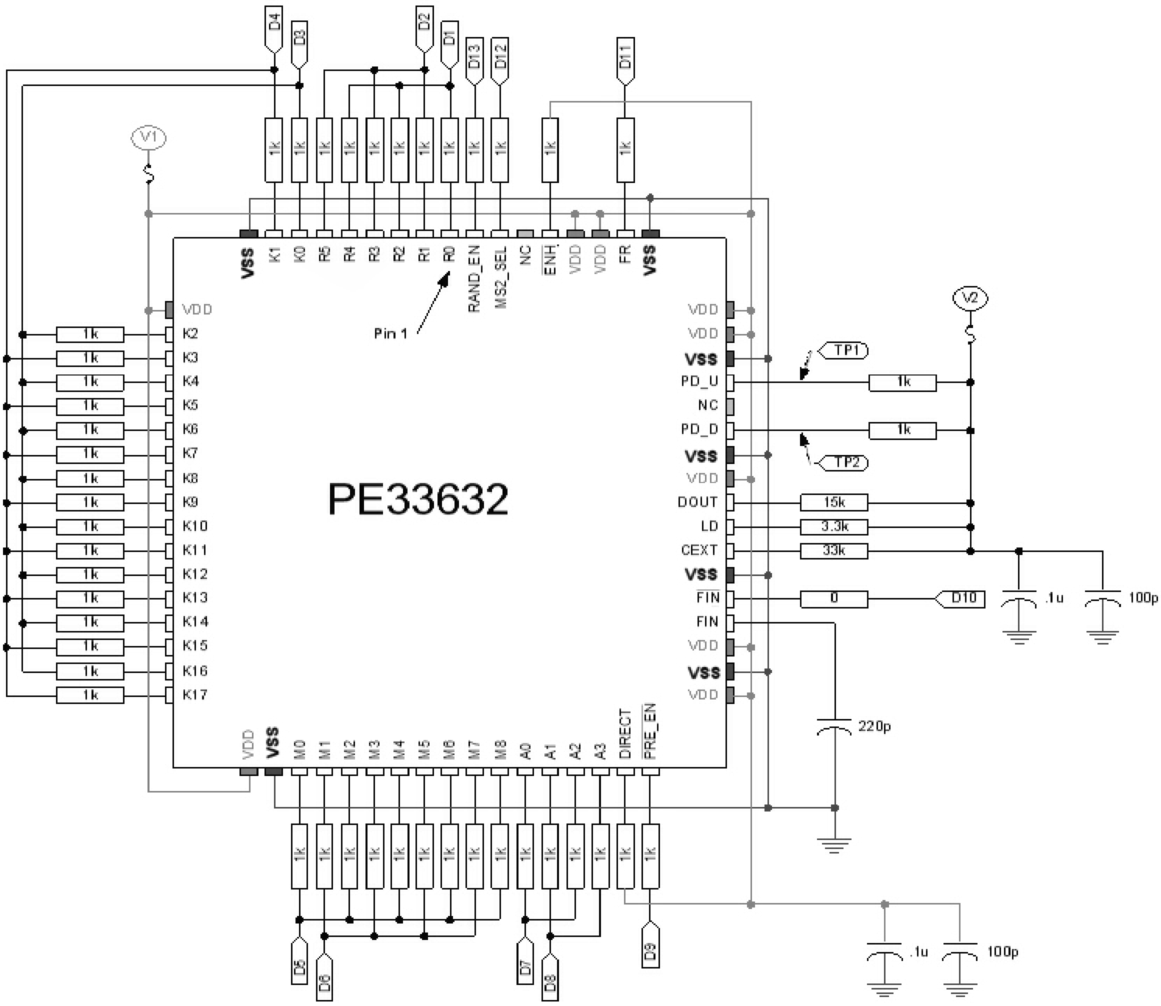
The device shall be set up in direct mode and counters loaded with checkerboard values in such a way that the PD_U and PD_D pins toggle alternately. The device shall go sequentially through seven (7) by-pass modes and sixteen (16) normal modes. Each mode includes eighty-six (86) vectors or forty-three (43) FIN clock cycles. FR (resp. MS2_SEL and RND_SEL) toggles every 11 (resp. 19 and 13) periods of FIN. There shall be 1978 vectors.

$\overline{PRE\_EN}$	A (hex)	K (hex)	M (hex)	R (hex)	FIN/FR ratio
By-pass mode					
1	-	-	155	2A	7.95
1	-	-	155	15	15.55
1	-	-	AA	2A	3.98
1	-	-	AA	15	7.77
1	-	-	1FF	15	23.27
1	-	-	1FF	3F	8
1	-	-	1FF	2A	11.91
Normal mode					
0	5	15555	155	15	155.7
0	5	15555	155	2A	79.66
0	5	15555	AA	15	77.97
0	5	15555	AA	2A	38.89
0	5	2AAAA	155	15	155.71

$\overline{\text{PRE\_EN}}$	A (hex)	K (hex)	M (hex)	R (hex)	FIN/FR ratio
0	5	2AAAA	155	2A	79.67
0	5	2AAAA	AA	15	77.98
0	5	2AAAA	AA	2A	39.9
0	A	15555	155	15	155.92
0	A	15555	155	2A	79.78
0	A	15555	AA	15	78.2
0	A	15555	AA	2A	40.01
0	A	2AAAA	155	15	155.94
0	A	2AAAA	155	2A	79.78
0	A	2AAAA	AA	15	78.21
0	A	2AAAA	AA	2A	40.02

2.6.4 Burn-in Schematic

The following schematic shows a suitable burn-in configuration for a single socket.



NOTES:

1. V1 is connected via a 500mA fuse.
2. V2 is connected via a 100mA fuse.
3. All resistors have a tolerance of ±1%. All capacitors have a tolerance of ±10%.
4. D1, D2, D3 etc. are Driver Numbers.
5. TP1 and TP2 are the Test Probes.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

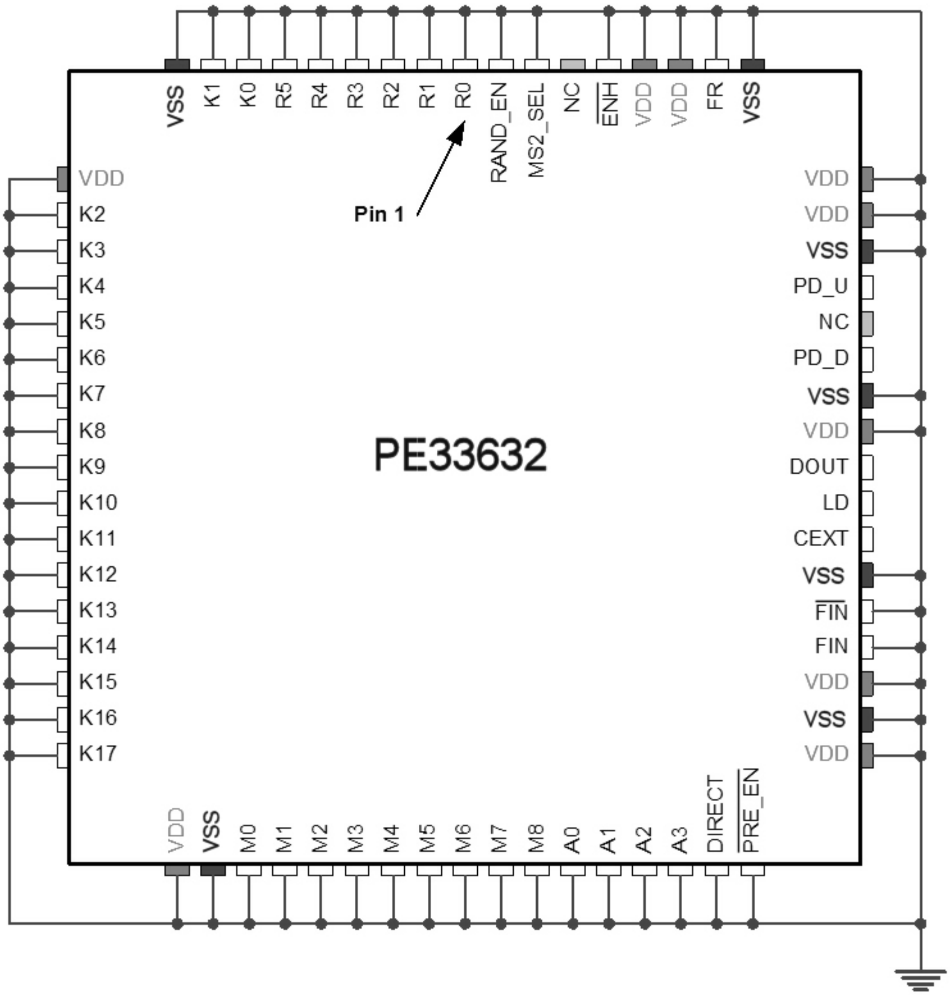
2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

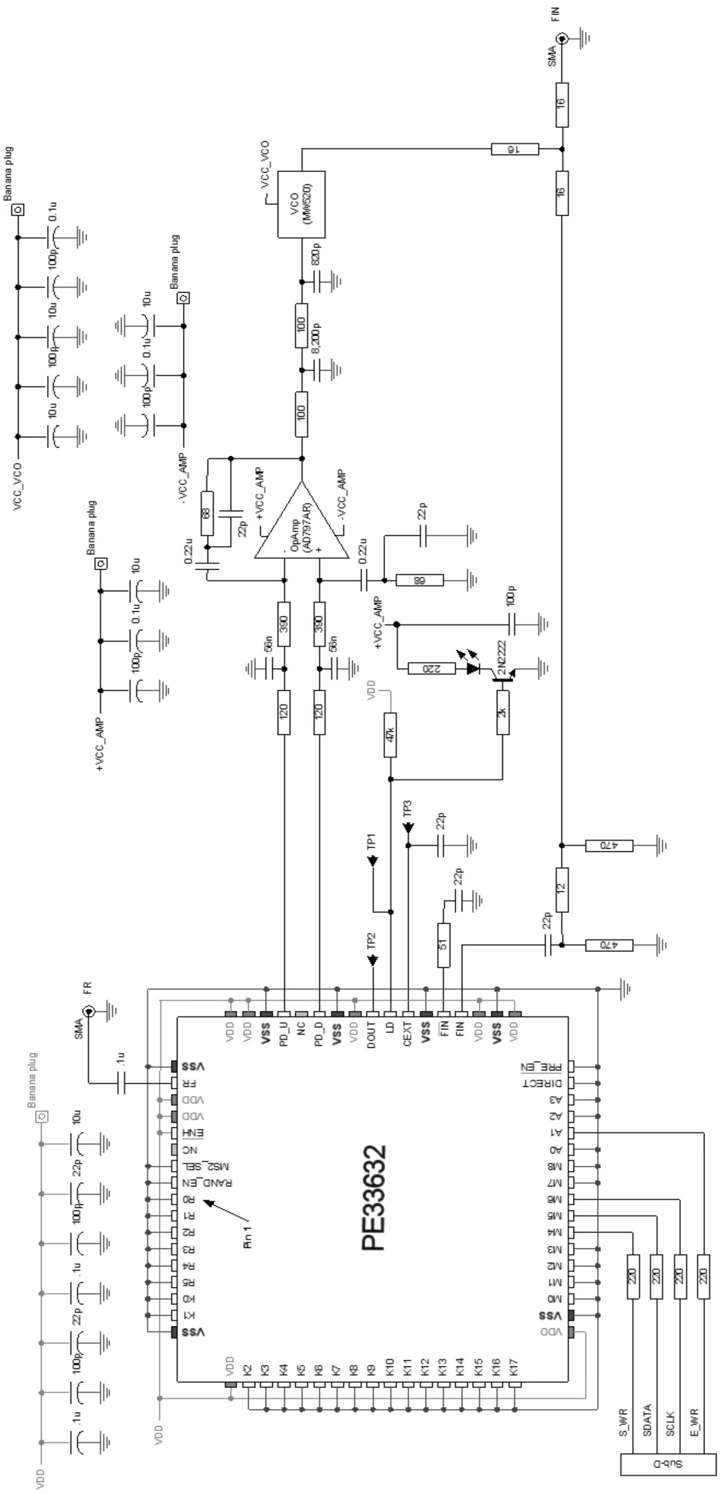
Bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

The following schematic shows a suitable test configuration for a single socket in unbiased condition (OFF).



The following schematic shows a suitable test configuration for a single socket in biased condition (ON).



NOTES:

1. V_{DD}=3.3V, V_{CC}_VCO=5±0.2V, +V_{CC}_AMP=5V and -V_{CC}+AMP=-5V.
2. f_r=40MHz, V_P=V_{SS} to V_{DD}.
3. f_{IN}=1920.4 MHz, V_P=V_{SS} to V_{DD}.
4. All resistors have a tolerance of ±1%. All capacitors have a tolerance of ±10%.
5. TP1, TP2 and TP3 are the Test Probes.
6. The table below shows how the device shall be serially programmed during Total Dose Radiation

Testing so the f_{IN} frequency is 1920.4 MHz.

Description	Value
R Counter	1
K Counter	5243
M Counter	8
A Counter	6
Reference Frequency	40 MHz

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Unless otherwise specified the measurements shall be performed at T_{amb}=22±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

APPENDIX 'A'

AGREED DEVIATIONS FOR PEREGRINE SEMICONDUCTOR EUROPE

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Wafer Lot Acceptance - Chart F2	The SEM inspection may be performed using the specified ESCC Method or, alternatively, may be carried out in accordance with the requirements of MIL-STD-883 Test Method 2018.
Deviations from Screening Tests - Chart F3	Following the PIND test, a Seal Test (Fine and Gross Leak) shall be performed in accordance with MIL-STD-883 Test Method 1014. An External Visual Inspection shall then be performed in accordance with ESCC Basic Specification No. 20500. Initial High and Low Temperatures Electrical Measurements may be performed prior to Burn-in at the option of the Manufacturer. The Check for Lot Failure shall only take into account any failures during Room Temperature Electrical Measurements. The number of failed components shall not exceed 5% of the components submitted to Burn-in. Room Temperature Electrical Measurements may be performed after Seal Test (Fine and Gross Leak).
Deviations from Qualification and Periodic Tests - Chart F4	Permanence of Marking shall not be performed on devices which have been laser marked.

Pages 1 to 10

RADIOGRAPHIC INSPECTION OF ELECTRONIC COMPONENTS

ESCC Basic Specification No. 20900

Issue 1	October 2002

Document Custodian: European Space Agency - see https://escies.org

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1. SCOPE

1.1 GENERAL

This specification describes the equipment and procedures to be used for the internal inspection of electronic components by radiographic means. When radiographic inspection is called for in an ESCC specification, it shall be used in conjunction with the relevant Ancillary ESCC Specification, numbered in the 209XXXX series, wherein the specific accept/reject criteria are prescribed (see Ancillary Specifications).

NOTES:

1. This type of inspection is not intended as an alternative to pre- and post- assembly visual examination.
2. For certain component types, the opacity of the construction materials may effectively prevent radiographic identification of certain types of defects or materials from some or all possible viewing angles. This factor should be considered in relation to the design of the component when the application of this test method is specified.

1.2 ALTERNATIVE STANDARDS

Where the configuration of a particular component is not in accordance with the examples shown in an Ancillary Specification, or where current in-house inspection drawings or standards (accepted in the PID) are to be used, it shall be the Manufacturer's responsibility to obtain the formal interpretation of the ESCC Executive, concerning any deviation.

2. EQUIPMENT AND MATERIALS

The equipment and materials for this test shall include:-

(a) Radiographic equipment with a sufficient energy level to penetrate the component. The focal distance shall be adequate to maintain a sharply defined image of an object with a major dimension of 0.0254mm.
(b) Radiographic film: Very fine grain industrial X-ray film grade, either single or double emulsion.
(c) Radiographic viewer: Capable of 0.0254mm resolution in major dimension.
(d) Holding fixtures: Capable of holding component in the required positions without interfering with the accuracy or ease of image interpretation of all specified defects, or damaging component.
(e) Film holder: A 1.6mm minimum lead-topped table or lead-backed film holder to prevent back-scatter of radiation.
(f) Penetrameters: Suitable penetrameters as quality references for the radiographs.

3. PROCEDURE

3.1 GENERAL

The X-ray exposure factors, voltage, milli-ampere setting and time settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details of defect features within the sensitivity limitations of the component.

The X-ray voltage shall be the lowest consistent with these requirements, but shall in no case exceed 150 kV.

3.2 MOUNTING

Components shall be mounted in the holding fixture so that they are not damaged or contaminated and are in the proper plane as specified. The components may be mounted in any type of fixture and masking with lead diaphragms or barium clay may be used to isolate multiple specimens. The fixtures or masking materials shall not block the view from the X-ray source to the film of any portion of the body of the component.

3.3 PENETRAMETERS

As a quality reference, penetrameters shall be employed in all radiographic testing. The penetrameter image shall meet the following requirements:-

(a) Penetrameter wires shall be visible on each radiograph.
(b) Penetrameters shall be selected to give a radiographic density within ±10% of the density of the area of interest of the component under inspection.
(c) Penetrameters shall be placed in diagonal corners on the source side of the film. The plane of the penetrameters shall be normal to the radiation beam. When 35mm film strip is used, the penetrameter shall be placed in a position normally occupied by a component and a penetrameter image shall be made (exposed) for every 50 components or every 40cm of film, whichever is more convenient.
(d) Distortion of any penetrameter shall not exceed 10%.
(e) The spacing between wires of a penetrameter shall not be distorted by more than 10%. The percentage of distortion as used in this specification is defined as follows:-

$$\frac{S0 - S1}{S0} \times 100, \text{ where}$$

S0= actual wire spacing.
S1= Wire spacing as it appears on the X-ray film.

A suitable range of penetrameters is shown in Figure 1 and Table 1. Equivalent penetrameters, to give an image of similar quality, may be used.

3.4 POSITIONING OF COMPONENTS

Components shall be radiographed in consecutive serial number order, when applicable. When a component is missing, the blank space shall contain either the serial number or an X-ray opaque object to assist in the accurate correlation of X-ray data.

Components shall be aligned in rows, starting with the lowest serial number in the top left-hand corner, continuing to the right, then forming a second row from left to right and so on. A clearance distance on the processed film of not less than 6.0mm shall be provided between the outer perimeters of all components, components and penetrameters, and components or penetrameters and the edge of the film.

3.5 VIEWS

The directions of radiographic exposure shall be as prescribed for the component in the relevant Ancillary Specification.

3.6 FILM AND MARKING

The radiograph film shall be in film holder backed with a minimum 1.6mm of lead, or the holder shall be placed on a lead-topped table. The film shall be identified such that the following information may be referenced to the radiograph:-

(a) Component Manufacturer's name or code.
(b) Component type or part number.
(c) Production lot number or date code or inspection lot number.
(d) Radiographic film view number and date.
(e) Component serial numbers or cross-reference numbers, when applicable.
(f) X-ray laboratory identification.

3.7 NON-FILM TECHNIQUES

When specified, the use of non-film techniques is permitted if permanent records are not required. The equipment shall be capable of producing results of equal quality when compared with film techniques. All requirements of this specification shall be complied with, except those pertaining to the actual film.

3.8 TESTS

The X-ray exposure factor shall be selected to achieve resolution of 0.0254mm major dimension, and a film density between 1 and 2 in the area of interest of the image.

Radiographs shall be made for each specified view.

3.9 PROCESSING

The radiographic film Manufacturer's recommended procedure shall be used to develop the exposed film and the film shall be processed so that it is free of processing defects such as fingerprints, scratches, fogging, chemical spots, blemishes, etc.

3.10 OPERATING PERSONNEL

The radiographic examination shall be carried out by the component Manufacturer. Personnel who will perform radiographic inspection shall be properly trained in the radiographic procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards.

4. INTERPRETATION OF RADIOGRAPHS

Utilising the equipment specified herein, radiographs shall be inspected to determine that each component conforms to the applicable standard and the relevant criteria. Defective components shall be rejected. Interpretation of the radiograph shall be made under low light level conditions without glare on the radiograph viewing surface. The radiographs shall be examined on a suitable illuminator with variable intensity or on a viewer suitable for radiographic inspection on projection-type viewing equipment. The radiograph shall be viewed at a magnification between x6 and x25. Viewing masks may be used when necessary.

5. REPORTS AND RECORDS

5.1 REPORTS OF INSPECTION

When specified in the appropriate ESCC specification, the manufacturer shall furnish inspection reports with each component delivery lot. The report shall describe the results of the radiographic inspection and list the following:-

(a) Purchase Order number or equivalent identification.
(b) Component type or part number.

(c) Date code.
(d) Quantity inspected, with serial numbers, when applicable.
(e) Quantity rejected, with serial numbers, when applicable
(f) Date of inspection.

For each rejected component, the type or part number, serial number when applicable and cause for rejection shall be listed.

5.2 RADIOGRAPHS

When specified in the appropriate ESCC specification, the Manufacturer shall furnish photographic reproductions of each radiograph relevant to a component delivery lot.

5.3 RETENTION OF REPORT AND RADIOGRAPHS

The Manufacturer shall retain one set of the radiographs and a copy of the inspection report relevant to a component delivery lot for a minimum period of 3 years.

6. EXAMINATION AND ACCEPTANCE CRITERIA

The detailed examination/inspection requirements for a component and the accept/reject criteria shall be as specified in the relevant Ancillary Specification.

7. ANCILLARY SPECIFICATIONS

The following Ancillary Specifications in the ESCC 209XXXX series have been issued for use in conjunction with this specification:-

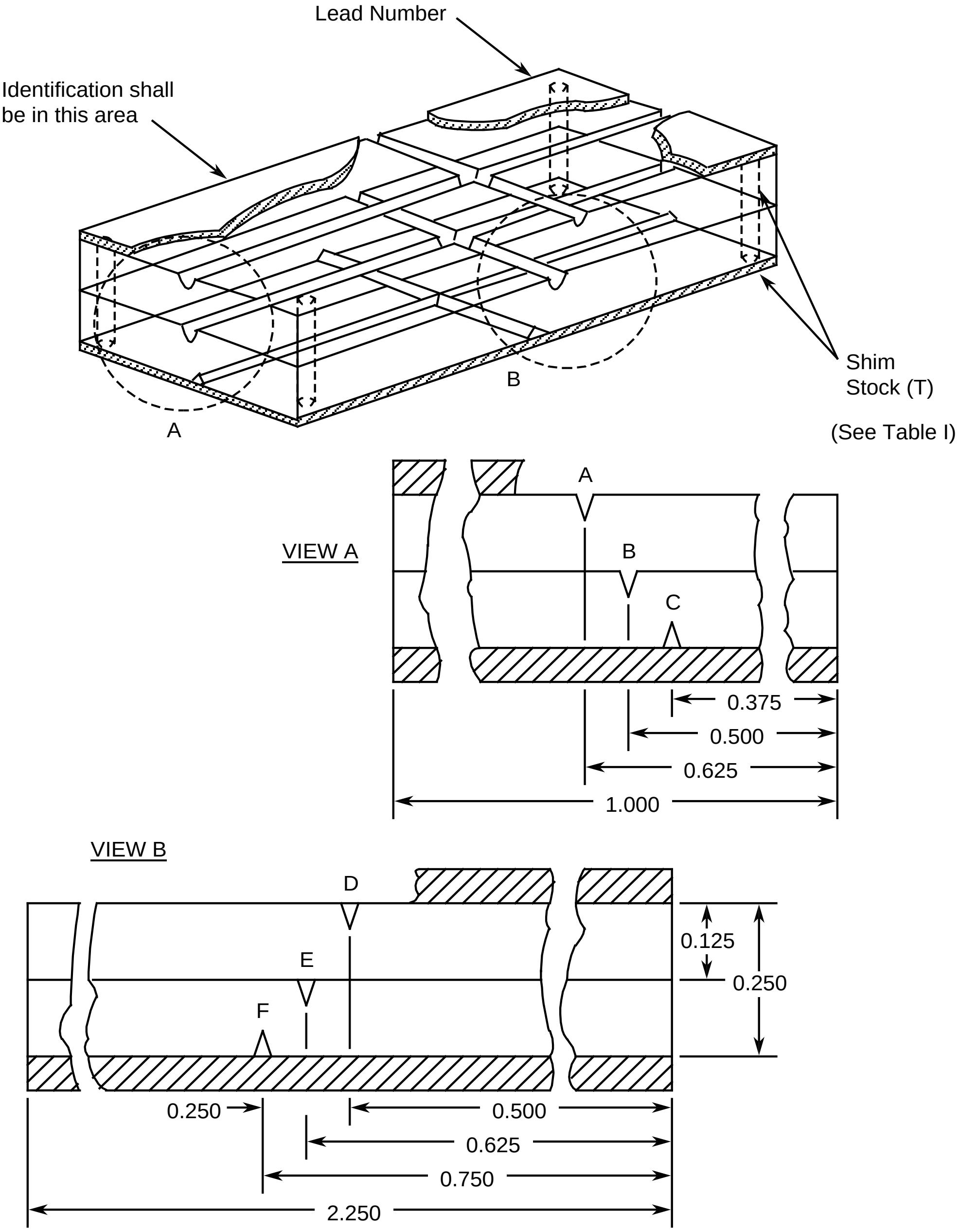
ESCC No. 2093000, Radiographic Inspection of Capacitors.
ESCC No. 2093501, Radiographic Inspection of Quartz Crystal Units.
ESCC No. 2093502, Radiographic Inspection of Surface Acoustic Wave (SAW) Devices.
ESCC No. 2094000, Radiographic Inspection of Resistors.
ESCC No. 2095000, Radiographic Inspection of Discrete Semiconductors (1).
ESCC No. 2099000, Radiographic Inspection of Integrated Circuits.

NOTES:

1. For Discrete Mircrowave Semiconductor Devices (ESCC Generic Specification No. 5010), no individual ancillary specification for Radiographic Inspection exists. ESCC No. 2095000 should be used to the extent applicable.

8. FIGURES

8.1 FIGURE 1: PENETRAMETER



NOTES:

1. All dimensions are in inches.
2. Except for grooves and wires, dimensional tolerances shall be ± 0.005 inch.
3. For the purpose of this specification, metric dimensions shall be in accordance with the conversion detailed in Table 2.

9. TABLES

9.1 TABLE 1: TYPES OF PENETRAMETER

Penetrameter Number	Shim Stock Thickness T (Inches)	Wire Size (Inches)					
		A	B	C	D	E	F
1	0.005	0.002	0.001	0.0005	0.0005	0.001	0.002
2	0.007	0.002	0.001	0.0005	0.0005	0.001	0.002
3	0.010	0.003	0.002	0.001	0.001	0.002	0.003
4	0.015	0.003	.002	0.001	0.001	0.002	0.003
5	0.025	0.005	0.003	0.002	0.002	0.003	0.005
6	0.035	0.005	0.003	0.002	0.002	0.003	0.005

NOTES:

1. Shim stock shall be made of steel.
2. Wires shall be made of tungsten, except for penetrameters used with relays, in which case, copper wires shall be utilised.
3. Groove details are not critical. Wire shall be flush or below plastic and located as shown.
4. Centre sections shall be made of clear plastic of low X-ray density.
5. All materials shall be bonded with clear-type cement.
6. Plastic cement shall have a low X-ray density.
7. Dimensions, except grooves and wires, shall be ± 0.005 inch.
8. In addition to bonding the penetrameter sections, assemblies may be fastened within 0.250 inch of each corner; bottom face to be flush.
9. Fastener shall not interfere with the end-use of the penetrameter.
10. For the purpose of this specification, metric dimensions shall be in accordance with the conversion detailed in Table 2.

9.2 TABLE 2: METRIC CONVERSION

inches	mm	inches	microns
1.000	25.40	0.035	889
0.750	19.05	0.025	635
0.625	15.88	0.015	381
0.500	12.70	0.010	254
0.375	9.52	0.007	178
0.250	6.35	0.005	127
0.125	3.17	0.003	77
		0.002	55
		0.001	25
		0.0005	13

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Pages 1 to 10

RADIOGRAPHIC INSPECTION OF

INTEGRATED CIRCUITS

ESA/SCC Basic Specification No. 2099000

SCC

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	September 1994		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.

TABLE OF CONTENTS

1. SCOPE

This specification, to be read in conjunction with ESA/SCC Basic Specification No. 20900, Radiographic Inspection, contains additional requirements to be applied to Integrated Circuits.

2. GENERAL REQUIREMENTS

2.1 APPLICABILITY

The following criteria may not be varied or modified after commencement of any inspection stage. Any ambiguity or proposed deviation shall be referred to the Qualifying Space Agency for resolution and approval.

2.2 PROCEDURE

All items shall be examined in such a manner that a minimum of handling and movement of the components is involved.

3. X-RAY PHOTOGRAPHS

Each component shall be radiographed once along one axis.

4. DETAILED REQUIREMENTS

4.1 REJECT CRITERIA

The individual device examination shall include, but not be limited to, inspection for foreign particles, build-up of bonding material, placement of lead wires, bond of lead to semiconductor element and lead to terminal post, and mounting of semiconductor element. Any device for which the radiograph reveals any of the following defects shall be rejected.

4.2 PRESENCE OF EXTRANEOUS MATTER

Extraneous matter (foreign particles) shall include, but not be limited to:-

(a) Any foreign particle, loose or attached, greater than 0.0254mm (see Figure I), or of any lesser size which is sufficient to bridge non-connected conducting elements of the device.

(b) Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see Figure I).

(c) Any burr on a post (header lead) greater than 0.08mm in its major dimension or of such configuration that it may break away.

(d) Excessive semiconductor element bonding material build-up.

(1) A semiconductor element shall be mounted and bonded so that it is not tilted more than 10 degrees from the normal mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor element and touches the side of the semiconductor element shall not accumulate to a thickness greater than that of the semiconductor element (see Figures II and III). Where the bonding agent is built up, but is not touching the semiconductor element, the build-up shall not be greater than twice the thickness of the semiconductor element.

(2) There shall be no visible extraneous material of 0.0254mm or larger in the major dimension. Loose bonding material will be considered extraneous material. Excessive (but not loose) bonding material will not be considered extraneous unless it fails to meet the requirements of Paragraph 4.2(d) (1) or the accumulation of bonding material is in the pedestal form (see Figures II and III).

(e) Gold flaking on the header or posts or anywhere inside the case.

(f) Extraneous ball bonds anywhere inside the case, except for attached residue when rebonding is allowed.

4.3 UNACCEPTABLE CONSTRUCTION

In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit the following defects shall be rejected:-

(a) Voids - When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see Figure I).

(1) Contact area voids in excess of one-half of the total contact area.

(2) A single void equal to the length of the semiconductor element.

(3) A single void that traverses the width of the semiconductor element.

(b) Wires present other than those connecting specific areas of the semiconductor element to the external leads. Device designs calling for the use of such wires, including jumping wires, are acceptable (see Figure I).

(c) Cracks, splits or chips of the electrical elements.

(d) Defective seal - Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75%. Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is attached to the parent material and does not exhibit a tear-drop confuguration (i.e. where the base support's least dimension is smaller than the dimension it is supposed to support).

(e) Inadequate clearance - Acceptable devices shall have adequate internal clearance to ensure that the elements cannot contact one another or the case. No cross-overs shall be allowed. Depending upon the case type, devices shall be rejected for the following conditions:-

(1) Flat pack and dual-in-line (see Figure IV).

(a) Any lead wire that appears to touch or cross another lead wire or bond (Y plan only).

(b) Any lead wire that deviates from a straight line from bond to external lead and appears to be within 0.05mm of another wire or bond (Y plane only).

(c) Lead wires that do not deviate from a straight line from bond to external lead and appear to touch antoher wire or bond (Y plane only).

(d) Any lead wire that touches or comes within 0.05mm of the case or external lead to which it is not attached (X and Y planes).

(e) Any bond that is less than 0.025mm (excluding bonds connected by a common conductor) from another bond (Y plane only).

(f) Any wire making a straight line run from die bonding pad to package post that has no arc.

(2) Round Transistor Type (see Figure V).

(a) Any lead wire that touches or comes within 0.05mm of the case or external lead to which it is not attached (X and Y planes).

(b) Lead wires that sag below an imaginary plane across the top of the bond (X plane only).

(c) Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

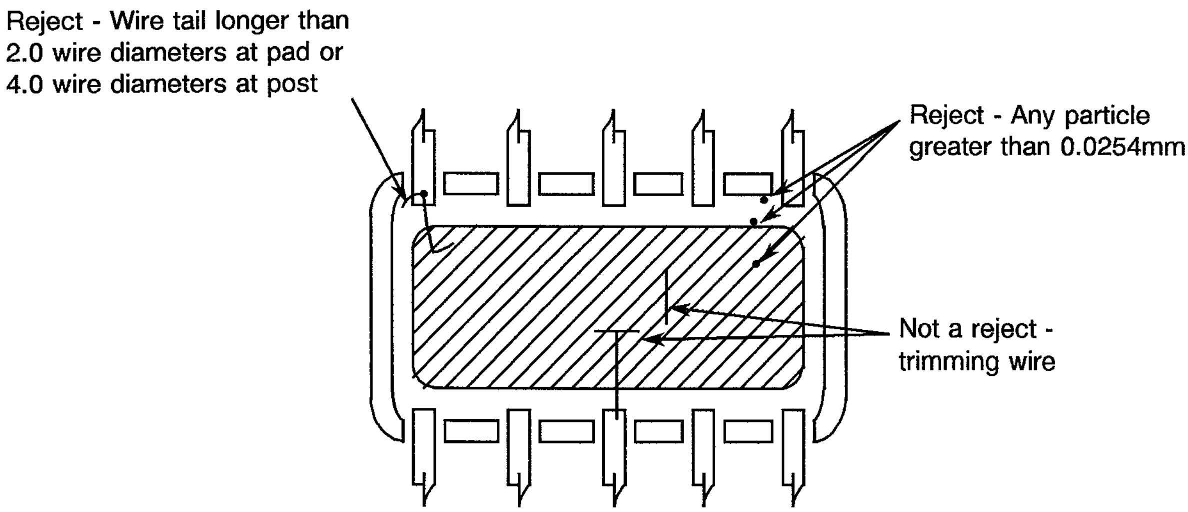
(d) Any lead wire that deviates from a straight line from bond to external lead and appears to touch or be within 0.05mm of another wire or bond (Y plane only).

(e) Any bond that is less than 0.025mm (excluding bonds connected by a common conductor) from another bond (Y plane only).

(f) Any wire making a straight line run from die bonding pad to package post that has no arc.

FIGURE I - PARTICLE LOCATIONS, PIGTAILS, TRIMMING WIRES AND VOIDS

(a) Particle Locations, Pigtails & Trimming Wires



(b) Voids

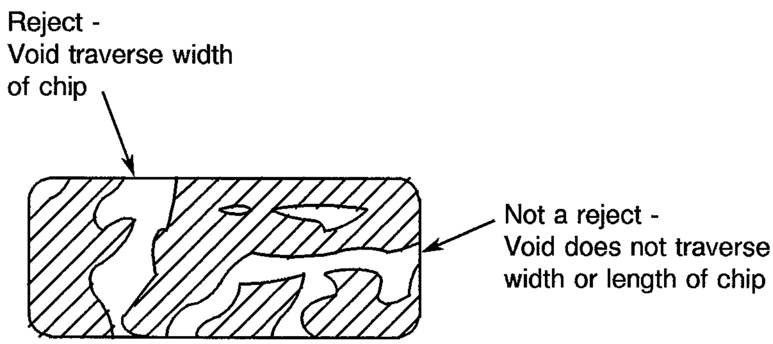


FIGURE II - ACCEPTABLE AND UNACCEPTABLE BONDING MATERIAL BUILD-UP

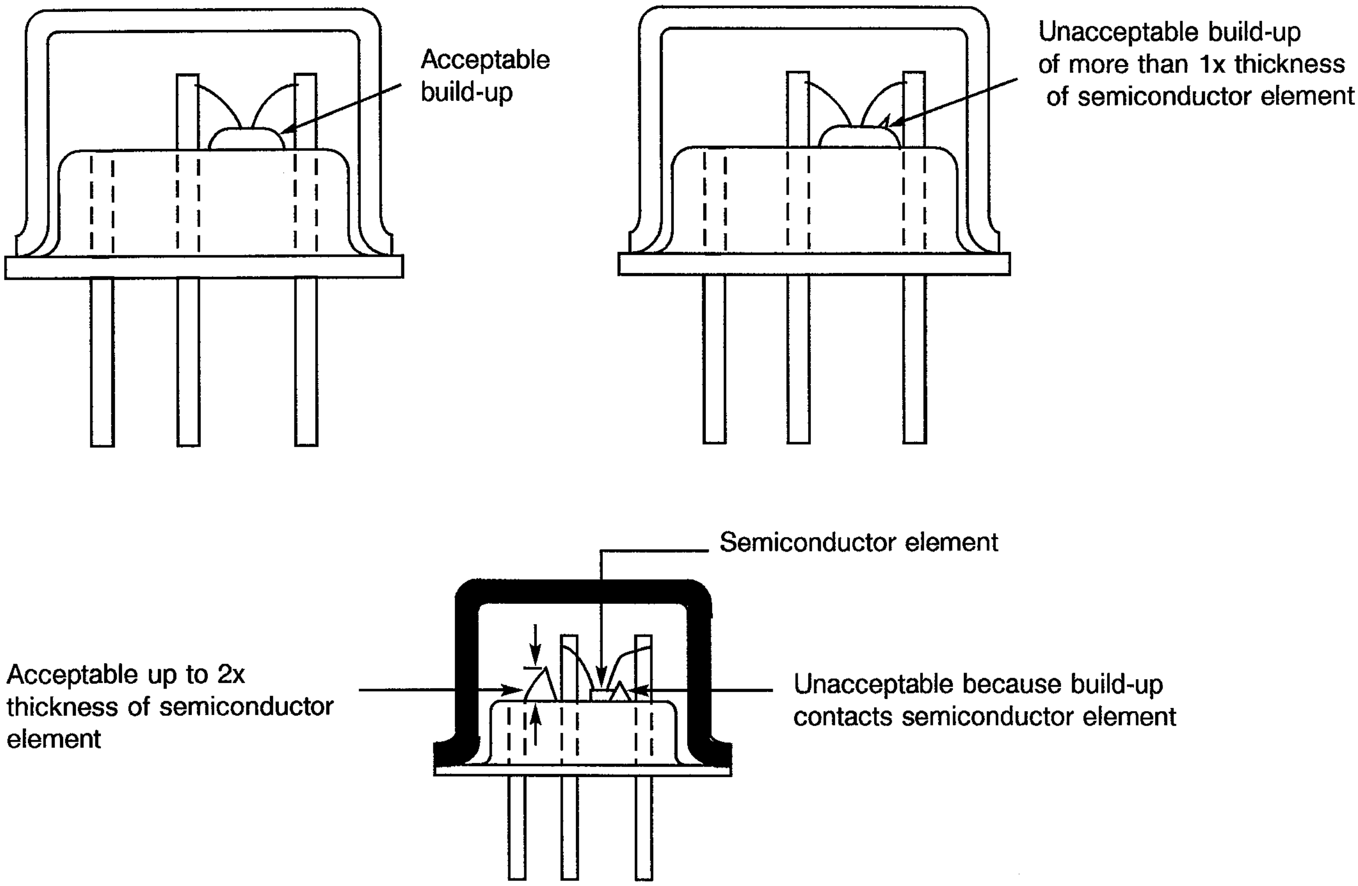


FIGURE III - EXTRANEOUS BONDING MATERIAL BUILD-UP

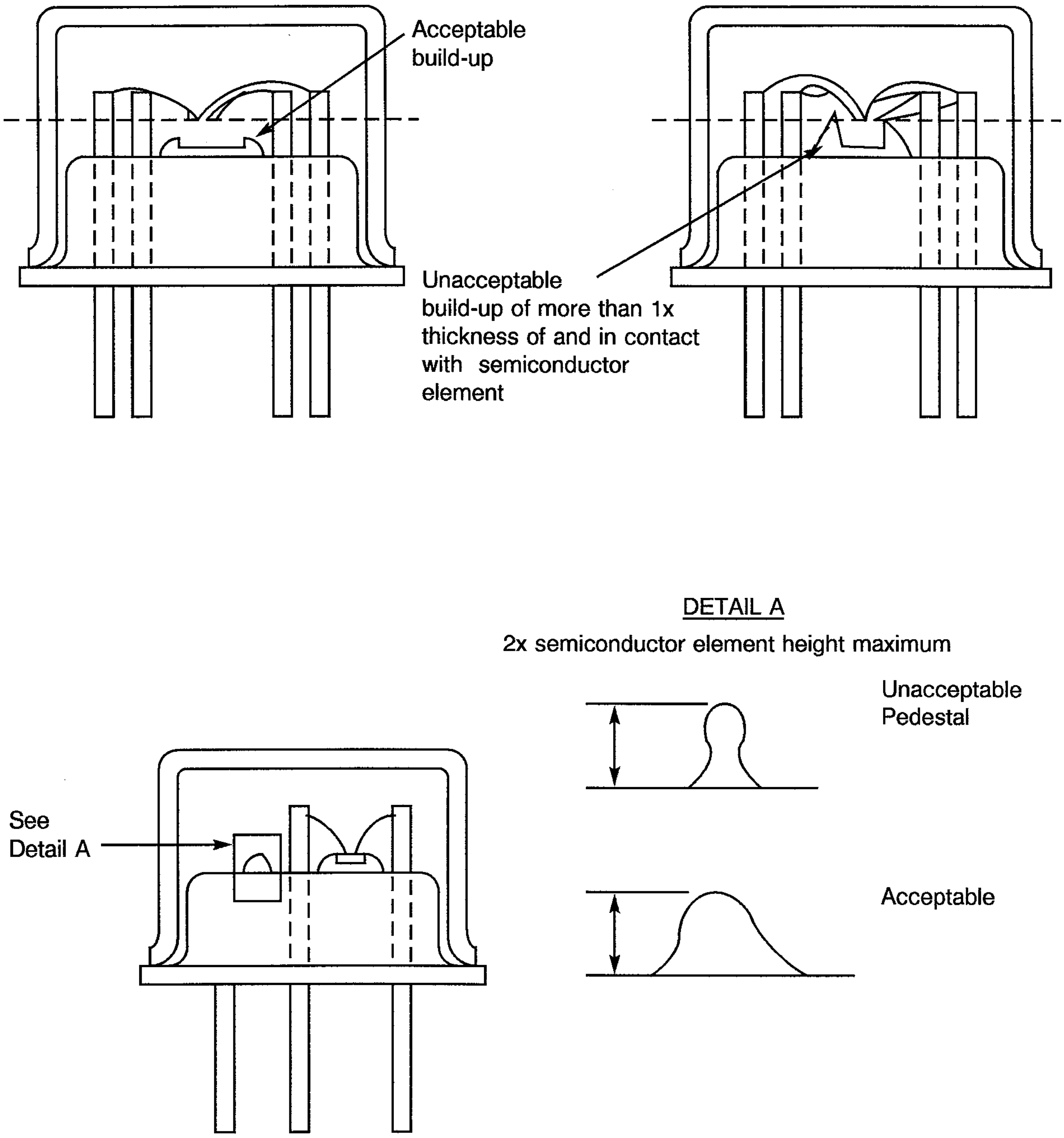


FIGURE IV - CLEARANCE IN DUAL-IN-LINE OR FLAT PACK TYPE DEVICE

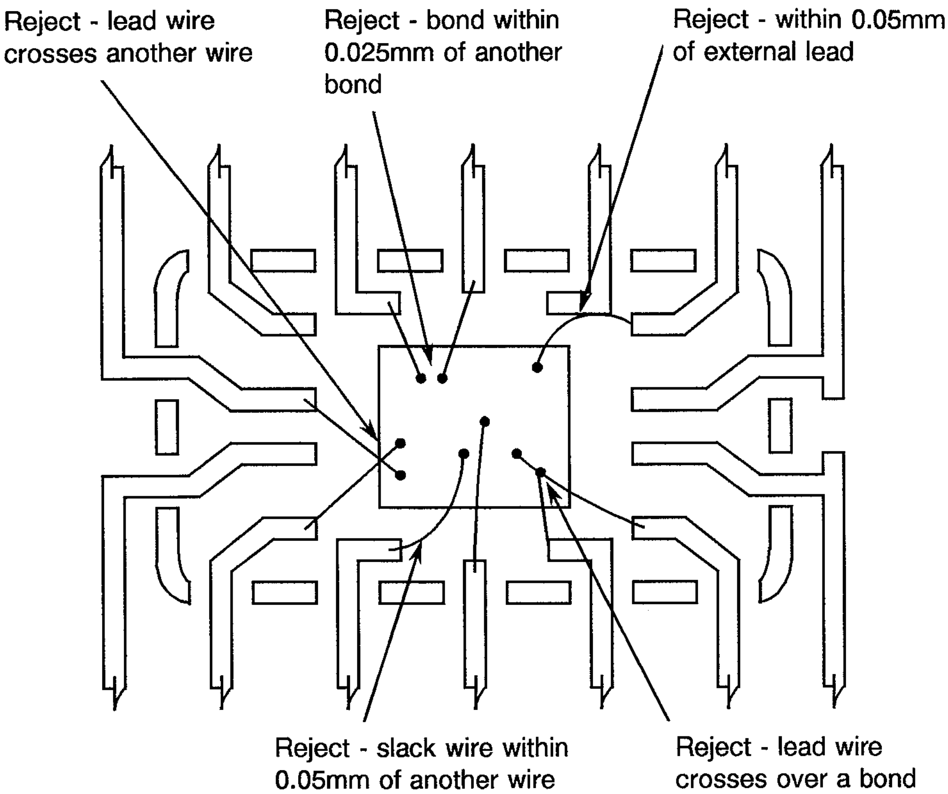
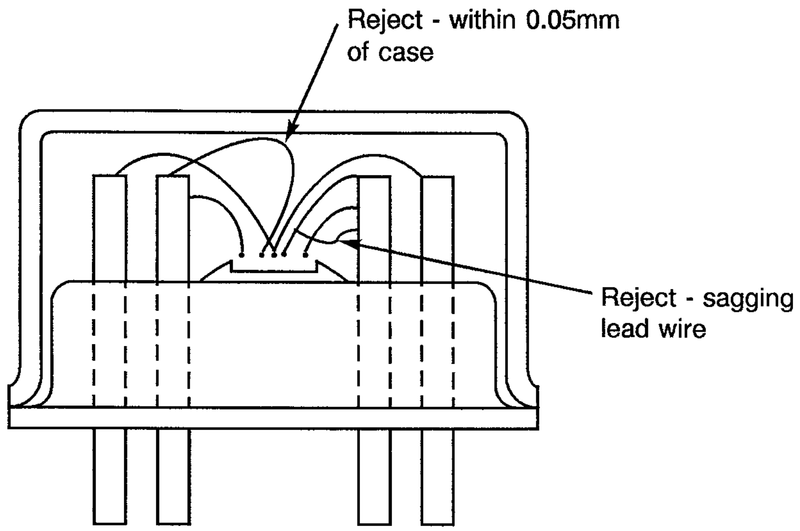


FIGURE V - CLEARANCE IN ROUND TRANSISTOR TYPE DEVICE

(a) X-AXIS CLEARANCE



(b) Y-AXIS CLEARANCE