

### DOCUMENT CHANGE REQUEST

517 DCR number Changes required for: General Originator: S Jeffery - ESCC Date: 2009/05/06 Organisation: ESA/ESTEC Date sent: 2009/05/06 Status: IMPLEMENTED Title: Transistors Silicon Switching PNP, based on type 2N3467 Number: 2 5208/009 Issue: Other documents affected: Page: See attachment Paragraph: See attachment Original wording: Proposed wording: Update the Maximum Ratings table (see the attachment for details) so that this detail spec is clear, complete and the content and format is in-line with other detail specifications for similar Part Types. Justification: Improve the content and clarity of the spec. Attachments: 5208009\_Issue\_3\_-\_Draft\_A.pdf, null Modifications: N/A Approval signature: 12. (c f(an-) Date signed: 2009-05-06

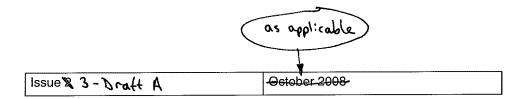


Pages 1 to 13

# TRANSISTORS, SWITCHING, PNP

# **BASED ON TYPE 2N3467**

ESCC Detail Specification No. 5208/009







ESCC Detail Specification No. 5208/009

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# **DOCUMENTATION CHANGE NOTICE**

(Refer to https://escies.org for ESCC DCR content)

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**ISSUE 2** 

At Trase = +25°C

| Characteristics             | Symbols            | Maximum Ratings | Unit | Remarks                           |
|-----------------------------|--------------------|-----------------|------|-----------------------------------|
| Collector-Base Voltage      | V <sub>CBO</sub>   | -40             | V    | Over entire                       |
| Collector-Emitter Voltage   | V <sub>CEO</sub>   | -40             | V    | operating<br>temperature<br>range |
| Emitter-Base Voltage        | V <sub>EBO</sub>   | -5              | V    |                                   |
| Collector Current           | I <sub>C</sub>     | -1              | Α    | Continuous                        |
| Power Dissipation           | P <sub>tot</sub> 1 | 1               | W    | At T <sub>amb</sub> ≤ +25°C       |
|                             | Ptot2              | 5               | W    | -Note-1-                          |
| Operating Temperature Range | T <sub>op</sub>    | -65 to +200     | °C   | Note & 1                          |
| Storage Temperature Range   | T <sub>stg</sub>   | -65 to +200     | °C   | Note % 1                          |
| Soldering Temperature       | T <sub>sol</sub>   | +265            | °C   | Note & 2                          |

So

see attached

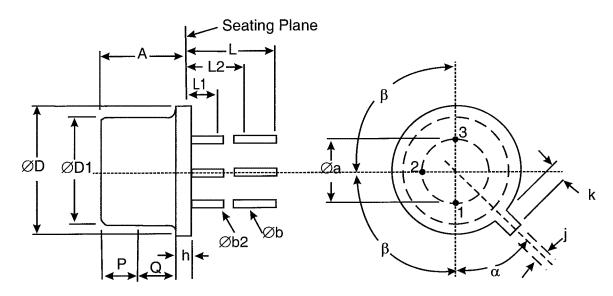
#### **NOTES:**

1.—For Tamb>+25°C, derate-linearly to 0W at +200°C

- 1. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at T<sub>amb</sub> > +125°C shall be carried out in a 100% inert atmosphere.
- 2. S. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

### 1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

#### 1.6.1 Metal Can Package (TO-39) - 3 lead



| Symbols | Dimension | Notes |        |
|---------|-----------|-------|--------|
|         | Min       | Max   | indies |
| Øa      | 4.83      | 5.35  |        |
| Α       | 6         | 6.6   |        |
| Øb      | 0.4       | 0.533 | 2, 3   |
| Øb2     | 0.4       | 0.483 | 2, 3   |

| Thermal Resistance, |               |     |      |  |
|---------------------|---------------|-----|------|--|
| Junction-to-Ambient | $R_{th(j-a)}$ | 175 | °C/W |  |
| Thermal Resistance, |               |     | ·    |  |
| Junction-to-Case    | $R_{th(j-c)}$ | 30  | °C/W |  |