



DOCUMENT CHANGE REQUEST

DCR number 503 Changes required for: General

Date: 2009/04/28

Date sent: 2009/04/28

Originator: S Jeffery - ESCC

Organisation: ESA/ESTEC

Status: IMPLEMENTED

Title: Transistors High Power NPN, based on types 2N3439 and 2N3440

Number: 5203/011

Issue: 2

Other documents affected:

Page:

See attached mark-up of 5203/011 (Issue 3 - Draft A). Note that this mark-up also includes the change of DCR 447 (DCR 447 was approved 16th December 2008); it is proposed that once this DCR has been approved, DCR 447 is introduced concurrently.

Paragraph:

See attached mark-up of 5203/011 (Issue 3 - Draft A). Note that this mark-up also includes the change of DCR 447 (DCR 447 was approved 16th December 2008); it is proposed that once this DCR has been approved, DCR 447 is introduced concurrently.

Original wording:

Proposed wording:

To introduce a number of editorial and technical changes (see the attached mark-up) which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types.

Justification:

Improve the appearance, content and clarity of the spec.

Attachments:

5203011_Issue_3_-_Draft_A.pdf, null

Modifications:

Page 6: original Note 2 to Maximum Ratings, add ", and any handling," between "testing" and "performed".

Approval signature:

A handwritten signature in black ink, appearing to read "A. G. Suter". The signature is written in a cursive style with a prominent initial "A".

Date signed:

2009-04-28



Pages 1 to 15

TRANSISTORS, HIGH VOLTAGE, NPN

BASED ON TYPE 2N3439 AND 2N3440

ESCC Detail Specification No. 5203/011

as applicable

Issue 2 3 - Draft A	February 2008
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Document Custodian: European Space Agency - see <https://escies.org>

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
187 832	Specification up issued to incorporate editorial and technical changes per DCRs.

447, tbd

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage Variants 01 to 04 Variants 05 to 08	V_{CBO}	450 300	V	Over T_{op}
Collector-Emitter Voltage Variants 01 to 04 Variants 05 to 08	V_{CEO}	350 250	V	Over T_{op}
Emitter-Base Voltage	V_{EBO}	7	V	Over T_{op}
Collector Current	I_C	1	A	
Power Dissipation	P_{tot1}	800	mW	At $T_{amb} \leq +25^\circ C$ Notes
	P_{tot2}	5	W	At $T_{case} \leq +25^\circ C$ Notes
Operating Temperature Range	T_{op}	-65 to +200	$^\circ C$	Note 1
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ C$	Note 1
Soldering Temperature	T_{sol}	+260	$^\circ C$	Note 2

make
o
bigger

NOTES:

- ~~1. For T_{amb} or $T_{case} > +25^\circ C$, derate linearly to 0W at +200 $^\circ C$.~~
1. ✂ For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^\circ C$ shall be carried out in a 100% inert atmosphere.
2. ✂ Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	218.8	$^\circ C/W$	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	35	$^\circ C/W$	



2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25 ±5 (+0-5)	°C
Power Dissipation	P_{tot}	800	mW
Collector-Emitter Voltage Variants 01, 02, 03, 04	V_{CE}	250	V
Variants 05, 06, 07, 08		180	

NOTES:

1. No heat sink nor forced air directly on the device shall be permitted.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.



APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 3) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.

(Approved DCR 447 refers)