DOCUMENT CHANGE REQUEST

DCR number 502	Changes required for: General	Originator: S Jeffery - ESCC
Date: 2009/04/28	Date sent: 2009/04/28	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	Transistors High Power NPN, based on type 2N5672		
Number:	5203/004	Issue:	2

Other documents affected:

Page:

See attached mark-up of 5203/004 (Issue 3 - Draft A). Note that this mark-up also includes the change of DCR 447 (DCR 447 was approved 16th December 2008); it is proposed that once this DCR has been approved, DCR 447 is introduced concurrently.

Paragraph:

See attached mark-up of 5203/004 (Issue 3 - Draft A). Note that this mark-up also includes the change of DCR 447 (DCR 447 was approved 16th December 2008); it is proposed that once this DCR has been approved, DCR 447 is introduced concurrently.

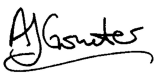
Original wording:

Proposed wording:

To introduce a number of editorial and technical changes (see the attached mark-up) which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types.

Justification:

Improve the appearance, content and clarity of the spec.

Attachments:
5203004_Issue__3_-_Draft_A.pdf, null
Modifications:
Page 6: original Note 2 to Maximum Ratings, add ", and any handling,"between "testing" and "performed".
Approval signature:

Date signed:
2009-04-28

Pages 1 to 13

TRANSISTORS, HIGH POWER, NPN

BASED ON TYPE 2N5672

ESCC Detail Specification No. 5203/004

as applicable

Issue ~~2~~ 3 – Draft A	~~February 2008~~

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
~~TBD~~	Specification up issued to incorporate editorial and technical changes per DCR's.

447, TBD

Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	1.25	°C/W	

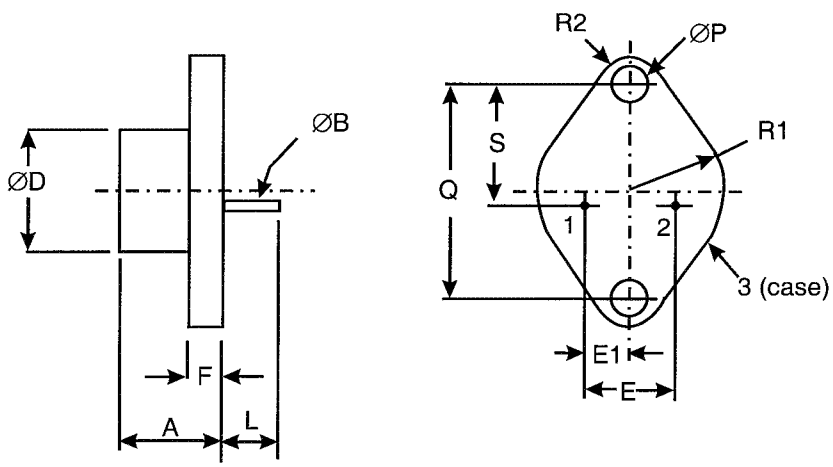
Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	150	V	Over T_{op}
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	120	V	Over T_{op}
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	7	V	Over T_{op}
Collector Current	I_C	30	A	
Base Current	I_B	10	A	
Power Dissipation	P_{tot}	140	W	At $T_{case} \leq +25°C$
Operating Temperature Range	T_{op}	-65 to +200	°C	Note 1
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note 1
Soldering Temperature	T_{sol}	+260	°C	Note 2

NOTES:

1. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125°C$ shall be carried out in a 100% inert atmosphere.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Metal Flange Mount Package (TO-3) - 2 lead



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.35	11.43	
ØB	0.97	1.09	2
ØD	-	22.23	

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Emitter Cut-off Current	I_{CEO}	±500 or (1) ±100%	-	10000	µA
Forward-Current Transfer Ratio 2	h_{FE2}	±15%	20	100	-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	±15%	-	750	mV

NOTES:
1. Whichever is greater, referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Emitter Cut-off Current	I_{CEO}	-	10	mA
Forward-Current Transfer Ratio 2	h_{FE2}	20	100	-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	750	mV

2.7 POWER BURN-IN CONDITIONS

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Characteristics	Symbols	Conditions	Units
Case Temperature	T_{case}	+100 (+0 -5)	°C
Power Dissipation	P_{tot}	As per Maximum Ratings, P_{tot} derated at the specified T_{case}	W
Collector-Base Voltage	V_{CB}	20	V

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

using the specified $R_{th(j-c)}$.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.

(Approved DCR 447 refers)