	ES C		DOCUMENT	CHANGE REQUEST	
DCR number	493	Changes required for:	General	Originator: S Jeffery - ESCC	
Date: 2009/04	/14	Date sent: 2009/04/14		Organisation: ESA/ESTEC	
Status: IMPLE	MENTED				
Title:	Transistors Low I	Power PNP, based on type	2N4033		
Number:	5202/008	Issue:	3		
Other documen	ts affected:	·			
Page:					
See attachmen	t				
Paragraph:					
See attachmen	t				
Original wording	g:				
Proposed wordi	ng:				
Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 462.					
Justification:					
Improve the appearance, content and clarity of the spec.					
Attachments:					
5202008_Issue_4Draft_B.pdf, null					
Modifications:					
N/A					
Approval signat	Approval signature:				
Albsutes					
Date signed:					
2009-04-14					

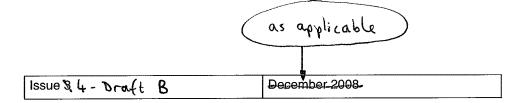


Pages 1 to 16

TRANSISTORS, LOW POWER, PNP

BASED ON TYPE 2N4033

ESCC Detail Specification No. 5202/008





Document Custodian: European Space Agency - see https://escies.org



PAGE 2 ISSUE 34 - Draft B

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PAGE 3 ISSUE&4-braft B

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION	
423, 447	Specification up issued to incorporate editorial and tec	chnical changes per DCR.
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PAGE 6 ISSUE \$ 4 ~ Droite 8

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

	Characteristics	Symbols	Maximum Ratings	Unit	Remarks	
	Collector-Base Voltage	V _{CBO}	-80	V	Over entire	
	Collector-Emitter Voltage	V _{CEO}	-80	V	operating temperature	
	Emitter-Base Voltage	V _{EBO}	-5	V	range	
	Collector Current	Ι _C	1	A	Continuous	
	Power Dissipation For TO-39 For CCP	P _{tot1}	800 500	mW	At T _{amb} ≤ +25°C Note-t∿	
	RANGER	J Ptots	760 (Note 2)	- Mo	NN	(Mak
Sea	For TO-39	P _{tot3}	800	mW	At T _{case} ≤ +25°Ô ₩o te <i>s</i> ħ	bigg
attached)	Operating Temperature Range	T _{op}	-65 to +200	°C	Note 🖏 2.	
	Storage Temperature Range	T _{stg}	-65 to +200	°C	Note & 2	
	Soldering Temperature For TO-39 For CCP	T _{sol}	+260 +245	°C	Note 💐 3 Note 5 4	
2.4 3.4 4.5	 shall be carried out in a 100% ir Duration 10 seconds maximum same lead shall not be resolder Duration 5 seconds maximum a) .6mm cerar g or hot sold nert atmosph at a distanc ed until 3 mi and the sam	nic substrate. er dip lead finish all testi nere. e of not less than 1.5m inutes have elapsed. e terminal shall not be	ng perforr m from the resoldered	e device body and th d until 3 minutes hav	PC ne ve
L[1.	elapsed. Themal Resistance, Jun Variants.	otion - to	- Case anly appl	us to	70-39 packaged	ļ
l	Variants.					

Thermal Resistance, Junction-to-Ambient	R _{th(j-a)}	218.8 350	°C/W	For TO-39 For CCP
Thermal Resistance,				
Junction-to-Case	R _{th(j-c)}	218.8	°c/w	Note 1

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PAGE 15

ISSUE \$4 - Draft B

Characteristics	Symbols	Lin	nits	Units
		Min	Max	
Collector-Base Cut-off Current	I _{CBO}	-	-50	nA
Collector-Emitter Saturation Voltage	V _{CE(sat)}	-	-150	mV
Forward-Current Transfer Ratio 2	h _{FE2}	100	300	-

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+150(+0 -5)	°C
Emitter-Base Voltage	V _{EB}	4	V
Collector-Base Voltage	V _{CB}	40	V
Duration	t	48 minimum	hours

2.8 POWER BURN-IN CONDITIONS

2.9

Ambient TemperaturePower Dissipation	T _{amb}	+20 to +50	°C
Power Dissipation			
	P _{tot}	As per Maximum Ratings.) P _{tot1} derated at the chosen T _{amb} using the	W
Collector-Base Voltage	V _{CB}	-40	V



2

PAGE 16

ISSUE \$ 4 - Draft B

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

P

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control- Chart F2	Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.
Deviations from Room Temperature Electrical Measurements	 All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.