



DOCUMENT CHANGE REQUEST

DCR number 489 Changes required for: General

Date: 2009/04/14

Date sent: 2009/04/14

Originator: S Jeffery - ESCC

Organisation: ESA/ESTEC

Status: IMPLEMENTED

Title: Transistors Low Power NPN, based on type 2N3700

Number: 5201/004 Issue: 3

Other documents affected:

Page:

See attachment

Paragraph:

See attachment

Original wording:

Proposed wording:

Various editorial and technical changes as detailed in the attachment, which are required to make this detail spec clear, complete and consistent with the standard format and content of specifications for similar Part Types. Note that this DCR replaces the withdrawn DCR 459.

Justification:

Improve the appearance, content and clarity of the spec.

Attachments:

5201004_Issue_4_-_Draft_B.pdf, null

Modifications:

N/A

Approval signature:

Date signed:

2009-04-14



Pages 1 to 14

TRANSISTORS, LOW POWER, NPN

BASED ON TYPE 2N3700

ESCC Detail Specification No. 5201/004

as applicable

Issue ~~4~~ - Draft B

~~December 2008~~



Document Custodian: European Space Agency - see <https://escies.org>



as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
423, 447 413	Specification up issued to incorporate editorial and technical changes per DCR 3 .

tbd

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	140	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	80	V	
Emitter-Base Voltage	V_{EBO}	7	V	
Collector Current	I_C	1	A	Continuous
Power Dissipation For TO-18 and CCP	P_{tot1}	0.5	W	At $T_{amb} \leq +25^\circ\text{C}$
For CCP	P_{tot2}	0.76 (Note 2)	W	At $T_{amb} \leq +25^\circ\text{C}$
For TO-18	$P_{tot} \times 2$	1.8	W	At $T_{case} \leq +25^\circ\text{C}$
Operating Temperature Range	T_{op}	-65 to +200	$^\circ\text{C}$	Note 2
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$	Note 2
Soldering Temperature For TO-18	T_{sol}	+260	$^\circ\text{C}$	Note 3
For CCP		+245		Note 4

see attached

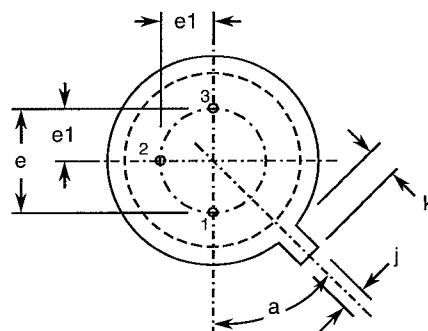
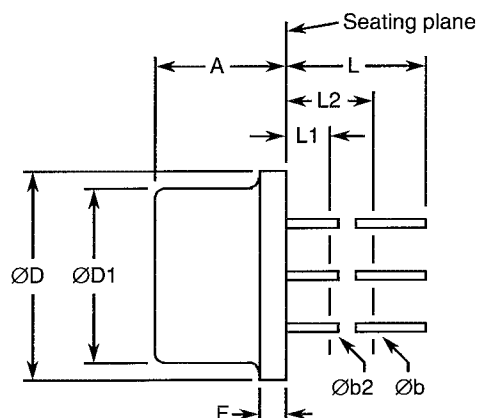
NOTES:

1. For T_{amb} or $T_{case} > +25^\circ\text{C}$, derate linearly to 0W at $+200^\circ\text{C}$.
 2. When mounted on a 15 x 15 x 0.6mm ceramic substrate.
 - 2.3 For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^\circ\text{C}$ shall be carried out in a 100% inert atmosphere.
 - 3.4 Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
 - 4.5 Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.
- [1. Thermal Resistance, Junction - to - Case only applies to TO-18 packaged Variants.

, and any handling,

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.6.1 Metal Can Package (TO-18) - 3 lead



Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	350	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	97.2	°C/W	Note 1

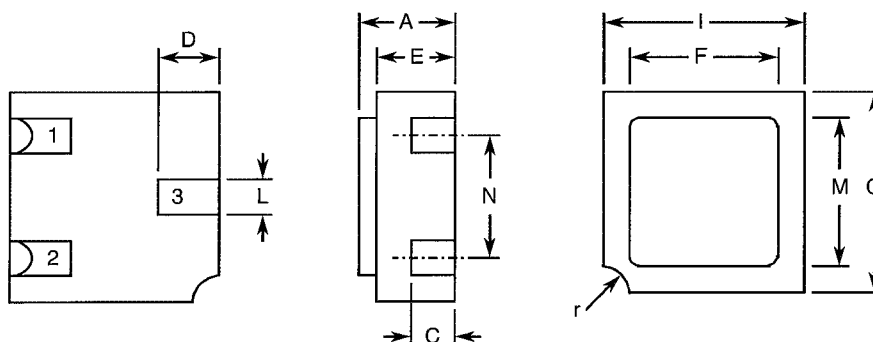
Note
addition of
horizontal
lines

Symbols	Dimensions mm		Notes
	Min	Max	
A	4.32	5.33	
Øb	0.406	0.533	2, 3
Øb2	0.406	0.483	2, 3
ØD	5.31	5.84	
ØD1	4.52	4.95	
e	2.54 BSC		4
e1	1.27 BSC		4
F	-	0.762	
j	0.914	1.17	
k	0.711	1.22	5
L	12.7	-	2
L1	-	1.27	3
L2	6.35	-	3
a	45° BSC		1, 4, 6

NOTES:

1. Terminal identification is specified by reference to the tab position where lead 1 = emitter, lead 2 = base, lead 3 = collector.
2. Applies to all leads.
3. Øb2 applies between L1 and L2. Øb applies between L2 and 12.7mm from the seating plane. Diameter is uncontrolled within L1 and beyond 12.7mm from the seating plane.
4. Leads having maximum diameter 0.483mm measured in the gauging plane 1.37(+0.025,-0)mm below the seating plane of the device shall be within 0.178mm of their true position relative to a maximum-width-tab.
5. Measured from the maximum diameter of the actual device.
6. Tab centreline.

1.6.2 Chip Carrier Package (CCP) - 3 terminal



Note
addition of
horizontal
lines

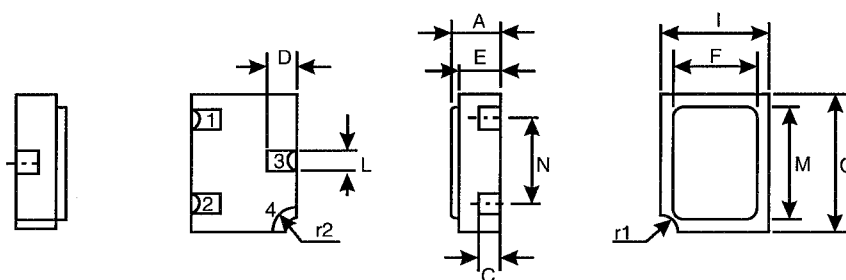
Symbols	Dimensions mm		Notes
	Min	Max	
A	1.15	1.5	
C	0.45	0.56	2
D	0.6	0.91	2
E	0.91	1.12	
F	1.9	2.15	
G	2.9	3.25	
I	2.4	2.85	
L	0.4	0.6	2
M	2.4	2.65	
N	1.8	2	
r	0.3 TYPICAL		1

NOTES:

- Terminal identification is specified by reference to the corner notch position where terminal 1 = emitter, terminal 2 = base, terminal 3 = collector.
- Applies to all terminals.

1.6.3

Chip Carrier Package (CCP) - 4 terminal



Note
addition of
horizontal
lines

Symbols	Dimensions mm		Notes
	Min	Max	
A	1.15	1.5	
C	0.45	0.56	2
D	0.6	0.91	2
E	0.91	1.12	
F	1.9	2.15	
G	2.9	3.25	
I	2.4	2.85	
L	0.4	0.6	2

Note
addition of
horizontal
lines

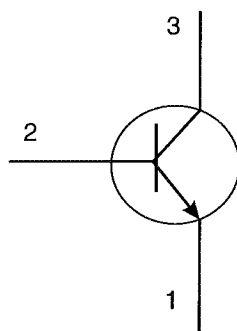
Symbols	Dimensions mm		Notes
	Min	Max	
M	2.4	2.65	
N	1.8	2	
r1	0.3 TYPICAL		1
r2	0.56 TYPICAL		1

NOTES:

- Terminal identification is specified by reference to the corner notch position where terminal 1 = emitter, terminal 2 = base, terminal 3 = collector, terminal 4 = shielding connected to the lid.
- Applies to terminals 1, 2, 3.

1.7

FUNCTIONAL DIAGRAM



- Emitter.
- Base.
- Collector.
- Shield.

NOTES:

- For TO-18, the collector is internally connected to the case.
- For 3 terminal CCP (Variants 04, 05) the lid is not connected to any terminal.
- For 4 terminal CCP (Variants 06, 07) the shielding terminal is connected to the lid.

1.8

MATERIALS AND FINISHES

Materials and finishes shall be as follows:

- Case
 - For the metal can package the case shall be hermetically sealed and have a metal body with hard glass seals.
 - For the chip carrier package the case shall be hermetically sealed and have a ceramic body with a Kovar lid.
- Leads/Terminals
 - As specified in Component Type Variants.

2.

REQUIREMENTS

2.1

GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification,

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	10	nA
Collector-Emitter Saturation Voltage 1	$V_{CE(sat)1}$	-	200	mV
Forward-Current Transfer Ratio 2	h_{FE2}	100	300	-

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Conditions	Units
Ambient Temperature	T_{amb}	+20 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings. <i>Derated at the chosen T_{amb}</i>	W
Collector-Base Voltage	V_{CB}	50	V

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

using the specified $R_{th(j-a)}$.

Derate P_{tot1}

P
APPENDIX 'A'
S -

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control-Chart F2	<p>Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.</p>
Deviations from Room Temperature Electrical Measurements	<p>All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
Deviations from High and Low Temperatures Electrical Measurements	<p>All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
Deviations from Screening Tests - Chart F3	<p>Solderability is not applicable unless specifically stipulated in the Purchase Order.</p>