DOCUMENT CHANGE REQUEST

DCR number 377	Changes required for: N/A	Originator: Ronald Fidler
Date: 2007/09/21	Date sent: 2007/09/21	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS 8-Bit Micro-Controller, based on types 80C32E and 80C52E		
Number:	9521/002	Issue:	1

Other documents affected:

Page:

Total re-format as part of the ongoing conversion to the ESCC format, scope changed from "80C32E and 80C52Eâ. to "80C32Eâ. only (the 82C52E device is no longer made) and correction to errors.

Paragraph:

Total re-format as part of the ongoing conversion to the ESCC format, scope changed from "80C32E and 80C52Eâ. to "80C32Eâ. only (the 82C52E device is no longer made) and correction to errors.

Original wording:

Proposed wording:

Rewording and restructure of various sections and paragraphs of the specification as part of the ongoing conversion to the ESCC format. This includes deletion of redundant paragraphs and replacement of Table Numbering with Paragraphs and/or Titles together with only including essential drawings and/or circuits.

NB: There is known support for active procurement against this specification from the manufacturer ATMEL.

1) Title â.. Type 80C52E deleted and the term â..ROMLESSâ. added to correctly describe the 80C32E.

2) Type Variants â..03, 04, 05 & 06 removed and Total Dose Radiation Level â..P 30kRAD(Si)â. added against 01 and 02

3) Maximum Ratings - The PD rating corrected from â..0.3Wâ. to â..1Wâ. to align with the manufacturerâ..s data sheet. CCP variant removed together with corresponding Note 5. The Thermal resistance changed to reflect the Junction to Case characteristic that is different for each package type.

4) Physical Dimensions â..Drawing, Dimensions and Titles for DIP and JLCC revised and LCC variant removed. Also drawings aligned with JEDEC industry standards MS-015 and MO-109 for these packages.

5) Pin Assignment - JLCC revised (previous specification had LCC & JLCC reversed) and LCC removed.

6) Circuit Description - Replaced by a tabulation of pin functions following Pin Assignment (previous specification

contained too much application data).

7) Functional Diagram - Changed to align with 80C32 diagram of the Data sheet.

8) Truth Table Instruction set - Removed (previously this was a list of various instructions aimed at application and/or ATE Test Program generation - an actual Truth Table was not included). Where applicable, aspects of the instructions are included in the Timing Diagrams.

9) Input Protect Networks - Pin names corrected for all three circuits.

10) Abbreviations - List removed (definitions contained within Timing Waveforms).

11) Weight - this is now given under Type Variants.

12) Electrical Measurements at Room Temperature â.. re-formatted per latest requirements. Other changes are:-

ï± Functional Test 1 â.. VDD condition corrected to 4.5V.
ï± Tests VOL1 and VOL3 amalgamated into one test as they are the same.
ï± Limit for VOH6 corrected to 4.05V (0.9xVDD) per the manufacturerâ..s data sheet for this component.
ï± VOH7, VOH8 and VOH9 amalgamated with VOH1, VOH3 and VOH5 respectively as they are the same tests.

13) Electrical Measurements at Low & High Temperature - Table deleted and new text added â..... same as specified for Room Temperature Electrical Measurementsâ..

14) Circuits for Electrical Measurements - All deleted, where necessary, extra detail has been given under the Test Conditions of Electrical Measurements at Room Temperature and Timing Diagrams

15) Parameter Drift Values - VOL3 and VOH7 deleted.

16) Intermediate and end-point Electrical Measurements - VOL3 and VOH7 deleted.

17) Power Burn-in and Operating Life Conditions - changes are:-

ï± Electrical Circuit (ex Figure 5) deleted. Note 2 now added to Power Bum-in Conditions and references to Pin Numbers changed to Pin Functions.
ï± Symbol GEN2 changed to fGEN2 and what was Note 2 incorporated into Test Conditions.

18) Total Dose Irradiation Testing - Changes are:-

ï± Bias Conditions Circuit (ex Figure 6) deleted and instead requirements tabulated under " Bias Conditions and Total Dose Level for Total Dose Radiation Testing"
ï± Electrical Measurements - VOL3 and VOH7 deleted.

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Justification:

As defined above.

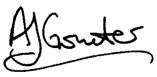
Attachments:

9521002.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2007-09-21

Pages 1 to 30

INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS 8-BIT ROMLESS MICROCONTROLLER

BASED ON TYPE 80C32E

ESCC Detail Specification No. 9521/002

Issue 2 Draft A	September 2007

Document Custodian: European Space Agency - see https://escies.org

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DCR No.	CHANGE DESCRIPTION
TBD	Specification up issued to incorporate editorial and technical changes per DCR.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:
Example: 952100201P

- Detail Specification Reference: 9521002
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: P (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	80C32	MDIL40	D2	8	P [30kRAD(Si)]
02	80C32	MQFPJ44	G3	5	P [30kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
The total dose radiation level letter shall be as defined in ESCC Basic Specification no. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.3 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.3 to V_{DD} +0.3	V	Notes 1, 2
Output Current	I_{OUT}	±80	mA	Note 3
Device Power Dissipation (Continuous)	P_D	1	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+265	^oC	Note 4
Junction Temperature	T_j	+165	^oC	
Thermal Resistance Junction to Case For MDIL40 For MQFPJ44	$R_{th(j-c)}$	 8 6	$^oC/W$	

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional for $4.5V \leq V_{DD} \leq 5.5V$.
2. V_{DD}+0.3V shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

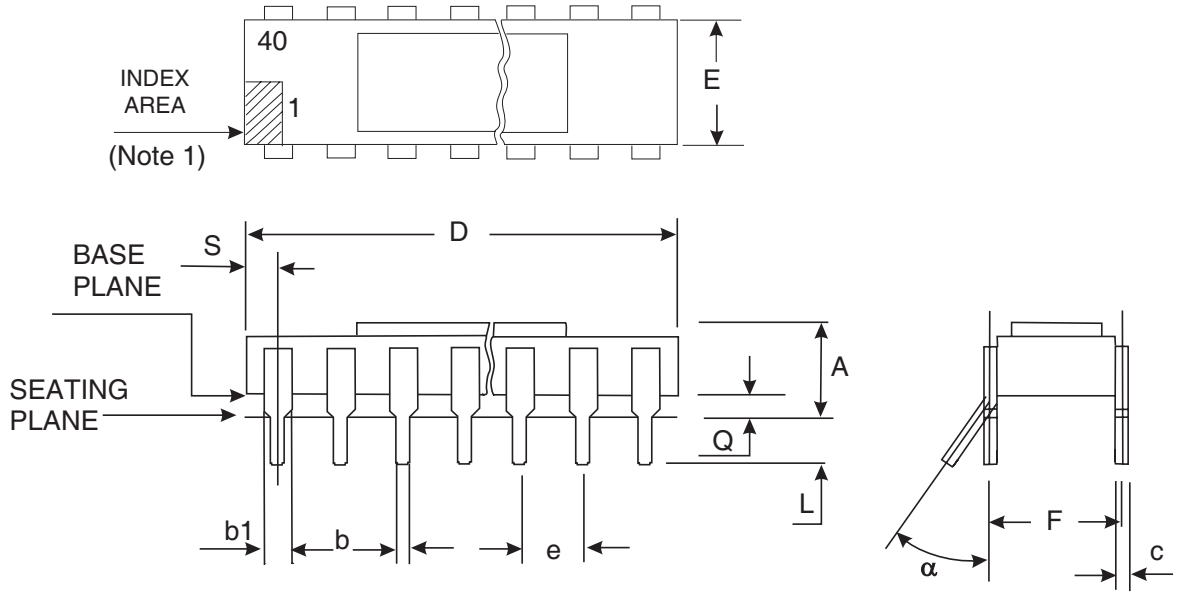
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

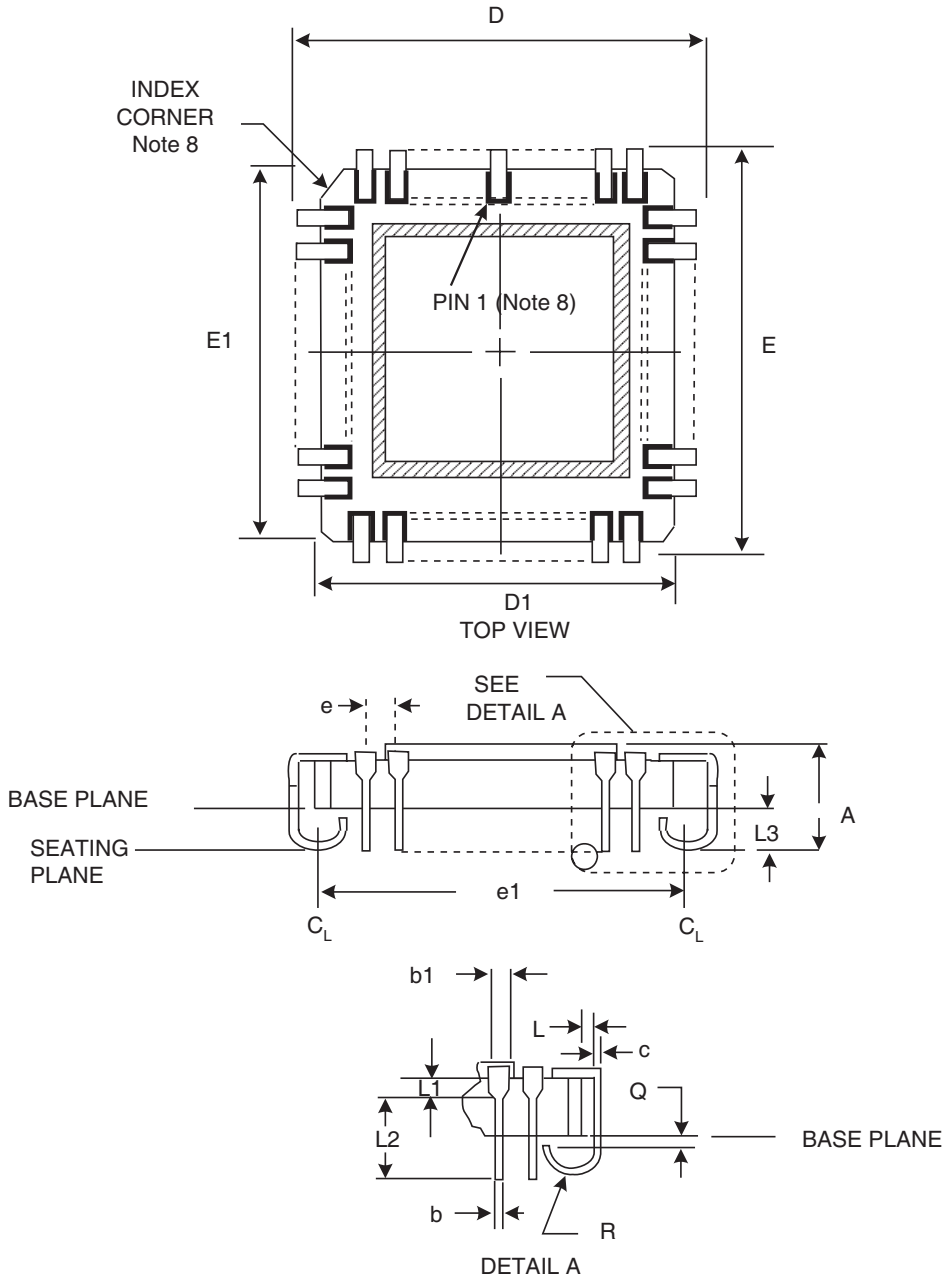
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Ceramic Multilayer Dual-in-Line Package (MDIL40) - 40 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.16	4.83	2
b	0.38	0.58	3
b1	0.97	1.52	3
c	0.2	0.3	3
D	50.3	51.56	
E	14.74	15.49	
e	2.54 BSC		3, 4
F	15.12	15.87	3, 5
L	3.18	4.44	2, 3
S	0.77	1.65	6
Q	0.51	1.77	2, 7
α	0^o	15^o	3

1.7.2 Ceramic Multilayer J-BEND Leaded Chip Carrier (MQFPJ44) - 44 Lead



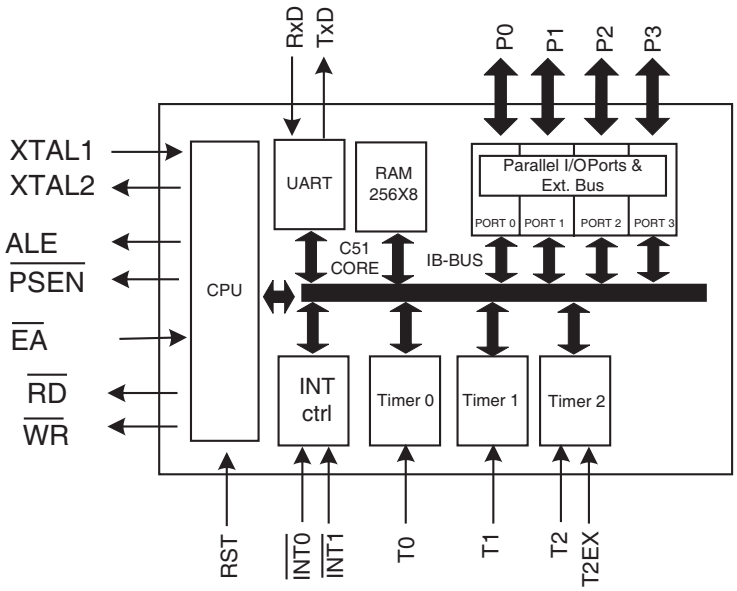
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.67	4.95	
b	0.33	0.56	9
b1	0.55	0.88	9
c	0.17	0.25	9
D/E	17.14	17.78	
D1/E1	15.74	16.76	

Symbols	Dimensions mm		Notes
	Min	Max	
e	1.27 BSC		9, 10
e1	16 BSC		11
L	0.12	-	9
L1	0.51	-	9
L2	0.63	-	9
L3	0.58	-	9, 12
Q	0.07	-	
R	0.5	1.01	9

1.7.3 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. Dimensions are measured with the package seated in a seating plane gauge.
3. All leads.
4. 38 places. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. Dimensions are measured with the leads constrained to be perpendicular to the base plane.
6. Two places.
7. The dimension shall be measured from the seating plane to the base plane.
8. A terminal identification mark shall be located in the region of Pin 1 as shown. Terminal numbers shall increase counter-clockwise when viewed as shown starting from the centre terminal (Pin 1). The index corner shall be clearly unique but may vary from that shown on the drawing.
9. Applies to all 44 terminations (11 per side).
10. 40 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to the package centrelines.
11. Four places.
12. Measured from Seating Plane to Base Plane (i.e., including dimension Q).

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Name	
	MDIL40	MQFPJ44
1	T2/P1.0	-
2	T2EX/P1.1	T2/P1.0
3	P1.2	T2EX/P1.1
4	P1.3	P1.2
5	P1.4	P1.3
6	P1.5	P1.4
7	P1.6	P1.5
8	P1.7	P1.6
9	RST	P1.7
10	P3.0/RXD	RST
11	P3.1/TXD	P3.0/RXD
12	P3.2/$\overline{\text{INT0}}$	-
13	P3.3/$\overline{\text{INT1}}$	P3.1/TXD
14	P3.4/T0	P3.2/$\overline{\text{INT0}}$
15	P3.5/T1	P3.3/$\overline{\text{INT1}}$
16	P3.6/$\overline{\text{WR}}$	P3.4/T0
17	P3.7/$\overline{\text{RD}}$	P3.5/T1

Pin	Name	
	MDIL40	MQFPJ44
18	XTAL2	P3.6/$\overline{WR}$
19	XTAL1	P3.7/$\overline{RD}$
20	V_{SS}	XTAL2
21	P2.0	XTAL1
22	P2.1	V_{SS}
23	P2.2	-
24	P2.3	P2.0
25	P2.4	P2.1
26	P2.5	P2.2
27	P2.6	P2.3
28	P2.7	P2.4
29	$\overline{PSEN}$	P2.5
30	ALE	P2.6
31	$\overline{EA}$	P2.7
32	P0.7	$\overline{PSEN}$
33	P0.6	ALE
34	P0.5	-
35	P0.4	$\overline{EA}$
36	P0.3	P0.7
37	P0.2	P0.6
38	P0.1	P0.5
39	P0.0	P0.4
40	V_{DD}	P0.3
41	-	P0.2
42	-	P0.1
43	-	P0.0
44	-	V_{DD}

Pin Name	Type Note 1	Function
Port 0 (P0.0-7)	I/O	Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float and, in that state, can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus (A0 - A7) during access to external programme and data memory. In this application, it uses strong internal pull-ups when emitting 1's. External pull-ups are required during programme verification. Port 0 can sink eight LS TTL inputs.
Port 1 (P1.0-7)	I/O	Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups. Port 1 also receives the lower address byte during programme verification. It can drive CMOS inputs without external pull-ups. Also in this device Port 1 can sink/source three LS TTL inputs. Two inputs of Port 1 are also used for Timer/Counter 2: - P1.0: (T2) External Clock Inputs. - P1.1: (T2EX) Trigger input to be reloaded or captured causing Timer/Counter 2 to interrupt.
Port 2 (P2.0-9)	I/O	Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs Port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte (A8 - A15) during fetches from external Programme Memory and during accesses to external Data Memory that use 16-bit addresses. In this application, it uses strong internal pull-ups when emitting 1's. During access to external Data Memory that use 8-bit addresses, Port 2 emits the contents of the P2 Special Function Register (SFR - P2). Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs with external pull-ups. Port 2 also receives the high-order address bit and control signals during programme verification.
Port 3 (P3.0-7)	I/O	Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups. It also serves the functions of various special features of the 8051 family as listed in Note 2. Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pull-ups.

Pin Name	Type Note 1	Function
RST	I	Device Reset: A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connector to V_{DD}. As soon as the reset is applied (V_{IN}), Ports 1, 2 and 3 are tied to "1". this operation is achieved asynchronously even if the oscillator does not start up.
ALE	O	Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 of the oscillator frequency except during an external data memory access, at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.
$\overline{\text{PSEN}}$	O	Programme Store Enable output is the read strobe to external Programme Memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external Programme Memory (however when executing out of external programme memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external Data Memory). $\overline{\text{PSEN}}$ is not activated during fetches from internal Programme Memory. $\overline{\text{PSEN}}$ can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.
$\overline{\text{EA}}$	I	When $\overline{\text{EA}}$ is held high, the CPU executes out of internal Programme Memory (unless the Programme Counter exceeds 3FFFH). When $\overline{\text{EA}}$ is held low, the CPU executes only out of external Programme Memory. $\overline{\text{EA}}$ must not be floated.
XTAL1	I	Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.
XTAL2	O	Output of the inverting amplifier that forms the oscillator and input of the internal clock generator. This pin should be floated when an external oscillator is used.

NOTES:

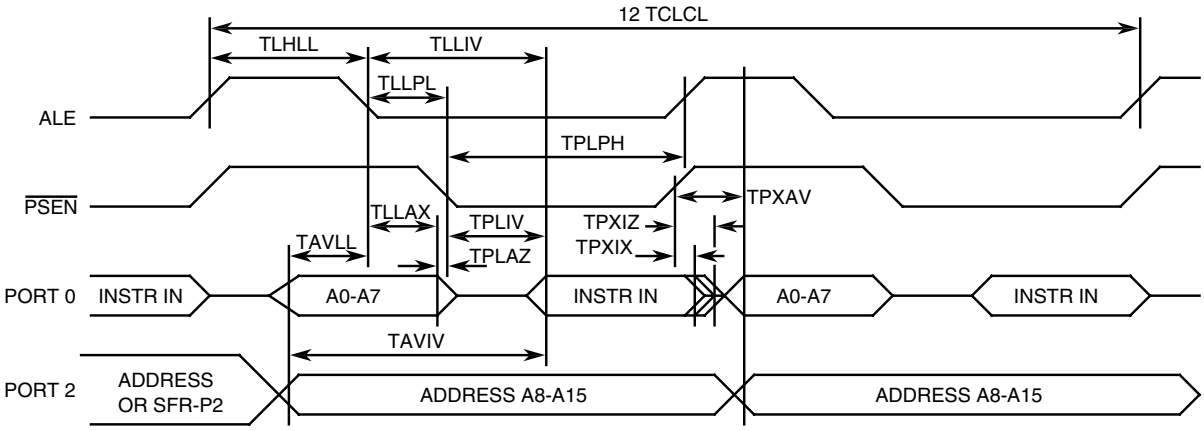
1. I=Input, O=Output, I/O=Input/Output.
2. Port 3 special features:

Port 3 Pin Name	Alternate Pin Name and Function
P3.0	RXD (Serial input port)
P3.1	TXD (Serial output port)
P3.2	$\overline{\text{INT0}}$ (External interrupt 0)
P3.3	$\overline{\text{INT1}}$ (External interrupt 1)
P3.4	T0 (Timer 0 external input)

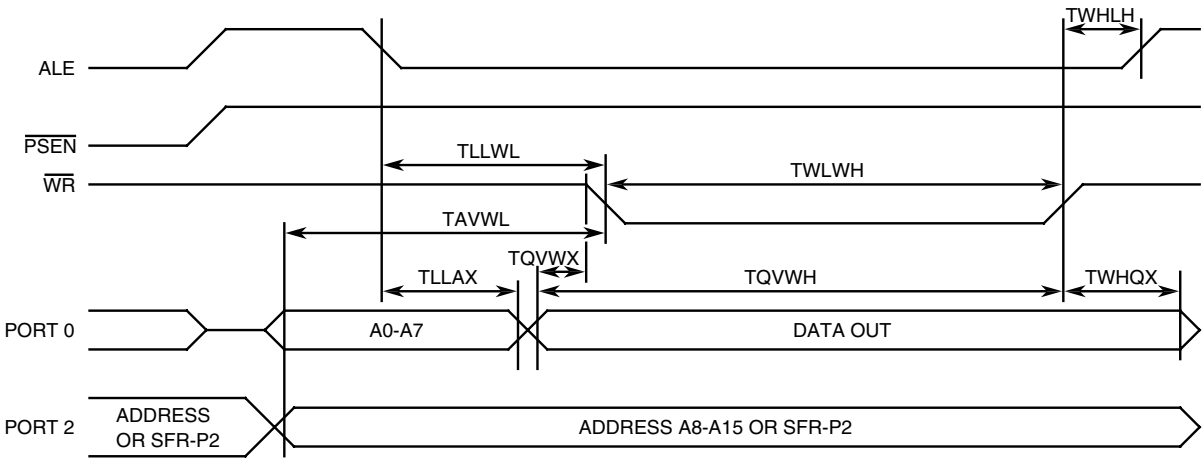
Port 3 Pin Name	Alternate Pin Name and Function
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (External data memory write strobe)
P3.7	$\overline{RD}$ (External data memory read strobe)

1.10 TIMING DIAGRAMS

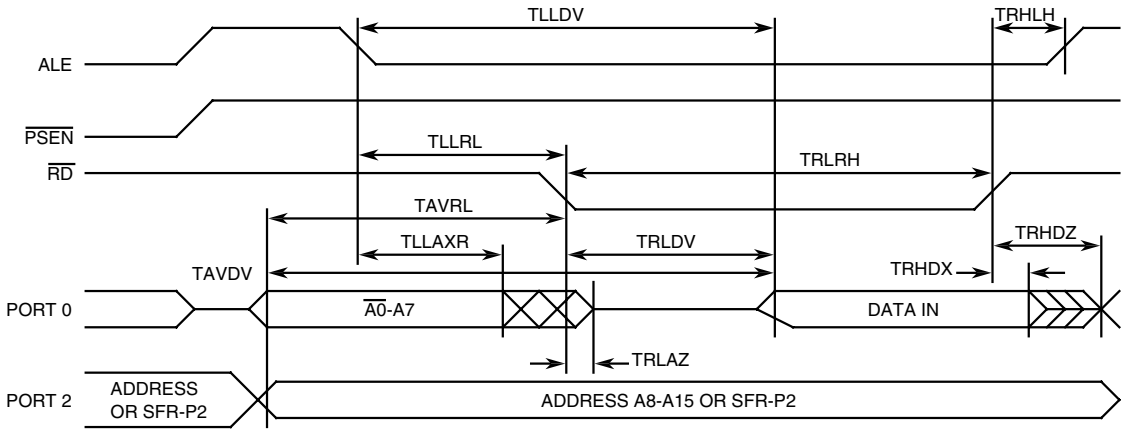
External Programme Memory Read Cycle



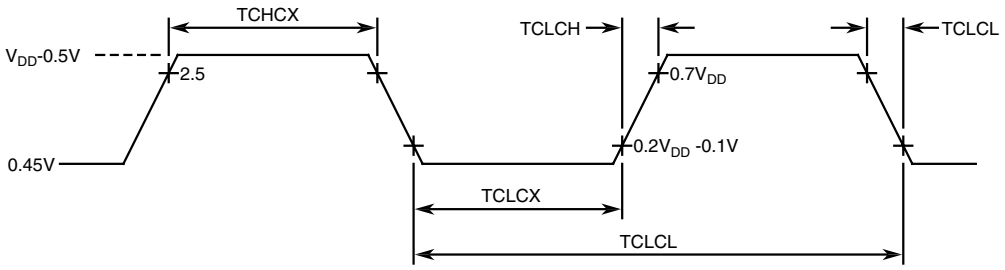
External Data Memory Write Cycle



External Data Memory Read Cycle



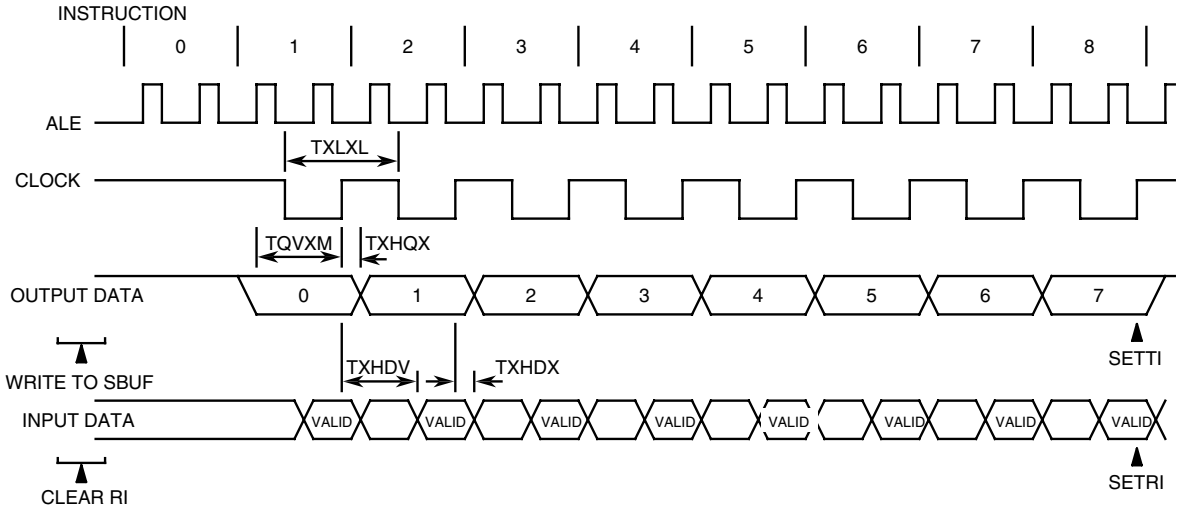
External Clock Waveforms



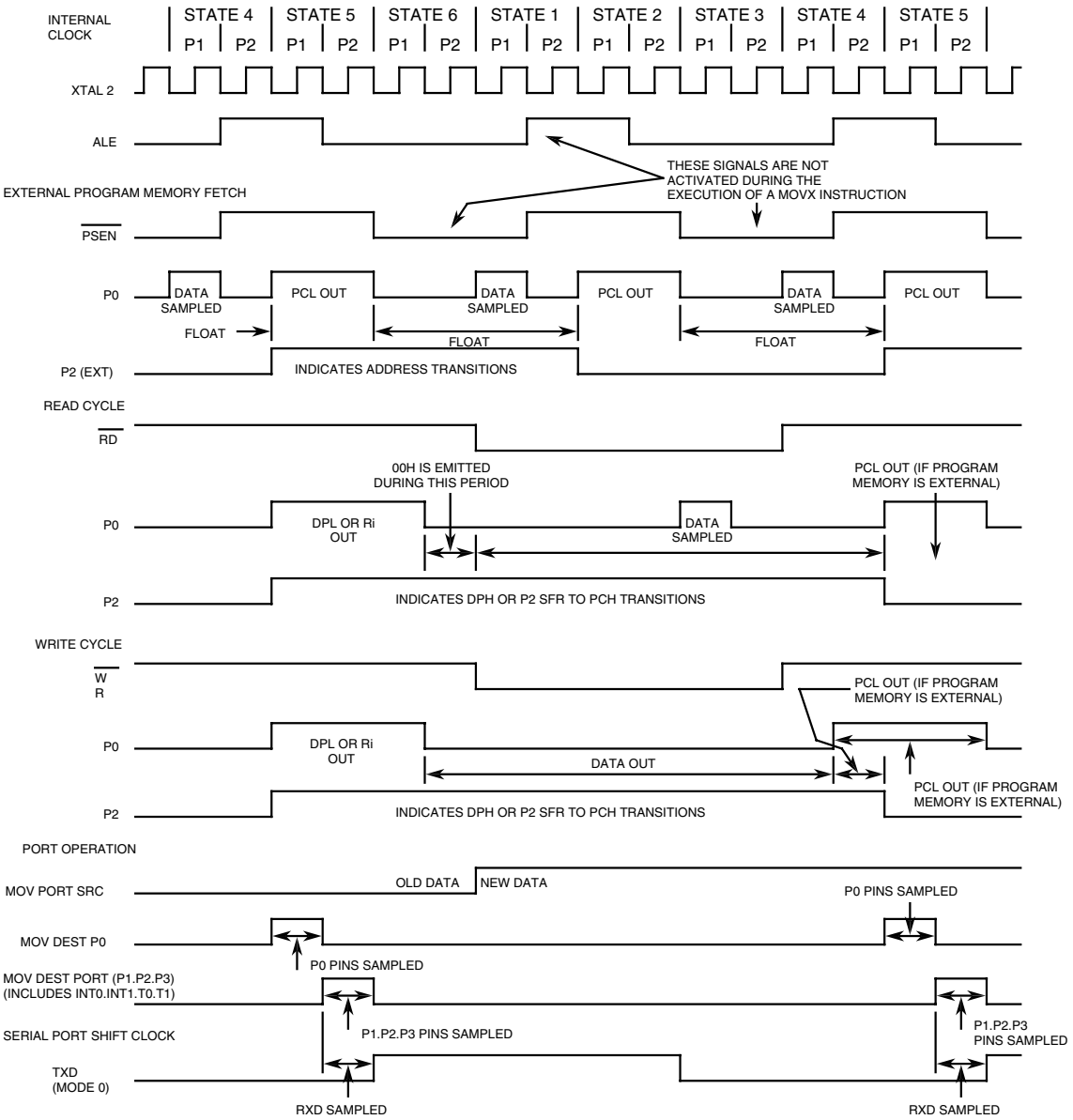
External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min.	Max.	Unit
TCLCL	Oscillator Period	33.33		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

Shift Register Timing Waveforms

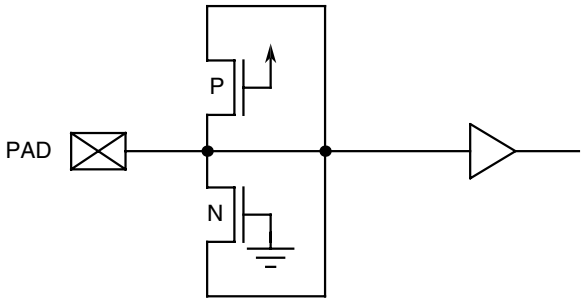


Internal Clock Waveforms

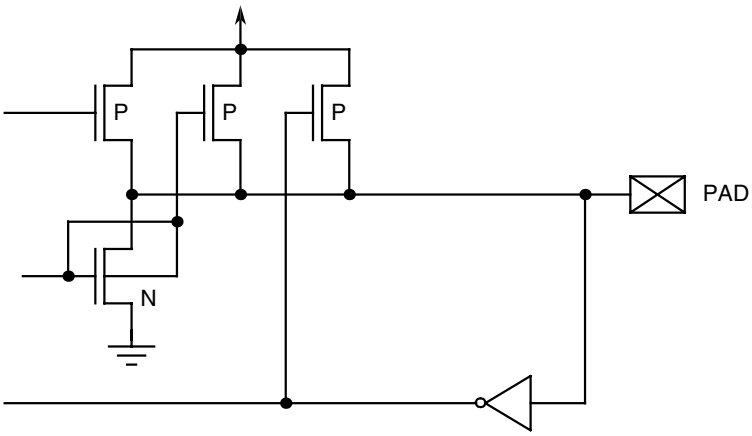


1.11 INPUT PROTECTION NETWORKS

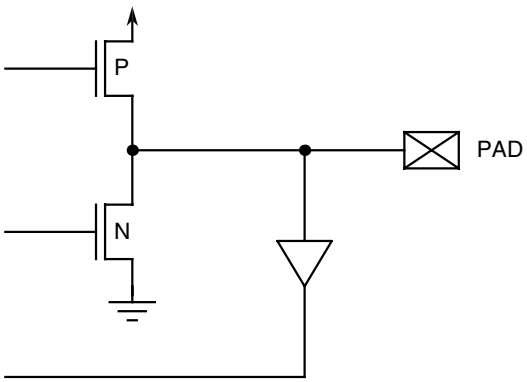
Inputs $\overline{EA}$, RST, XTAL1



I/O's P1.n, P2.n, P3.n



I/O's P0.n, ALE, $\overline{PSEN}$



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this

specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.
Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.
The information to be marked on the component shall be:
(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Function without Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=1MHz V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Function without Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=1MHz V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3	-	3014	Verify Function without Load V_{IL}=0.8V V_{IH}=2.2V V_{OUT}=1.5V f=1MHz V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 4	-	3014	Verify Function without Load V_{IL}=0.8V V_{IH}=2.2V V_{OUT}=1.5V f=1MHz V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 5	-	3014	Verify Function with Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=1MHz Outputs: 1TTL+50pF V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 6	-	3014	Verify Function with Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=1MHz Outputs: 1TTL+50pF V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 7	-	3014	Verify Function with Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=12MHz Outputs: 1TTL+50pF V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 8	-	3014	Verify Function with Load V_{IL}=0V V_{IH}=3V V_{OUT}=1.5V f=12MHz Outputs: 1TTL+50pF V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	3022	I_{IN} (Under Test)= 100µA All Other Pins Open V_{DD}=Open, V_{SS}=0V Note 3	200	-	mV
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	3022	I_{IN} (Under Test)= 100µA All Other Pins Open V_{DD}=0V, V_{SS}=Open Note 3	-	-200	mV
Low Level Input Leakage Current 1	I_{IL1}	3009	V_{IN} (Under Test)=450mV V_{DD}=5.5V,V_{SS}=0V	-	±10	µA
Low Level Input Leakage Current 2	I_{IL2}	3009	I/O Ports P1, P2, P3: V_{IN} (Under Test)=450mV V_{IN}(Remaining Inputs)=0V V_{DD}=5.5V,V_{SS}=0V	-	-75	µA
High Level Input Leakage Current	I_{IH}	3010	V_{IN} (Under Test)=5.5V V_{DD}=5.5V,V_{SS}=0V	-	±10	µA
High Level to Low Level Transition Current	I_{IT}	-	I/O Ports P1, P2, P3: V_{IN} (Under Test)=2V V_{IN}(Remaining Inputs)=0V V_{DD}=5.5V,V_{SS}=0V	-	-750	µA
Low Level Output Voltage 1	V_{OL1}	3007	I/O Port PO, ALE, $\overline{PSEN}$: I_{OL}=3.2mA V_{DD}=4.5V, V_{SS}=0V	-	450	mV
Low Level Output Voltage 2	V_{OL2}	3007	I/O Ports P1, P2, P3: I_{OL}=1.6mA V_{DD}=4.5V, V_{SS}=0V	-	450	mV
High Level Output Voltage 1	V_{OH1}	3006	I/O Port PO, ALE, $\overline{PSEN}$: I_{OH}=-400µA V_{DD}=4.5V, V_{SS}=0V	2.4	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Output Voltage 2	V_{OH2}	3006	I/O Ports P1, P2, P3: I_{OH}=-60µA V_{DD}=4.5V, V_{SS}=0V	2.4	-	V
High Level Output Voltage 3	V_{OH3}	3006	I/O Port PO, ALE, $\overline{PSEN}$: I_{OH}=-150µA V_{DD}=4.5V, V_{SS}=0V Note 3	3.375	-	V
High Level Output Voltage 4	V_{OH4}	3006	I/O Ports P1, P2, P3: I_{OH}=-25µA V_{DD}=4.5V, V_{SS}=0V Note 3	3.375	-	V
High Level Output Voltage 5	V_{OH5}	3006	I/O Port PO, ALE, $\overline{PSEN}$: I_{OH}=-40µA V_{DD}=4.5V, V_{SS}=0V Note 3	4.05	-	V
High Level Output Voltage 6	V_{OH6}	3006	I/O Ports P1, P2, P3: I_{OH}=-10µA V_{DD}=4.5V, V_{SS}=0V Note 3	4.05	-	V
Idle Supply Current	I_{DDI}	3005	V_{IL}=0.5V,V_{IH}=5V V_{IN}($\overline{EA}$, RST)=0V V_{IN}(P0.n)=5.5V XTAL2=NC All Outputs Open f=30MHz V_{DD}=5.5V,V_{SS}=0V Note 4	-	15	mA
Operating Supply Current	I_{DDOP}	3005	V_{IL}=0.5V,V_{IH}=5V V_{IN}($\overline{EA}$, RST, P0.n)=0V XTAL2=NC All Outputs Open f=30MHz V_{DD}=5.5V,V_{SS}=0V Note 4	-	50	mA
Power-Down Supply Current 1	I_{DDPD1}	3005	All Outputs Open V_{IN}($\overline{EA}$,P0.n)=2V V_{IN}(RST, XTAL1)=0V XTAL2=NC V_{DD}=2V,V_{SS}=0V Note 3	-	75	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Power-Down Supply Current 2	I_{DDPD2}	3005	All Outputs Open V_{IN}($\overline{EA}$,P0.n)=5.5V V_{IN}(RST, XTAL1)=0V XTAL2=NC V_{DD}=5.5V,V_{SS}=0V	-	75	µA
Reset Resistor	R_{RST}	-	V_{DD}=4.5V, V_{SS}=0V	50	200	kΩ
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test)=0V f=1MHz V_{DD}= V_{SS}=0V Note 5	-	10	pF
Output Capacitance	C_{OUT}	3012	V_{OUT} (Not Under Test)=0V f=1MHz V_{DD}= V_{SS}=0V Note 5	-	10	pF
Address Latch Enable Pulse Width	t_{LHLL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	60	-	ns
Address Valid to Address Latch Enable	t_{AVLL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	15	-	ns
Address Hold to Address Latch Enable	t_{LLAX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	35	-	ns
Address Latch Enable to Valid Instruction In	t_{LLIV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	100	-	ns
Programme Store Enable to Valid Instruction In	t_{PLIV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	65	-	ns
Address to Valid Instruction In	t_{AVIV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	130	-	ns
Programme Store Enable Low to Address Float	t_{PLAZ}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	-	6	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Read Strobe to Valid Data In	t_{RLDV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	135	-	ns
Address Latch Enable to Valid Data In	t_{LLDV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	235	-	ns
Address Latch Enable to Write Strobe	t_{LLWL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	90	115	ns
Address to Write Strobe	t_{AVWL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	115	-	ns
Address to Read Strobe	t_{AVRL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Note 6	115	-	ns
Address Latch Enable to Programme Store Enable	t_{LLPL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	25	-	ns
Programme Store Enable Pulse Width	t_{PLPH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	80	-	ns
Programme Store Enable to Input Instruction Hold	t_{PXIX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	-	0	ns
Programme Store Enable to Input Instruction Float	t_{PXIZ}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	-	30	ns
Programme Store Enable to Address Valid	t_{PXAV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	30	-	ns
Read Strobe Pulse Width	t_{RLRH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	180	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Write Strobe Pulse Width	t_{WLWH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	180	-	ns
Address Latch Enable to Data Address Hold	t_{LLAXR}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	55	-	ns
Read Strobe to Data Hold	t_{RHDX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	-	0	ns
Read Strobe to Data Float	t_{RHDZ}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	60	-	ns
Address to Valid Data In	t_{AVDV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	260	-	ns
Address Latch Enable to Read Strobe	t_{LLRL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	90	115	ns
Data Valid to Write Strobe	t_{QVWX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	20	-	ns
Data Setup to Write Strobe high	t_{QVWH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	215	-	ns
Write Strobe to Data Hold	t_{WHQX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	20	-	ns
Read Strobe to Address Float	t_{RLAZ}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	-	0	ns
Write Strobe to Address Latch Enable High	t_{WHLH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	20	40	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Read Strobe High to Address Latch Enable High	t_{RHLH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	20	40	ns
Serial Port Clock Cycle Time	t_{XLXL}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	400	-	ns
Out Data Setup to Clock	t_{QVXH}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	300	-	ns
Clock to Out Data Hold	t_{XHQX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	50	-	ns
Clock to In Data Hold	t_{XHDX}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	-	0	ns
Clock High to In Data Valid	t_{XHDV}	3003	f=30MHz V_{DD}=4.5 & 5.5V V_{SS}=0V Notes 3, 6	300	-	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional test shall verify the operation of the instruction set, internal registers, interrupts, timer, serial port, external data, programme counter, RAM, idle mode and the power-down mode. Functional test shall also guarantee the following parameters:

V_{IL} min = -0.5V	V_{IL} max = $0.2V_{DD}$-0.25V (0.85V at 5.5V) Except pin $\overline{EA}$: V_{IL} max=$0.2V_{DD}$-0.45V.
V_{IH} max = V_{DD}+0.5V	V_{IH} min = $0.2V_{DD}$+1.1V (2V at 4.5V) Except pins XTAL1, RST: V_{IH} min = $0.7V_{DD}$+0.2V.

3. Guaranteed but not tested.
4. XTAL1 is driven with t_{CLCH}=t_{CHCL}=5ns.
5. Characterised at initial design or at major design or process change. Guaranteed but not tested.
6. For AC parameter measurements unless otherwise stated:
   - The load capacitance for I/O Port P0, ALE and $\overline{PSEN}$ = 100pF
   - The load capacitance for all other outputs = 80pF
   - Refer to Timing Diagrams herein.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125(+0-5)°C and T_{amb}=-55(+5-0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ± 3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.
The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Leakage Current 1	I_{IL1}	±1	-	±10	µA
Low Level Input Current 2	I_{IL2}	±7.5	-	-75	µA
High Level Input Leakage Current	I_{IH}	±1	-	±10	µA
High Level to Low Level Transition Current	I_{IT}	±75	-	-750	µA
Low Level Output Voltage 1	V_{OL1}	±40	-	450	mV
Low Level Output Voltage 2	V_{OL2}	±40	-	450	mV
High Level Output Voltage 1	V_{OH1}	±0.2	2.4	-	V
High Level Output Voltage 2	V_{OH2}	±0.2	2.4	-	V
Operating Supply Current	I_{DDOP}	±5	-	50	mA
Power-Down Supply Current 2	I_{DDPD2}	±7.5	-	75	µA

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.
The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Functional Test 1	-	-	-	-
Functional Test 2	-	-	-	-
Functional Test 3	-	-	-	-
Functional Test 4	-	-	-	-
Functional Test 5	-	-	-	-
Functional Test 6	-	-	-	-
Functional Test 7	-	-	-	-

Characteristics	Symbols	Limits		Units
		Min	Max	
Functional Test 8	-	-	-	-
Low Level Input Leakage Current 1	I_{IL1}	-	±10	µA
Low Level Input Leakage Current 2	I_{IL2}	-	-75	µA
High Level Input Leakage Current	I_{IH}	-	±10	µA
High Level to Low Level Transition Current	I_{IT}	-	-750	µA
Low Level Output Voltage 1	V_{OL1}	-	450	mV
Low Level Output Voltage 2	V_{OL2}	-	450	mV
High Level Output Voltage 1	V_{OH1}	2.4	-	V
High Level Output Voltage 2	V_{OH2}	2.4	-	V
Idle Supply Current	I_{DDI}	-	15	mA
Operating Supply Current	I_{DDOP}	-	50	mA
Power-Down Supply Current 2	I_{DDPD2}	-	75	µA
Reset Resistor	R_{RST}	50	200	kΩ
Address Latch Enable Pulse Width	t_{LHLL}	60	-	ns
Address Valid to Address Latch Enable	t_{AVLL}	15	-	ns
Address Hold to Address Latch Enable	t_{LLAX}	35	-	ns
Address Latch Enable to Valid Instruction In	t_{LLIV}	100	-	ns
Programme Store Enable to Valid Instruction In	t_{PLIV}	65	-	ns
Address to Valid Instruction In	t_{AVIV}	130	-	ns
Read Strobe to Valid Data In	t_{RLDV}	135	-	ns
Address Latch Enable to Valid Data In	t_{LLDV}	235	-	ns
Address Latch Enable to Write Strobe	t_{LLWL}	90	115	ns
Address to Write Strobe	t_{AVWL}	115	-	ns
Address to Read Strobe	t_{AVRL}	115	-	ns

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs P0.n, P1.n, P2.n, P3.n, $\overline{PSEN}$, ALE	V_{OUT}	Parallel Connected (Notes 1, 2)	V

Characteristics	Symbols	Test Conditions	Units
Input $\overline{EA}$	V_{IN}	V_{DD} (Notes 1, 2)	V
Output XTAL2	V_{OUT}	V_{SS} (Notes 1, 2)	V
Input XTAL1	V_{IN}	V_{GEN1} (Notes 1, 2)	V
Input RST	V_{IN}	V_{GEN2} (Notes 1, 2)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}	400k ±20% 50% Duty Cycle	Hz
Pulse Frequency Square Wave	f_{GEN2}	3.77k 22.6% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	+5.5 (+0-0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = Output Load = 1kΩ.
2. All inputs and outputs are connected to their equivalents on each device by a common bus.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.
The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	°C
Output XTAL2	V_{OUT}	Open	V
Input RST	V_{IN}	V_{GEN} (Note 1)	V
Inputs/Outputs Remaining	$V_{IN/OUT}$	V_{DD} (Note 1)	V
Pulse Voltage	V_{GEN}	0 to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	3.77k 22.6% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	5±0.1	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = Output Load = 1kΩ

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb}=22±3°C. The test methods and test conditions shall be as per the corresponding test defined in electrical measurements at Room Temperature.

The parameters to be measured during and on completion of radiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits		Units
		Min	Max	
Idle Supply Current	I_{IL1}	-	±10	µA
High Level Input Leakage Current 1	I_{IH}	-	±10	µA
Low Level Input Leakage Current 2	I_{IL2}	-	-75	µA
High Level to Low Level Transition Current	I_{IT}	-	-750	µA
Low Level Output Voltage 1	V_{OL1}	-	450	mV
Low Level Output Voltage 2	V_{OL2}	-	450	mV
High Level Output Voltage 1	V_{OH1}	2.4	-	V
High Level Output Voltage 2	V_{OH2}	2.4	-	V
Idle Supply Current	I_{DDI}	-	100	mA
Operating Supply Current	I_{DDOP}	-	100	mA
Power-Down Supply Current 2	I_{DDPD2}	-	15	mA