DOCUMENT CHANGE REQUEST

DCR number 207	Changes required for: General	Originator: Steve Thacker
Date: 2005/10/25	Date sent: 2005/10/25	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	IC Silicon Monolithic, 32-BIT SPARC Embedded Processor, based on Type TSC695F		
Number:	9512/003	Issue:	1

Other documents affected:

Page:

Page 5 Para 1.4.2
Page 7 Para 1.7.1
Page 29 Para 2.1
Page 30, 31 Para 2.3.1
Page 34 Para 2.3.3
Page 35 Para 2.4
Page 36 Para 2.6
Page 39 Para 2.7
Page 39 Para 2.8.1

Paragraph:

Page 5 Para 1.4.2
Page 7 Para 1.7.1
Page 29 Para 2.1
Page 30, 31 Para 2.3.1
Page 34 Para 2.3.3
Page 35 Para 2.4
Page 36 Para 2.6
Page 39 Para 2.7
Page 39 Para 2.8.1

Original wording:

Proposed wording:

See attached mark-up for details.

1) Page 5, 39 Para 1.4.2, 2.7, 2.8.1. Capitalise the term "Purchase Order"

2) Page 7 Para 1.7.1. Amend the title. Amend the table header titles. Add notes 1 & 2

DOCUMENT CHANGE REQUEST

DCR number 207	Changes required for: General	Originator: Steve Thacker
Date: 2005/10/25	Date sent: 2005/10/25	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

3) Page 29 Para 2.1. Delete "applicable" from sub-para 1 and 2.

4) Page 30, 31, 35 Para 2.3.1 & 2.4. Amend the limits for IIL1, IIL2, IOZL to be max values (instead of Min values) to be in line with the convention being applied to ESCC detail specifications (as per 54HCMOS detail specifications) where min/max limits are independant of the polarity of the limit value.
Capitalise and removed parentheses for charateristic titles (IOZL, IOHZ, IDDPD, IDDOP)
Amend symbol for input Capacitance to be "CIN" (was "CI")

5) Page 34 Para 2.3.3. Move the contents of para 2.3.3 to be part of para 2.3.1

6) Page 36, 39 Para 2.6, 2.8.1. Add "note 1" to VGEN1 & VGEN2 test conditions

7) Some other minor editorial changes have been incorported due to the change to the publishing software being used for ESCC specifications.

Justification:

1), 2), 3), 4), 5), 6), 7) Editorial amendments made for the purposes of clarification plus consistency with other ESCC detail specifications.

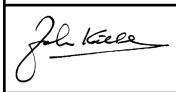
Attachments:

Mark-up_for_DCR_on_9512003.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2005-10-25

MARK-UP
Showing amendments
for DCR.
Conversion from
Globalview to
Framemaker
software
S. Inacio.
20/10/2005

ESCC
European Space Components Coordination

Pages 1 to 40

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

32-BIT SPARC EMBEDDED PROCESSOR,

BASED ON TYPE TSC695F

ESCC Detail Specification No. 9512/003

2 Draft A

ISSUE ~~1~~

~~February 2004~~

October 2005.

esa

Document Custodian: European Space Agency - see https://escies.org

2005

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
TBD1 TBD2	Specification up issued to incorporate editorial and Technical changes per DCR

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specfied in ESCC Basic specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200301R
- Detail Specification Reference: 9512003
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

shade in →

Variant Number	Based on Type	Case	Terminal Material and/or Finish	Weight Max g	Total Dose Radiation Level Letter
01	TSC695F	MQFP-F256	G2	15	R [100kRAD(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Shade in →

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to +7	V	1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.5	V	2
Input Current per Signal pin per Power pin	I_{IN}	 -10 to +10 -50 to +50	mAdc	
Output Current	I_{OUT}	-90 to +110	mAdc	3
Device Power Dissipation	P_D	1.5	W	
Operating Temperature	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature	T_{stg}	-65 to +150	°C	
Junction Temperature	T_{Jmax}	165	°C	
Thermal Resistance	$Rth_{(J-C)}$	3	°C/W	
Soldering Temperature	T_{sol}	265	°C	4

NOTES

1. Device is functional for $4.5 \leq V_{DD} \leq 5.5V$ with reference to V_{SS} = 0V.
2. V_{DD} +0.5V shall not exceed +7V.
3. The maximum output current of any single output for a maximum duration of 1 second.
4. Duration 10 seconds maximum at a distrance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

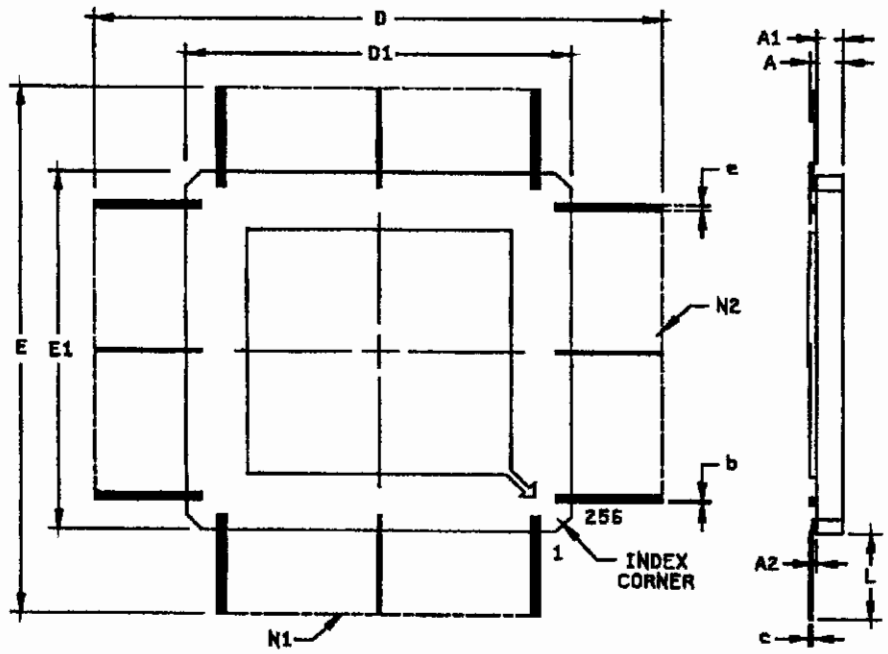
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000 volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 ~~256 Flat Leaded~~ Multilayer Quad Flat Package - (MQFP-F256) - 256 Flat leads



Shade in

Symbols ~~Dimension~~	Dimension mm		Skeleton Notes
	Min	Max	
A	2.41	3.18	
A1	2.06	2.56	
A2	0.05	0.36	
b	0.15	0.25	1
c	0.1	0.2	1
D, E	53.23	55.74	
D1, E1	36.83	37.34	
e	0.508 BSC		1
L	8.2	9.2	1
N1, N2	64		

NOTES

1. All leads
2. Terminal identification is specified by reference to the index corner as shown.

1.9 PIN ASSIGNMENT AND DESCRIPTION

Shade → in

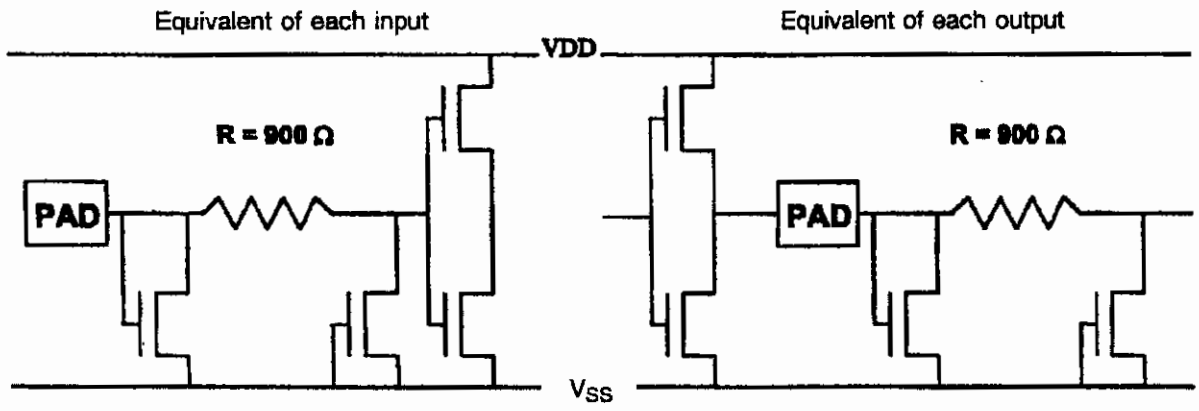
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GPINNT	33	D[20]	65	D[0]	97	RA[18]
2	GPI[7]	34	D[19]	66	RSIZE[1]	98	V_{DDO}
3	V_{DDO}	35	D[18]	67	RSIZE[0]	99	V_{SSO}
4	V_{SSO}	36	V_{DDO}	68	RASI[3]	100	RA[17]
5	GPI[6]	37	V_{SSO}	69	V_{DDO}	101	RA[16]
6	GPI[5]	38	D[17]	70	V_{SSO}	102	RA[15]
7	GPI[4]	39	D[16]	71	RASI[2]	103	V_{DDO}
8	GPI[3]	40	V_{DDI}	72	RASI[1]	104	V_{SSO}
9	V_{DDO}	41	V_{SSI}	73	RASI[0]	105	RA[14]
10	V_{SSO}	42	D[15]	74	RA[31]	106	V_{DDI}
11	GPI[2]	43	D[14]	75	RA[30]	107	V_{SSI}
12	GPI[1]	44	V_{DDO}	76	V_{DDO}	108	RA[13]
13	GPI[0]	45	V_{SSO}	77	V_{SSO}	109	RA[12]
14	D[31]	46	D[13]	78	RA[29]	110	V_{DDO}
15	D[30]	47	D[12]	79	RA[28]	111	V_{SSO}
16	V_{DDO}	48	D[11]	80	RA[27]	112	RA[11]
17	V_{SSO}	49	D[10]	81	V_{DDO}	113	RA[10]
18	D[29]	50	V_{DDO}	82	V_{SSO}	114	RA[9]
19	D[28]	51	V_{SSO}	83	RA[26]	115	V_{DDO}
20	V_{DDI}	52	D[9]	84	RA[25]	116	V_{SSO}
21	V_{SSI}	53	D[8]	85	RA[24]	117	RA[8]
22	D[27]	54	D[7]	86	V_{DDI}	118	RA[7]
23	D[26]	55	D[6]	87	V_{SSI}	119	RA[6]
24	V_{DDO}	56	V_{DDO}	88	V_{DDO}	120	V_{DDO}
25	V_{SSO}	57	V_{SSO}	89	V_{SSO}	121	V_{SSO}
26	D[25]	58	D[5]	90	RA[23]	122	RA[5]
27	D[24]	59	D[4]	91	RA[22]	123	RA[4]
28	D[23]	60	D[3]	92	RA[21]	124	RA[3]
29	D[22]	61	D[2]	93	V_{DDO}	125	V_{DDO}
30	V_{DDO}	62	V_{DDO}	94	V_{SSO}	126	V_{SSO}
31	V_{SSO}	63	V_{SSO}	95	RA[20]	127	RA[2]
32	D[21]	64	D[1]	96	RA[19]	128	RA[1]

Pin	Function	Pin	Function	Pin	Function	Pin	Function
129	RA[0]	161	SYSERR	193	DXFER	225	$\overline{\text{MEMCS[3]}}$
130	V_{DDO}	162	SYSAV	194	$\overline{\text{MEXC}}$	226	V_{DDO}
131	V_{SSO}	163	EXTINT[4]	195	V_{DDO}	227	V_{SSO}
132	RAPAR	164	EXTINT[3]	196	V_{SSO}	228	$\overline{\text{MEMCS[2]}}$
133	RASPAR	165	EXTINT[2]	197	$\overline{\text{RESET}}$	229	$\overline{\text{MEMCS[1]}}$
134	DPAR	166	EXTINT[1]	198	$\overline{\text{SYSRESET}}$	230	$\overline{\text{MEMCS[0]}}$
135	V_{DDO}	167	EXTINT[0]	199	BA[1]	231	V_{DDI}
136	V_{SSO}	168	V_{DDI}	200	BA[0]	232	V_{SSI}
137	SYSCLK	169	V_{SSI}	201	CB[6]	233	$\overline{\text{OE}}$
138	TDO	170	EXTINTACK	202	CB[5]	234	V_{DDO}
139	$\overline{\text{TRST}}$	171	$\overline{\text{IUERR}}$	203	V_{DDO}	235	V_{SSO}
140	TMS	172	V_{DDO}	204	V_{SSO}	236	$\overline{\text{MEMWR}}$
141	TDI	173	V_{SSO}	205	CB[4]	237	$\overline{\text{BUFFEN}}$
142	TCK	174	CPAR	206	CB[3]	238	DDIR
143	CLK2	175	TXA	207	CB[2]	239	V_{DDO}
144	$\overline{\text{DRDY}}$	176	RXA	208	CB[1]	240	V_{SSO}
145	DMAAS	177	RXB	209	V_{DDO}	241	$\overline{\text{DDIR}}$
146	V_{DDO}	178	TXB	210	V_{SSO}	242	$\overline{\text{MHOLD}}$
147	V_{SSO}	179	$\overline{\text{IOWR}}$	211	CB[0]	243	$\overline{\text{MDS}}$
148	$\overline{\text{DMAGNT}}$	180	$\overline{\text{IOSEL[3]}}$	212	$\overline{\text{ALE}}$	244	WDCLK
149	$\overline{\text{EXMCS}}$	181	V_{DDO}	213	V_{DDI}	245	IWDE
150	V_{DDI}	182	V_{SSO}	214	V_{SSI}	246	EWDINT
151	V_{SSI}	183	$\overline{\text{IOSEL[2]}}$	215	$\overline{\text{PROM8}}$	247	TMODE[1]
152	$\overline{\text{DMAREQ}}$	184	$\overline{\text{IOSEL[1]}}$	216	$\overline{\text{ROMCS}}$	248	TMODE[0]
153	$\overline{\text{BUSERR}}$	185	$\overline{\text{IOSEL[0]}}$	217	$\overline{\text{MEMCS[9]}}$	249	DEBUG
154	$\overline{\text{BUSRDY}}$	186	WRT	218	V_{DDO}	250	INULL
155	$\overline{\text{ROMWRT}}$	187	$\overline{\text{WE}}$	219	V_{SSO}	251	DIA
156	$\overline{\text{NOPAR}}$	188	V_{DDO}	220	$\overline{\text{MEMCS[8]}}$	252	V_{DDO}
157	$\overline{\text{SYSHALT}}$	189	V_{SSO}	221	$\overline{\text{MEMCS[7]}}$	253	V_{SSO}
158	$\overline{\text{CPUHALT}}$	190	RD	222	$\overline{\text{MEMCS[6]}}$	254	FLUSH
159	V_{DDO}	191	RLDSTO	223	$\overline{\text{MEMCS[5]}}$	255	INST
160	V_{SSO}	192	LOCK	224	$\overline{\text{MEMCS[4]}}$	256	RTC

Shade in →

Signal	Type	Active	Description	
RA[31-0]	I/O		32-bit registered address bus	Output buffer: 400pF
RAPAR	I/O	High	Registered address bus parity	-
RASI[3-0]	I/O		4-bit registered address space identifier	-
RSIZE[1-0]	I/O		2-bit registered bus transaction size	-
RASPAR	I/O	High	Registered ASI and SIZE parity	-
CPAR	I/O	High	Control bus parity	-
D[31-0]	I/O		32-bit data bus	-
CB[6-0]	I/O		7-bit check-bit bus	-
DPAR	I/O	High	Data bus parity	-
RLDSTO	I/O	High	Registered atomic load-store	-

1.11 PROTECTION NETWORKS



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the applicable ESCC Generic Specification. Permitted deviations from the applicable Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. ~~Consolidated~~ ~~Notes are given after the tables.~~

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22±3°C.

Shade in →

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Functional Test 1	-	3014	V_{IL} = 0.8V, V_{IH1} = 2.2V, V_{IH2} = 3V V_{DD} = 4.5V, V_{SS} = 0V Note 2	-	-	-
Functional Test 2	-	3014	V_{IL} = 0.8V, V_{IH1} = 2.2V, V_{IH2} = 3V V_{DD} = 5V, V_{SS} = 0V Note 2	-	-	-
Functional Test 3	-	3014	V_{IL} = 0.8V, V_{IH} = 2.2V, V_{IH2} = 3V V_{DD} = 5.5V, V_{SS} = 0V Note 2	-	-	-
Low Level Input Current 1	I_{IL1}	3009	V_{IN} = 0V, V_{DD} = 5.5V V_{SS} = 0V Note 3	~~10~~ —	-10	µA
Low Level Input Current 2	I_{IL2}	3009	V_{IN} = 0V, V_{DD} = 5.5V V_{SS} = 0V Note 3	~~250~~ —	-350	µA
High Level Input Current	I_{IH}	3010	V_{IN} = 5.5V, V_{DD} = 5.5V V_{SS} = 0V	-	10	µA
Low Level Output Voltage 1	V_{OL1}	3007	V_{DD} = 4.5V, V_{SS} = 0V, I_{OL} = 4mA Note 4	-	400	mV
Low Level Output Voltage 2	V_{OL2}	3007	V_{DD} = 4.5V, V_{SS} = 0V, I_{OL} = 12mA Note 4	-	400	mV
High Level Output Voltage 1	V_{OH1}	3006	V_{DD} = 4.5V, V_{SS} = 0V, I_{OH} = -6mA Note 4	2.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	V_{DD} = 4.5V, V_{SS} = 0V, I_{OH} = -16mA Note 4	2.4	-	V
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3020	Outputs disabled V_{OUT} = 0V, V_{DD} = 5.5V V_{SS} = 0V	~~10~~ —	-10	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
Output Leakage Current Third State, (High Level Applied)	I_{OZH}	3021	Outputs disabled $V_{OUT} = V_{DD} = 5.5V$ $V_{SS} = 0V$	-	10	µA
Supply Current, (Power Down)	I_{DDPD}	3005	$V_{DD} = 5.5V$, $V_{SS} = 0V$, f = 25MHz V_{DDI} Pins Power Down mode	-	41	mA
Supply Current, (Operating)	I_{DDOP}	3005	$V_{DD} = 5.5V$, $V_{SS} = 0V$, f = 25MHz V_{DDI} Pins	-	230	mA
Input Capacitance	C_{IN}	3012	$V_{DD} = 0V$, $V_{SS} = 0V$ Note 5	-	10	pF
CLK2 period	T_1	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	20	-	ns
SYSCLK Period	T_2	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	40	-	ns
CLK2 High and Low Pulse Width	T_3	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	9.75	-	ns
RA[31-0], RAPAR, RSIZE, RLDSTO and LOCK Output Delay from SYSCLK + Edge	T_4	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 7	-	6.5	ns
$\overline{\text{MEMCS}}$[9-0], $\overline{\text{ROMCS}}$, $\overline{\text{EXMCS}}$ Output Delay from SYSCLK + Edge	T_5	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	-	12.5	ns
DDIR, $\overline{\text{DDIR}}$ Output Delay from SYSCLK + Edge	T_6	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	-	15	ns
$\overline{\text{MEMWR}}$ and $\overline{\text{IOWR}}$ Output Delay from SYSCLK + and SYSCLK-Edge	T_7	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 7	-	23.5	ns
$\overline{\text{OE}}$ High to Low Output Delay from SYSCLK + Edge	T_8	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 7	-	20.5	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-1}	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	11.5	-	ns
Data Setup Time during Load from SYSCLK + Edge	T_{9-2}	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 7, 8	9	-	ns
Data Hold Time during Load from SYSCLK + Edge	T_{10}	3003	$V_{DD} = 4.5$ and 5.5V, $V_{SS} = 0V$ Note 6	5	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions (Note 1)	Limits		Units
				Min	Max	
SYSERR, SYSAV Output Delay from SYSCLK + Edge	T_{49}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	20	ns
$\overline{IUERR}$ Output Delay from SYSCLK + Edge	T_{50}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	20	ns
EXTINT[4-0] Setup Time from SYSCLK- Edge	T_{52}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	12	-	ns
EXTINT[4-0] Hold Time from SYSCLK-Edge	T_{53}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	0	-	ns
EXTINTACK Output Delay from SYSCLK + Edge	T_{54}		V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	15	ns
$\overline{OE}$ Low to High Output Delay from SYSCLK + Edge (no DMA Mode)	T_{56}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	8.5	ns
$\overline{BUFFEN}$ Low to High Output Delay from SYSCLK + Edge	T_{57}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	9	ns
INST Output Delay from SYSCLK + Edge	T_{60}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	-	22	ns
Data Output Delay to Low-Z from SYSCLK + Edge	T_{61}	3003	V_{DD} = 4.5 and 5.5V, V_{SS} = 0V Note 6	20	-	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

NOTES:

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Functional tests shall be performed at each supply voltage with f_{SYSCLK} = 25MHz, $t_r = t_f \leq 5$ns, V_{IL} = 0.8V, V_{IH1} = 2.2V, V_{IH2} = 3V, $V_{OL} \leq$ 1.45V, $V_{OH} \geq$ 1.55V. Functionality per the timing diagram specifed herein shall be verified.

   V_{IH2} applies to inputs RxA/RxB, GPI[7-0], EXTINT[4-0], EWDINT, $\overline{SYSRESET}$. V_{IH1} applies to all other inputs.
3. I_{IL2} applies to inputs $\overline{TRST}$, TMS, TDI. I_{IL1} applies to all other inputs.
4. V_{OL2} and V_{OH2} apply to outputs RA[31-0], $\overline{MEMCS}$[9-0], $\overline{MEMWR}$, $\overline{OE}$. V_{OL1} and V_{OH1} apply to all other outputs.
5. Guaranteed but not tested.

6. Parameter tested go-no-go at each supply voltage during AC testing with f_{SYSCLK} = 25MHz, C_L = 50pF, V_{ref} = 2.5V.
7. Parameter recorded at each supply voltage during AC testing with f_{SYSCLK} = 25MHz, C_L = 50pF, V_{ref} = 2.5V.
8. Parameter tested with following conditions: NOPAR = 0, rpa = rec = 0 or 1 (NOPAR: No Parity Input signal; rpa, rec: bit 13 and 14 of Memory Configuration Register)

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at Tamb = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current 1	I_{IL1}	±0.1	~~-10~~	~~-10~~	µA
High Level Input Current	I_{IH}	±0.1	-	~~10~~	µA
Low Level Output Voltage 1	V_{OL1}	±100	-	400	mV
Low Level Output Voltage 2	V_{OL2}	±100	-	400	mV
High Level Output Voltage 1	V_{OH1}	±0.1	2.4	-	V
High Level Output Voltage 2	V_{OH2}	±0.1	~~2.4~~	-	V
Output Leakage Current Third State, (Low Level Applied)	I_{OZL}	±0.1	~~-10~~ -	~~-~~ -10	µA
Output Leakage Current Third State, (High Level Applied)	I_{OZH}	±0.1	-	~~10~~	µA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Shade in →

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0, -3)	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
Input $\overline{SYSRESET}$	V_{IN}	V_{GEN2} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} per (Note 1)	V
Pulse Voltage	V_{GEN1}, V_{GEN2}	0V to V_{DD}	V
Pulse Frequency ↗ (Square Wave	f_{GEN1} f_{GEN2}	1.65M 50.3 (Note 2) 50±15% Duty Cycle $t_r = t_f \leq 5ns$	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5 (+0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a serial protection resistor/load as follows:

Shade in →

Pin	Signal	Wired to:	Serial Resistor	Pin	Signal	Wired to:	Serial Resistor
1	GPIINT	V_{DD}	5.6kΩ	24	V_{DDO}	V_{DD}	N/A
2	GPI[7]	V_{DD}	1kΩ	25	V_{SSO}	V_{SS}	N/A
3	V_{DDO}	V_{DD}	N/A	26	D[25]	V_{SS}	1kΩ
4	V_{SSO}	V_{SS}	N/A	27	D[24]	V_{SS}	1kΩ
5	GPI[6]	V_{DD}	1kΩ	28	D[23]	V_{DD}	1kΩ
6	GPI[5]	V_{DD}	1kΩ	29	D[22]	V_{SS}	1kΩ
7	GPI[4]	V_{DD}	1kΩ	30	V_{DDO}	V_{DD}	N/A
8	GPI[3]	V_{DD}	1kΩ	31	V_{SSO}	V_{SS}	N/A
9	V_{DDO}	V_{DD}	N/A	32	D[21]	V_{SS}	1kΩ
10	V_{SSO}	V_{SS}	N/A	33	D[20]	V_{DD}	1kΩ
11	GPI[2]	V_{DD}	1kΩ	34	D[19]	V_{DD}	1kΩ
12	GPI[1]	V_{DD}	1kΩ	35	D[18]	V_{SS}	1kΩ
13	GPI[0]	V_{DD}	1kΩ	36	V_{DDO}	V_{DD}	N/A
14	D[31]	V_{DD}	1kΩ	37	V_{SSO}	V_{SS}	N/A
15	D[30]	V_{DD}	1kΩ	38	D[17]	V_{SS}	1kΩ
16	V_{DDO}	V_{DD}	N/A	39	D[16]	V_{SS}	1kΩ
17	V_{SSO}	V_{SS}	N/A	40	V_{DDI}	V_{DD}	N/A
18	D[29]	V_{SS}	1kΩ	41	V_{SSI}	V_{SS}	N/A
19	D[28]	V_{SS}	1kΩ	42	D[15]	V_{SS}	1kΩ
20	V_{DDI}	V_{DD}	N/A	43	D[14]	V_{SS}	1kΩ
21	V_{SSI}	V_{SS}	N/A	44	V_{DDO}	V_{DD}	N/A
22	D[27]	V_{SS}	1kΩ	45	V_{SSO}	V_{SS}	N/A
23	D[26]	V_{DD}	1kΩ	46	D[13]	V_{SS}	1kΩ

Pin	Signal	Wired to:	Serial Resistor	Pin	Signal	Wired to:	Serial Resistor
227	V_{SSO}	V_{SS}	N/A	242	$\overline{MHOLD}$	V_{DD}	5.6kΩ
228	$\overline{MEMCS[2]}$	V_{DD}	5.6kΩ	243	$\overline{MDS}$	V_{DD}	5.6kΩ
229	$\overline{MEMCS[1]}$	V_{DD}	5.6kΩ	244	WDCLK	V_{SS}	1kΩ
230	$\overline{MEMCS[0]}$	V_{DD}	5.6kΩ	245	IWDE	V_{SS}	1kΩ
231	V_{DDI}	V_{DD}	N/A	246	EWDINT	V_{SS}	1kΩ
232	V_{SSI}	V_{SS}	N/A	247	TMODE[1]	V_{SS}	1kΩ
233	$\overline{OE}$	V_{DD}	5.6kΩ	248	TMODE[0]	V_{SS}	1kΩ
234	V_{DDO}	V_{DD}	N/A	249	DEBUG	V_{SS}	1kΩ
235	V_{SSO}	V_{SS}	N/A	250	INULL	V_{DD}	5.6kΩ
236	$\overline{MEMWR}$	V_{DD}	5.6kΩ	251	DIA	V_{DD}	5.6kΩ
237	$\overline{BUFFEN}$	V_{DD}	5.6kΩ	252	V_{DDO}	V_{DD}	N/A
238	DDIR	V_{DD}	5.6kΩ	253	V_{SSO}	V_{SS}	N/A
239	V_{DDO}	V_{DD}	N/A	254	FLUSH	V_{DD}	5.6kΩ
240	V_{SSO}	V_{SS}	N/A	255	INST	V_{DD}	5.6kΩ
241	$\overline{DDIR}$	V_{DD}	5.6kΩ	256	RTC	V_{DD}	5.6kΩ

2. $f_{GEN2} = f_{GEN1} / 2^{15}$.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for power burn-in.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the purchase order.

Shade in →

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	22 ± 3	°C
Input CLK2	V_{IN}	V_{GEN1} (Note 1)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD}, V_{SS} (Note 1)	V
Pulse Voltage	V_{GEN1}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1}	≤100 50±15% Duty Cycle $t_r = t_f \leq 500ns$	Hz
Positive Supply Voltage V_{DDO}, V_{DDI}	V_{DD}	5 (+0.5, -0)	V
Negative Supply Voltage V_{SSO}, V_{SSI}	V_{SS}	0	V

NOTES:

1. All Inputs and Outputs shall be connected through a serial protection resistor/load as defined for burn-in with the exception that Pin 198 $\overline{SYSRESET}$ shall be connected to V_{SS} through 1kΩ serial resistor.