DOCUMENT CHANGE REQUEST

DCR number 124	Changes required for: General	Originator: S Thacker
Date: 2004/06/08	Date sent: 2004/06/08	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS Quad 3-State NOR R/S Latches, based on type 4043B		
Number:	9202/042	Issue:	1

Other documents affected:

Page:

Page 14 Figure 3(c) Circuit Schematic

Paragraph:

Page 14 Figure 3(c) Circuit Schematic

Original wording:

Proposed wording:

Figure is amended to reflect an equivalent NOR Latch (as para 1.8 Functional diagram in amended spec) - see original and amended version as attached.

Justification:

Original figure was incorrect (it was an equivalent NAND Latch)

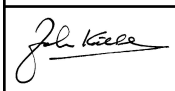
Attachments:

DCR_9202042_pages.pdf, null

Modifications:

N/A

Approval signature:



Date signed:

2004-06-08

FIGURE 3(c) - CIRCUIT SCHEMATIC (EACH LATCH)

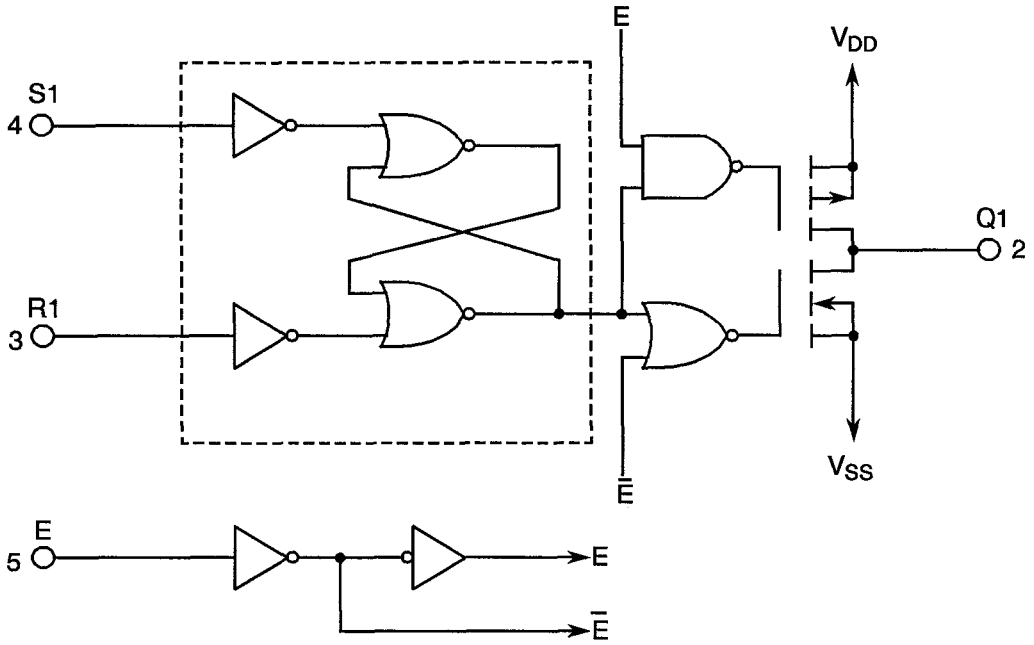
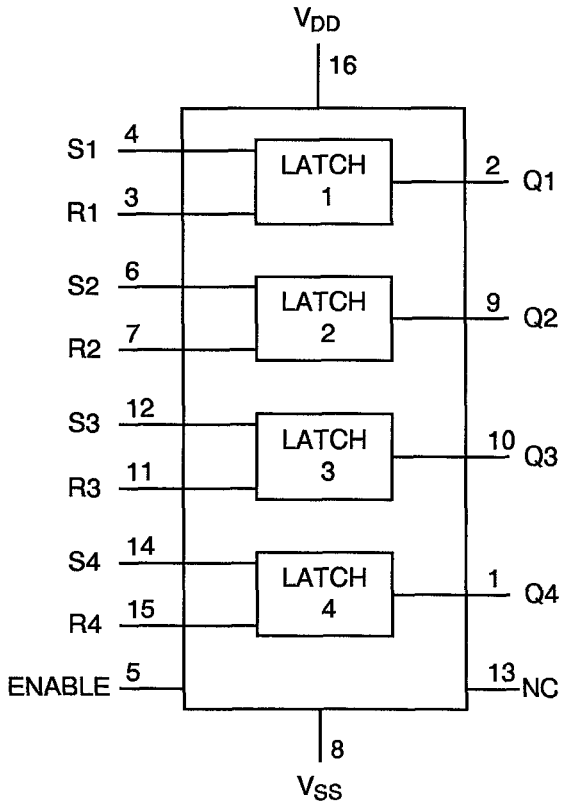


FIGURE 3(d) - FUNCTIONAL DIAGRAM



Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces for flat, dual-in-line and small outline packages.
   16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only

EACH LATCH