DOCUMENT CHANGE REQUEST

DCR number 122	Changes required for: General	Originator: S Thacker
Date: 2004/06/04	Date sent: 2004/06/04	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS Quad Bilateral Switch, based on type 4016B		
Number:	9202/050	Issue:	1

Other documents affected:

Page:

Electrical Test table Table 2 page 23 & Test Circuits Fig 4(p) page 44, Fig 4(q) page 45 - parameters: Propagation times tPLH1, tPLH2, tPHL.

Paragraph:

Electrical Test table Table 2 page 23 & Test Circuits Fig 4(p) page 44, Fig 4(q) page 45 - parameters: Propagation times tPLH1, tPLH2, tPHL.

Original wording:

Proposed wording:

In addition to general changes to the specification format/layout/content for the 4000B series as summarised in ESCC approved DCR90, there are some additional specific technical changes to this specification as follows :

Electrical Test table & circuit (Table 2/Fig 4(p &q) (para 2.3.1/2.3.3 note 8)) - parameters: Propagation times.
Test conditions for channel inputs for tPLH1 (=tPLH), tPHL1 (=tPHL), tPLH2 (=tPZH) have been amended/clarifed for correct switching including definition of load resistance and capacitance RL & CL.
The switching waveforms have been corrected for tPLH2 (=tPZH) in Fig 4(q)(para 2.3.3 note 8).
- see attached sheets for current and new table & fig/note.

Justification:

1), 2), 3) - The current specification is incomplete, unclear or incorrect for these requirements.

Attachments:
DCR_9202050_old_new_ref_pages.pdf, null
Modifications:
N/A
Approval signature:

Date signed:
2004-06-04

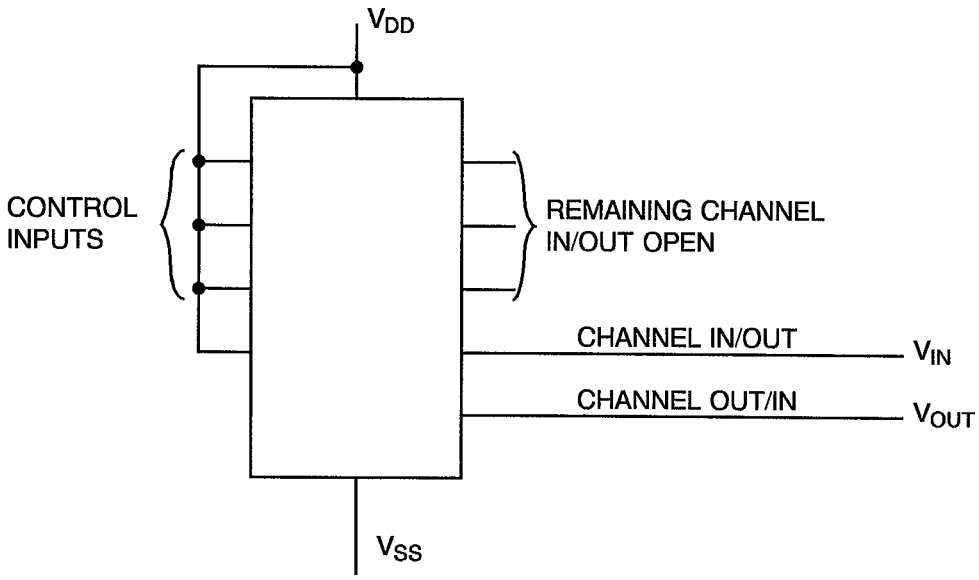
TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
208 to 211	Input Capacitance (Control)	C_{IN}	3012	4(m)	V_{IN} (Not Under Test) = 0Vdc $V_{DD} = V_{SS} = 0$Vdc Note 5 (Pins D/F 5-6-12-13) (Pins C 7-9-17-19)	-	7.5	pF
212 to 215	Channel Capacitance (Input)	C_{INC}	3012	4(n)	$V_{DD} = V_{SS} = 0$Vdc Note 5 (Pins D/F 1-4-8-11) (Pins C 2-6-12-16)	-	7.5	pF
216 to 219	Channel Capacitance (Output)	C_{OC}	3012	4(o)	$V_{DD} = V_{SS} = 0$Vdc Note 5 (Pins D/F 2-3-9-10) (Pins C 4-5-14-15)	-	7.5	pF
220	Propagation Delay Signal IN to Signal OUT (Channel turned ON)	t_{PLH1}	3003	4(p)	V_{IN} (Under Test) = Pulse Generator $V_{DD} = 5$Vdc, $V_{SS} = 0$Vdc Note 6 Pins D/F: 1 to 2 — Pins C: 2 to 4	-	100	ns
221	Propagation Delay Signal IN to Signal OUT (Channel turned ON)	t_{PHL}	3003	4(p)	V_{IN} (Under Test) = Pulse Generator $V_{DD} = 5$Vdc, $V_{SS} = 0$Vdc Note 6 Pins D/F: 1 to 2 — Pins C: 2 to 4	-	100	ns
222	Propagation Delay Time Control to Switch ON	t_{PLH2}	3003	4(q)	V_{IN} (Under Test) = Pulse Generator $V_{DD} = 5$Vdc, $V_{SS} = 0$Vdc Note 6 Pins D/F: 13 to 2 — Pins C: 19 to 4	-	70	ns

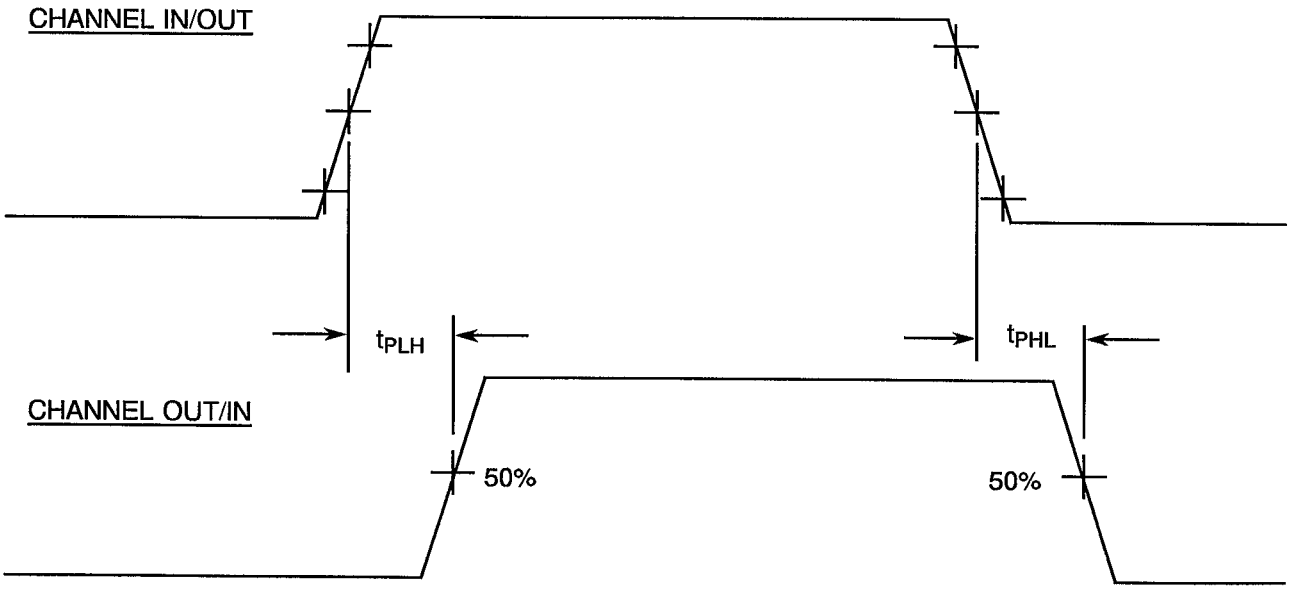
NOTES: See Page 24.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(p) - PROPAGATION DELAY, SIGNAL IN TO SIGNAL OUT



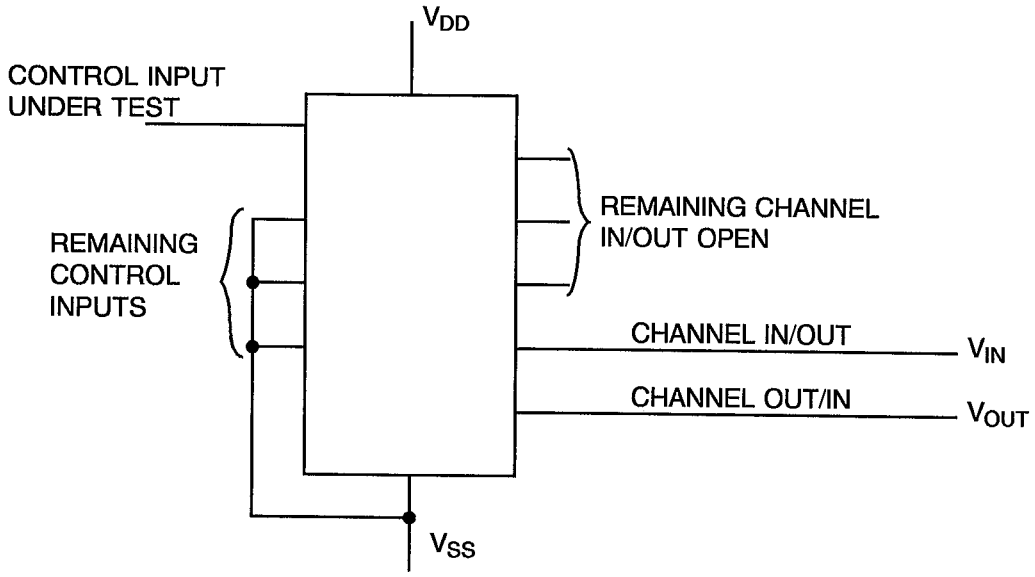
VOLTAGE WAVEFORMS



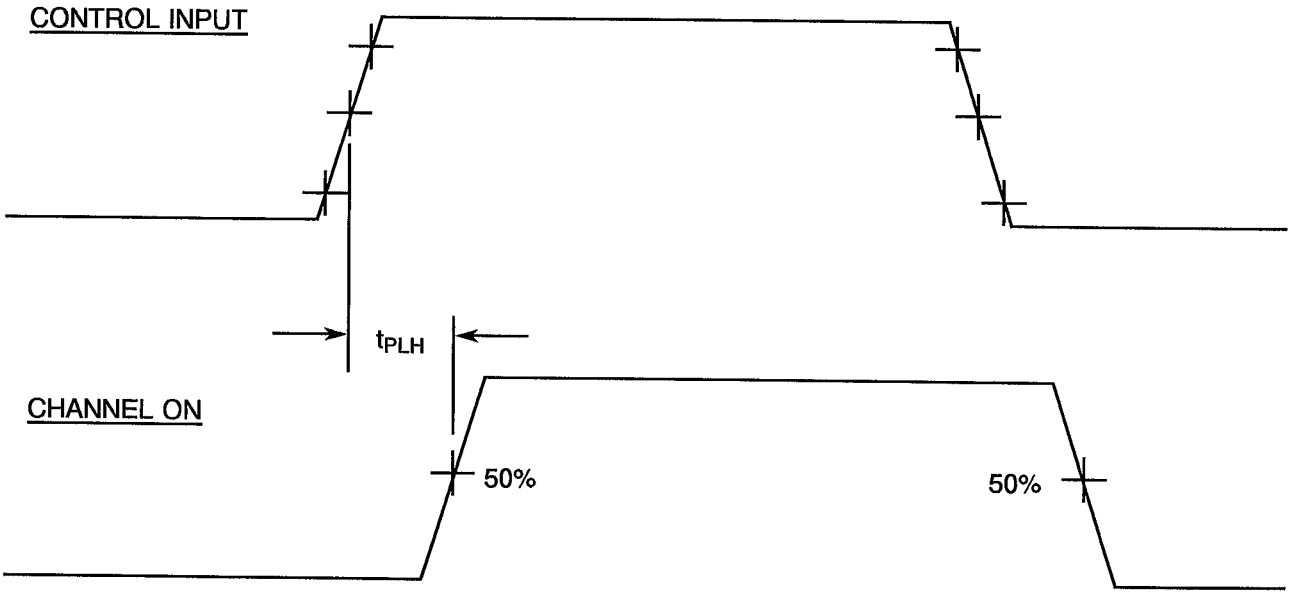
NOTES 1. Pulse Generator - $V_P = 0$ to V_{DD}, t_r and $t_f \leq 15$ns, f = 500KHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(q) - PROPAGATION DELAY, CONTROL TO SWITCH ON



VOLTAGE WAVEFORMS



NOTES 1. Pulse Generator - $V_P = 0$ to V_{DD}, t_r and $t_f \leq 15$ns, f = 500KHz.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Channel Capacitance, B Outputs/Inputs	C_{CHB}	3012	V_{IN} (Not Under Test)=0V V_{DD}= V_{SS}=0V f = 100 kHz to 1 MHz Note 7	-	7.5	pF
Propagation Delay Low to High, 1A to 1B	t_{PLH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, R_L=200kΩ V_{DD}=5V, V_{SS}=0V Note 8	-	100	ns
Propagation Delay High to Low, 1A to 1B	t_{PHL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, R_L=200kΩ V_{DD}=5V, V_{SS}=0V Note 8	-	100	ns
Output Enable Time High Impedance to High Output, 1C to 1B	t_{PZH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{IN}(1A)=5V, R_L=1kΩ V_{DD}=5V, V_{SS}=0V Note 8	-	70	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^{o}C and T_{amb}=- 55(+5-0)^{o}C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-

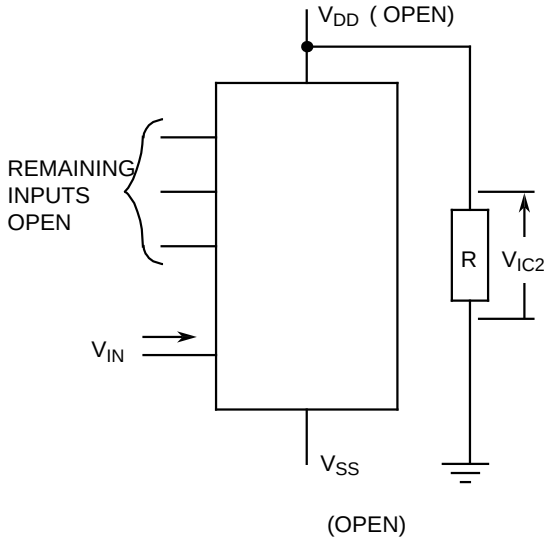
R_{ON4} shall be tested with V_{IN} (A or B) = 1.5V, 3V, 7V, 7.5V, 8V, 8.5V, 9V, 10V

Channel ON Resistance shall be recorded for Channel 1A to 1B and 3A to 3B at each specified V_{IN}. Other channels may be tested go-no-go.

5. Performed as a functional test to verify for all channels V_{OUT} (B) meets the following limits with the specified input conditions V_{IN} (A):

Characteristic	Input Conditions	Limit	Remark
	V_{IN} (A)	V_{OUT} (B)	
V_{IL1}	5V	≤ 0.1V	Channel OFF
V_{IL2}	15V	≤ 0.1V	Channel OFF
V_{IH1}	5V	≥ 4V	Channel ON
V_{IH2}	15V	≥ 12.5V	Channel ON

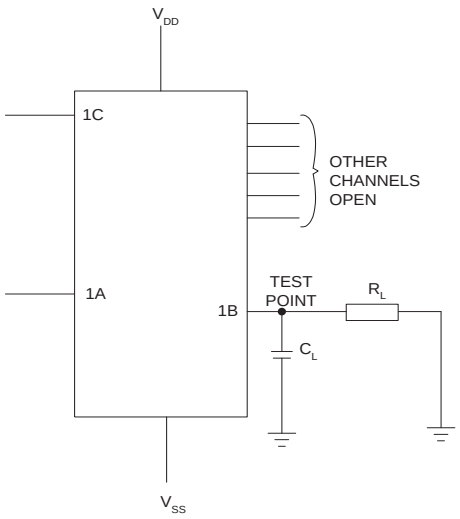
6. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:



7. Guaranteed but not tested.
8. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
The pulse generator shall have the following characteristics:

V_{GEN} = 0 to V_{DD}; f = 500kHz; tr and t_f ≤15 ns (10% to 90%); duty cycle = 50%. Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture. Channel bias resistance R_L = as specified.

Propagation delay times shall be measured as follows:



VOLTAGE WAVEFORMS