DOCUMENT CHANGE REQUEST

DCR number 991	Changes required for: General	Originator: Steve Thacker
Date: 2017/04/19	Date sent: 2016/05/04	Organisation: ESCC Executive Secretariat
Status: IMPLEMENTED		

Title:	Integrated Circuits: Monolithic And Multichip Microcircuits,Wire-Bonded, Hermetically Sealed And		
Number:	9000	Issue:	8

Other documents affected:

Page:

See attached 9000 Draft 9A (Naked Die implementation)(with track changes) for review.docx that details all changes.

Paragraph:

See attached 9000 Draft 9A (Naked Die implementation)(with track changes) for review.docx that details all changes.

Original wording:

See current ESCC9000 issue 8

Proposed wording:

Specification is amended throughout in order to implement changes to add to ESCC9000 the facility to qualify and procure “Naked Die Integrated Circuit components” (in addition to the currently specified “Packaged Integrated Circuit components”). The implementation takes into account the requirements applicable to procurement of active chips in ECSS-Q-ST-60-05C and is made in the same way as applies to ESCC5000 Draft 7C per DCR944.

All changes (both editorial and technical) made to ESCC 9000 issue 8 are identified and detailed in the DCR attachment: ESCC 9000 draft 9A.

Changes are summarised as follows (para numbers refer to ESCC9000 draft 9A):

1) General
Editorial changes necessary to clarify the requirements applicable to existing ‘Packaged Integrated Circuit components’. In addition some other minor editorial changes are made as detailed below.

Note: Apart from item 4 below, there are no technical changes in this DCR that are applicable to the existing ‘Packaged IC components’; all technical changes apply due to the addition of requirements for ‘Naked Die IC components’ to the Generic Specification.
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2) Para 3: Definitions of ‘Naked Die Integrated Circuit’ & ‘Packaged Integrated Circuit’ are specified.
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3) Spec title, Para 1.1, 4.1, 4.1.5.1, 4.3.2, 4.3.3, 4.4, 5.1, 5.2.2, 5.2.3, 5.3.1, 5.3.2, 5.3.4, 5.3.5, 6.1, 6.2.3, 6.4.1, 6.4.1.1, 6.4.2, 6.4.2.1, 6.4.2.2, 7.1.1, 7.1.2.1, 7.1.2.2, 7.4, 7.5, 7.8, 7.9, 8.1, 8.3, 8.4, 8.14.3.1, 9.1,, 9.1.2, 9.2, 9.5, 9.6, 9.8, 9.9,,

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9.9.2,9.10, 10, Charts F1A & F1B, F2B, F3B, F4B: Requirements for Naked Die IC components are added; see attached ESCC9000 draft 9A for details.

Notes on the implementation of Naked Die IC components requirements:

• Para 5.2, 9.5 & Chart F2B: Testing at wafer/die level applicable to Naked Die IC components is specified based on the requirements in ECSS-Q-ST-60-05C Para 8.3.1.

• Para 5.3.1, 6.4.2, 8.3, 8.4, Chart F3B: Sampling and allowed failures requirements for testing of Naked Die IC components (tested on the assembled Packaged Test Sublot samples) is defined based on the user LAT sampling specified in ECSS-Q-ST-60-05C Table 8-2. The tests to be performed on the Naked Die IC Components (Charts F2B Special In-process Controls & F3B Screening Tests) are based on the procurement of active chips requirements in Para 8.3 of ECSS Q ST-60-05C i.e. bondability test & user LAT.

Note: The procurement lot based user LAT 1000h/125°C life test and post life wire pull/shear tests of ECSS-Q-ST-60-05C Para 8.3.3.2.4 are not included as requirements in ESCC9000 Draft 9A on the basis that:
a) As part of ESCC qualification and maintenance of qualification, a 2000h life test is performed on a sample of components every 12 months (i.e. on assembled Naked Die IC components from a Packaged Test Sublot)(the same as for qualified Packaged IC components).

b) Bond pull/shear tests are performed on each lot after assembly of the Packaged Test Sublot samples plus are also performed as part of ESCC qualification and maintenance of qualification on a sample of components that have been subjected to a 2000h life test, every 24 months.

c) The user LAT requirements of ECSS-Q-ST-60-05C should be performed by the hybrid Manufacturer/customer using his own assembly processes (not the die Manufacturer).

• Chart F4B: The qualification and Periodic Testing requirements specified for Naked Die IC components are based on the current requirements for Packaged IC Components (Chart F4A). Any tests that are not relevant to Naked Die IC components are not included in Chart F4B.
The Endurance subgroup periodicity, sampling and Operating Life duration are the same as for Packaged IC components (i.e. 15 max samples for 2000 hours every 12 months).
The sample size of the De-encapsulation subgroup (4 max components from the Endurance subgroup samples) is based on ECSS-Q-ST-60-05C Paras 8.3.2 and 8.3.3.2.4c 8 & 9 and those for Packaged IC components.

• Para 4.3.2, 4.4, 9.1.2, 9.2, 9.5, 9.10: For Naked Die IC components, traceability to the wafer lot applies based on ECSS-Q-ST-60-05C Para 8.3.

• Chart F1B, F2B, F3B, F4B: new charts have been produced specifically for Naked Die IC components in order to make the different requirements applicable to Packaged IC components and Naked Die IC components clear.
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4) Para 9.1.1, 9.6, Chart F3A note 5, & Chart F4A (Thermal Shock): minor corrections.

Justification:

Currently ST, TESAT, as supported by ESA, wish to implement the possibility of Naked Die component qualification and procurement against ESCC5000 (similar to how it has already been implemented in ESCC5010). This DCR proposes to implement Naked Die IC components in the same way to how it is proposed for ESCC5000 (at ESA/PSWG request).

Attachments:

dcr991_modifications_per_9000_draft_9c_(s.thacker_2017_02_15).docx,
9000_draft_9a_(naked_die_implementation)(with_track_changes)_for_review.docx,
9000_draft_9a_(naked_die_implementation)(finalised)_for_review.docx,

Modifications:

The contents of the original DCR991 are replaced in full by the following:

Specification is amended throughout in order to implement changes to add to ESCC9000 the facility to qualify and procure “Die Components” (in addition to the currently specified “Packaged Components”). The die component implementation takes into account the requirements applicable to “procurement of active chips” in ECSS-Q-ST-60-05C Rev.1. and is made in the same way as applies to ESCC5000 Draft 7E per DCR944.

All changes (both editorial and technical) made to ESCC 9000 issue 8 are identified (highlighted yellow) in the DCR attachment: ESCC 9000 draft 9C.

Note: apart from DCR item 4) below, there are no technical changes in this DCR that are applicable to the existing ‘Packaged Components’; all other technical changes apply due to the addition of requirements for ‘Die Components’ to the Generic Specification.

Changes are summarised as follows (para numbers refer to ESCC9000 draft 9C):

1) General
Editorial changes throughout, necessary to clarify & differentiate the requirements applicable to existing ‘Packaged Components’ (see item 3 below and attached ESCC9000 draft 9C).

2) Para 3: Definitions of ‘Die Component’ & ‘Packaged Component’ are specified.

3) Spec title, Para 1.1, 4.1, 4.1.5.1, 4.1.5.2, 4.3.2, 4.3.3, 4.4, 4.5, 4.8, 5.1, 5.2.2, 5.2.3, 5.3.1, 5.3.2, 5.3.4, 5.3.5, 6.1, 6.2.3, 6.4.1, 6.4.1.1, 6.4.2, 6.4.2.1, 6.4.2.2, 7.1.1, 7.1.2.1, 7.1.2.2, 7.4, 7.5, 7.8, 7.9, 8.1, 8.3, 8.4, 8.14.3.1, 8.14.3.2, 9.1, 9.1.2, 9.2, 9.5, 9.7, 9.8, 9.9, 9.9.2, 9.10, 10, Charts F1A & F1B, Chart F2A & F2B, Charts F3A & F3B, Charts F4A & F4B :

Requirements for Die Components are added; see attached ESCC9000 draft 9C for details.

Notes on the implementation of Die Components requirements:

• Para 4.1, 7.4, 8.18, Chart F1B & F4B: a 1000h LVT life test on each wafer lot for Die Components is not required for each die component procurement as is the case in ECSS-Q-ST-60-05C (see below for justification).

Note: The procurement lot based user LAT 1000h/125°C life test and post life wire pull/shear tests of ECSS-Q-ST-60-05C Rev.1 Para 8.3.3.2.4 are not included as requirements in ESCC9000 Draft 9C on the basis that:
a) As part of ESCC qualification and maintenance of qualification, a 2000h life test is performed on samples every 12 months (i.e. on assembled Die Components from a Packaged Test Sublot)(the same as for qualified Packaged Components).
b) Bond pull/shear tests are performed on each lot after assembly of the Packaged Test Sublot samples plus are also performed as part of ESCC qualification, and maintenance of qualification on samples every 24 months.
c) The user LAT requirements of ECSS-Q-ST-60-05C Rev.1 should be performed by the hybrid Manufacturer/customer using his own assembly processes (not the die Manufacturer).

• Para 4.3.2, 4.4, 9.1.2, 9.2, 9.5, 9.10: For Die Components, traceability to the wafer lot applies based on ECSS-Q-ST-60-05C Rev.1 Para 8.3.

• Para 5.2, 9.5 & Chart F2B: Testing at wafer lot/die level applicable to Die Components is specified based on the requirements in ECSS-Q-ST-60-05C Rev.1 Para 8.3.1.

• Para 5.3.1, 6.4.2, 8.3, 8.4 & Chart F3B: Sampling and allowed failures requirements for testing of Die Components (tested on the assembled Packaged Test Sublot samples) is defined based on the user LAT sampling specified in ECSS-Q-ST-60-05C Rev.1 Table 8-2. The tests to be performed on the Packaged Test Sublot samples (Charts F2B Special In-process Controls & F3B Screening Tests) are based on the procurement of active chips requirements in Para 8.3 of ECSS-Q-ST-60-05C Rev.1 i.e. bondability test & user LAT.

• Chart F1B, F2B, F3B, F4B: new charts have been produced specifically for Die Components in order to make the different requirements applicable to Packaged Components and Die Components clear.

• Chart F4B: The qualification and Periodic Testing requirements specified for Die components are based on the current requirements for Packaged Components (Chart F4A). Any tests that are not relevant to Die Components, are not included in Chart F4B.
The Endurance subgroup periodicity, sampling and Operating Life duration are the same as for Packaged Components (e.g. 15 samples of a single type for 2000 hours every 12 months).
The sample size of the De-encapsulation subgroup (e.g. 4 components of a single type) is based on ECSS-Q-ST-60-05C Rev.1 Paras 8.3.2 and 8.3.3.2.4c 8 & 9 (but note that these samples have not been subjected to life testing).

4) Various minor editorial changes for the purposes of consistency & clarification were made (see ESCC 9000 Draft 9C for details):
Para: 2.1, 8.13, 9.1, 9.6, Chart F3A Note 6, Chart F4A (Thermal Shock)

Justification:

Requirements for die components are implemented into ESCC 9000 in the same manner as is currently also in progress per DCR944 for ESCC 5000 under the review and approval of the PSWG.

Approval signature:

Date signed:
2017-04-19