DOCUMENT CHANGE REQUEST

DCR number 944	Changes required for: General	Originator: Steve Thacker
Date: 2017/07/24	Date sent: 2015/07/22	Organisation: ESCC Executive Secretariat
Status: IMPLEMENTED		

Title:	Generic Specification for Discrete Semiconductor Components		
Number:	5000	Issue:	6

Other documents affected:

Page:

See DCR attachment

Paragraph:

See DCR attachment and as below

Original wording:

See ESCC 5000 issue 6

Proposed wording:

Specification is amended throughout in order to implement changes to add to ESCC5000 the facility to qualify and procure “Naked Die Components” (in addition to the currently specified “Packaged Components”). The implementation is made in a similar way as is already included in ESCC 5010 issue 2.

All changes (both editorial and technical) made to ESCC 5000 issue 6 are identified and detailed in the DCR attachment: ESCC 5000 draft 7A.

Changes are summarised as follows (para numbers refer to ESCC5000 draft 7A):

1) General
Editorial changes necessary to clarify the requirements applicable to existing ‘Packaged Components’

Note – there are no technical changes in this DCR that are applicable to the existing ‘Packaged Components’; all technical changes apply due to the addition of requirements for ‘Naked Die Components’ to the Generic Specification.

Note – the specification publishing software is migrated to MSWORD; accordingly some changes in presentation are also present.

2) Para 3: Definitions of ‘Naked Die Components’ & ‘Packaged Components’ are specified.

3) Spec title, Para 1.1, 4.1, 4.1.5.1, 4.3.2, 4.4, 5.2.2, 5.3.1, 5.3.2, 5.3.3, 6.1, 6.4.2, 7.1.1, 7.3, 7.4.2.1, 7.4.2.2, 8.1.1.1, 8.1.2.1, 8.1.2.2, 8.2, 8.5.1, 8.9, 8.20, 9.1.2, 9.2, 9.5, 9.6, 9.7, 9.9, 10, Chart F1B, Chart F2, Chart F3, Chart F4B :

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Requirements for Naked Die Components, equivalent to those in ESCC5010, are added.

Notes on the implementation of Naked Die Components requirements:

• Para 5.2.2, 8.1.1.1, 8.1.2.1, 9.5 & Chart F2: Wafer Screening is only specifically required for Naked Die Components.

• Para 6.4.2.1 & Chart F3: PDA0 = 10%. This indicates the good die yield at 1st electrical; the same PDA value is in ESCC5010.

• Para 6.4.2.2 & Chart F3: PDA1 = 5%. This is the PDA applicable to screening of the Packaged Test Sublot for Naked Die Components. 5% is the same PDA as applied in ESCC5000 for Packaged Components.

• Para 7.4.2.1 & Chart F1B: a 1000hour LVT life test is required for each wafer lot of ESCCQPL Naked Die Components; the same as is in ESCC5010.

• Para 8.20, 8.23 & Chart F3: Solderability and Verification of SoA are not required to be tested during Chart F3 Screening on the Packaged Test Sublot for Naked Die Components.

• Chart F4B: The Endurance subgroup sampling and Operating Life duration applicable to Naked Die Components are based on the requirements specified in ESCC5000 for the Endurance subgroup for Packaged Components (i.e. 15 samples for 2000 hours)

Justification:

ST, TESAT, as supported by ESA, wish to implement the possibility of Naked Die Component qualification and procurement against ESCC5000 (similar to how it has already been implemented in ESCC5010).

Attachments:

5000_issue_7e_(die_implementation)_dcr944_attachment_2017_02_15.docx,
5000_issue_7a_for_review_(s.thacker_2015_07_22)(2).docx,

Modifications:

The contents of the original DCR944 are replaced in full by the following:

Specification is amended throughout in order to implement changes to add to ESCC5000 the facility to qualify and procure “Die Components” (in addition to the currently specified “Packaged Components”). The die component implementation takes into account the requirements applicable to “procurement of active chips” in ECSS-Q-ST-60-05C Rev.1.

All changes (both editorial and technical) made to ESCC 5000 issue 6 are identified (highlighted yellow) in the DCR attachment: ESCC 5000 draft 7E.
Note: Changes per DCR904 are also highlighted (green) in the DCR attachment ESCC 5000 draft 7E.

Note: apart from DCR item 2) & 5) below, there are no technical changes in this DCR that are applicable to the existing 'Packaged Components'; all other technical changes apply due to the addition of requirements for 'Die Components' to the Generic Specification.

Changes are summarised as follows (para numbers refer to ESCC5000 draft 7E):

1) General
Editorial changes throughout, necessary to clarify & differentiate the requirements applicable to existing 'Packaged Components' (see item 4 below and attached ESCC5000 draft 7E).

Note – the specification publishing software is migrated to MSWORD; accordingly some changes in presentation are also present.

2) Para 2.1, 2.2 & 4.5: reference to ESCC 22600 for materials and finishes restrictions is added (ref to ECSS-Q-ST-70-02 is deleted from Para 2.2 & 4.5).

3) Para 3: Definitions of 'Die Component' & 'Packaged Component' are specified.

4) Spec title, Para 1.1, 4.1, 4.1.5.2, 4.3.2, 4.3.3, 4.4, 4.5, 4.7, 5.2.2, 5.2.3, 5.3.1, 5.3.2, 6.1, 6.2.3, 6.4.1, 6.4.1.1, 6.4.2, 6.4.2.1, 6.4.2.2, 7.1.1, 7.3, 7.4, 7.7, 7.8, 8.1.1.1, 8.1.2, 8.2, 8.5.1, 9.1, 9.1.2, 9.2, 9.5, 9.7, 9.8, 9.8.2, 9.9, 10, Charts F1A & F1B, Chart F2, Charts F3A & F3B, Charts F4A & F4B : Requirements for Die Components are added; see attached ESCC5000 draft 7E for details.

Notes on the implementation of Die Components requirements:

• Para 4.1, 7.4, 8.18, Chart F1B & F4B: a 1000h LVT life test on each wafer lot for Die Components is not required for each die component procurement as is the case in ECSS-Q-ST-60-05C (see below for justification).

Note: The procurement lot based user LAT 1000h/125°C life test and post life wire pull/shear tests of ECSS-Q-ST-60-05C Rev.1 Para 8.3.3.2.4 are not included as requirements in ESCC5000 Draft 7E on the basis that:
a) As part of ESCC qualification and maintenance of qualification, a 2000h life test is performed on 15 components every 12 months (i.e. on assembled Die Components from a Packaged Test Sublot)(the same as for qualified Packaged Components).
b) Bond pull/shear tests are performed on each lot after assembly of the Packaged Test Sublot samples plus are also performed on 4 components as part of ESCC qualification, and maintenance of qualification every 24 months.
c) The user LAT requirements of ECSS-Q-ST-60-05C Rev.1 should be performed by the hybrid Manufacturer/customer using his own assembly processes (not the die Manufacturer).

• Para 4.3.2, 4.4, 9.1.2, 9.2, 9.5, 9.9: For Die Components, traceability to the wafer lot applies based on ECSS-Q-ST-60-05C Rev.1 Para 8.3.

• Para 5.2, 9.5 & Chart F2: Testing at wafer lot/die level applicable to Die Components is specified based on the requirements in ECSS-Q-ST-60-05C Rev.1 Para 8.3.1.

• Para 5.3.1, 6.4.2, 8.5.1, 8.5.2 & Chart F3B: Sampling and allowed failures requirements for testing of Die Components (tested on the assembled Packaged Test Sublot samples) is defined based on the user LAT sampling specified in ECSS-Q-ST-60-05C Rev.1 Table 8-2. The tests to be performed on the Packaged Test Sublot samples (Charts F2 Special In-process Controls & F3B Screening Tests) are based on the procurement of active chips requirements in Para 8.3 of ECSS-Q-ST-60-05C Rev.1 i.e. bondability test & user LAT.

• Chart F1B, F3B, F4B: new charts have been produced specifically for Die Components in order to make the different requirements applicable to Packaged Components and Die Components clear.

• Chart F4B: The qualification and Periodic Testing requirements specified for Die components are based on the current requirements for Packaged Components (Chart F4A). Any tests that are not relevant to Die Components, are not included in Chart F4B.
The Endurance subgroup periodicity, sampling and Operating Life duration are the same as for Packaged Components (i.e. 15 samples for 2000 hours every 12 months).
The sample size of the De-encapsulation subgroup (4 components) is based on ECSS-Q-ST-60-05C Rev.1 Paras 8.3.2 and 8.3.3.2.4c 8 & 9 (but note that these samples have not been subjected to life testing).

5) Para 8.11 & 8.12: HTRB Burn-in & Power Burn-in.
The requirements for MOSFET are clarified/specified (was: “as specified in the Detail Specification”).
i.e.
HTRB Burn-in: per MIL-STD-750 TM1042 Condition A for 168h min/264h max.
Power Burn-in: per MIL-STD-750 TM1042 Condition B for 48h min.

6) Various minor editorial changes for the purposes of consistency & clarification were made (see ESCC 5000 Draft 7E for details):
Para: 4.1.5.1, 8.3, 8.7, 8.9.2, 8.13, 8.14.1, Chart F3A

Justification:

ST, TESAT, as supported by ESA, wish to implement the possibility of Die Component qualification and procurement against ESCC5000.

The changes contained in this DCR and ESCC 5000 Draft 7E have been discussed and agreed by the PSWG.

Approval signature:

Date signed:

2017-07-24