	ESC	C		DC	CUMENT	CHANGE REQUEST			
DCR number	611	Changes required for: Ge			eral	Originator: S Jeffery			
Date: 2010/05	5/26 Date sent: 2010/05/26					Organisation: CNES			
Status: IMPLEMENTED									
Title:	HCMOS Quad Bilateral Switch, based on type 54HC4066								
Number:	9408/052 Issue:			2					
Other documents affected:									
Page:									
Paragraphs 2.3.1, 2.3.2, 2.3.3 and Appendix A									
Paragraph:									
Paragraphs 2.3.1, 2.3.2, 2.3.3 and Appendix A									
Original wording:									
Proposed wordi	ng:								
Para. 2.3.1, Ch	aracteristic "Channel	ON Resistan	ce Matching	, 1", 0	delete the followi	ng from the Test Conditions:			
VIN(C)=3.15V IIN(A or B)=100µA VDD=4.5V, VSS=0V									
Para. 2.3.1, Characteristic "Channel ON Resistance Matching 2", delete the following from the Test Conditions:									
VIN(C)=4.2V IIN(A or B)=100µA VDD=6V, VSS=0V									
Para. 2.3.2, add "Channel ON Resistance Matching 1" and "Channel ON Resistance Matching 2" (per Para. 2.3.1, as modified above) between "Channel ON Resistance 2" and "Input Clamp Voltage 1".									
Para. 2.3.3, Note 4, add the following under "RON2 is performed with VIS=1V, 3V and 5V":									
"Channel ON Resistance Matching shall be calculated as follows: The results of the Channel ON Resistance measurements of each Channel's Input/Output and Output/Input shall be compared and shall not exceed the specified Limits."									

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Status: IMPLEMEN	NTED								
Appendix 'A', add "The Channel ON Resistance Matching (1 and 2) calculations are not performed." as the first of the agreed "Deviations from High and Low Temperatures Electrical Measurements" and "Deviations from Room Temperature Electrical Measurements".									
Justification:									
The proposed changes will clarify the Channel ON Resistance Matching tests and will also make it clear that STMicroelectronics do not perform the Channel ON Resistance Matching calculations.									
Attachments:									
N/A									
Modifications:									
Add the following to 'Justification': STMicroelectronics' test programme does not include Channel ON Resistance Matching. The matching test was never implemented prior to ESCC because Note 2 of the original (ESA/SCC) Detail Spec stated " Channel ON resistance matching may be calculated and the maximum limits are guaranteed.". However, STMicroelectronics' engineering team performed Channel ON Resistance Matching calculations (using the									
results of the Channel ON Resistance Test) as part of Qualification Testing. These results showed that the actual Channel ON Resistance Matching was <10 Ohms, well within the spec limit of ± 20 Ohms maximum.									
Approval signature:									
R.C. Hari-+									
Date signed:									

2010-05-26