DOCUMENT CHANGE REQUEST

DCR number 195	Changes required for: N/A	Originator: P. Griffin
Date: 2005/07/26	Date sent: 2005/07/26	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register with 3-State Outputs,		
Number:	9306/025	Issue:	1

Other documents affected:

Page:

Table 5(c) - Conditions for Burn-in Dynamic, Page 50

Paragraph:

Table 5(c) - Conditions for Burn-in Dynamic, Page 50

Original wording:

Proposed wording:

No 6 Input Pin D/F15, C17 VIN VGEN2No 7 Input Pin D/F10, C12 VIN VGEN1

Justification:

To correct error in issue 1. Input to Clock pin should be the highest frequency (confirmed by manufacturer STM)

Attachments:

N/A

Modifications:

N/A

Approval signature:

Date signed:

2005-07-26