DOCUMENT CHANGE REQUEST

DCR number 155	Changes required for: General	Originator: S Jeffery
Date: 2005/01/26	Date sent: 2005/01/26	Organisation: ESA/ESTEC
Status: IMPLEMENTED		

Title:	CMOS Quad 2-Input NAND-Gate with Schmitt Trigger Inputs, based on type 4093B		
Number:	9409/002	Issue:	1

Other documents affected:

Page:

Table 6 on Page 44

Paragraph:

Table 6 on Page 44

Original wording:

Proposed wording:

Quiescent Current Change Limit was + or -50nA; change within Intermediate and Endpoint Electrical Measurements to + or -75nA during the conversion (which is currently in progress) of this detail spec to "full" ESCC format per DCR 90.

Justification:

?50nA conflicts with the Quiescent Current Change Limit in the Parameter Drift Values Table (?75nA) - these Change Limits should be identical. In addition a similar device which has the same Room Temperature Electrical Measurement limit for Quiescent Current as this device (40106B, Detail Specification No. 9409/005), has Change Limits of ?75nA rather than ?50nA.

Attachments:

N/A

Modifications:

N/A

Approval signature:

Date signed:

2005-01-26