



DOCUMENT CHANGE REQUEST

DCR number	1249	Changes required for:	General	Originator:	Steve Thacker
Date:	2019/03/25	Date sent:	2019/03/18	Organisation:	ESCC Executive Secretariat
Status:	IMPLEMENTED				

Title: CMOS Quad Low to High 3-State Voltage Level Shifter, based on type 40109B

Number: 9407/003 Issue: 4

Other documents affected:

Page:

6, 14, 28, 29

Paragraph:

1.5, 2.3, 2.6, 2.7

Original wording:

In order to respond to the corrective action for the Manufacturers (ST) internal notice on observed glitches at the output of the level shifter part 40109B
i.e.: update of the detail specification ESCC 9407/003 with an appropriate power-on sequence

Accordingly, add the following:

Para 1.5, Max Ratings: add new note 2 to Supply Voltage:

Note 2. For correct functioning, the components supply voltages shall be turned on in the following sequence:
: VCC shall be fully established before VDD is applied.

Paras. 2.3: Electrical Measurements, 2.6: HTRB, & 2.7: Power Burn-in: Add the following sentence:
See Para 1.5 Note 2 for the required power-on sequence.

Proposed wording:

Justification:



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Attachments:

N/A

Modifications:

N/A

Approval signature:

Date signed:

2019-03-25