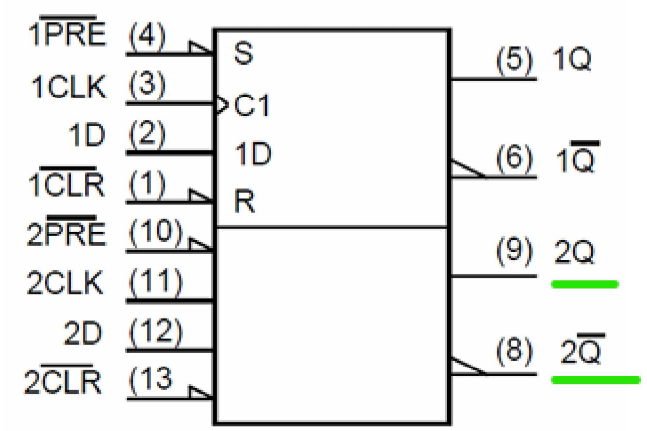
1.8 FUNCTIONAL DIAGRAM

Pin/Pad numbers relate to FP, DIP packages and Die.



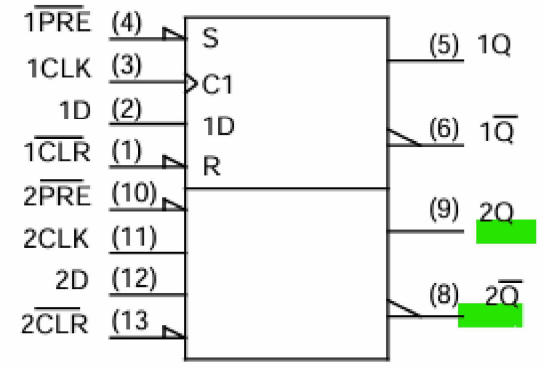

**NOTES:**

1. The package lid for all packages is not connected to any terminal.

1.9 PIN/PAD ASSIGNMENT

| Pin /Pad | Function | Pin /Pad | Function |
|---|---|---|---|
| 1 | 1$\overline{CLR}$ Input (Clear) | 8 | 2Q Output |
| 2 | 1D Input (Data) | 9 | 2$\overline{Q}$ Output |
| 3 | 1CLK Input (Clock) | 10 | 2$\overline{PRE}$ Input (Preset) |
| 4 | 1$\overline{PRE}$ Input (Preset) | 11 | 2CLK Input (Clock) |
| 5 | 1Q Output | 12 | 2D Input (Data) |
| 6 | 1$\overline{Q}$ Output | 13 | 2$\overline{CLR}$ Input (Clear) |
| 7 | $V_{SS}$ | 14 | $V_{DD}$ |






1.9 PIN ASSIGNMENT

| Pin | Function | | Pin | Function | |
|---|---|---|---|---|---|
| | FP, DIP and SO | CCP | | FP, DIP and SO | CCP |
| 1 | 1 $\overline{Clear}$ | - | 11 | 2 Clock | - |
| 2 | 1 Data Input | 1 $\overline{Clear}$ | 12 | 2 Data Input | 2$\overline{Q}$ Output |
| 3 | 1 Clock | 1 Data Input | 13 | 2 $\overline{Clear}$ | 2Q Output |
| 4 | 1 $\overline{Preset}$ | 1 Clock | 14 | $V_{DD}$ | 2 $\overline{Preset}$ |
| 5 | 1Q Output | - | 15 | - | - |
| 6 | 1$\overline{Q}$ Output | 1 $\overline{Preset}$ | 16 | - | 2 Clock |
| 7 | $V_{SS}$ | - | 17 | - | - |
| 8 | 2$\overline{Q}$ Output | 1Q Output | 18 | - | 2 Data Input |
| 9 | 2Q Output | 1$\overline{Q}$ Output | 19 | - | 2 $\overline{Clear}$ |
| 10 | 2 $\overline{Preset}$ | $V_{SS}$ | 20 | - | $V_{DD}$ |

1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2. ↑=Transition, Low to High, ↓=Transition, High to Low.