European Space Components Coordination

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TRANSISTORS, SWITCHING, PNP

BASED ON TYPE 2N3637

ESCC Detail Specification No. 5208/003

as applicable

Issue ~~2~~ 3 - Draft A	~~April 2008~~

Document Custodian: European Space Agency - see https://escies.org

as applicable

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
tbd	Specification up issued to incorporate editorial and technical changes per DCR.

at $T_{case} \leq +25°C$

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	175	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	175	V	
Emitter-Base Voltage	V_{EBO}	-5	V	
Collector Current	I_C	1	A	Continuous
Power Dissipation	P_{tot1}	1	W	At $T_{amb} \leq +25°C$
	P_{tot2}	5	W	Note 1
Operating Temperature Range	T_{op}	-65 to +200	°C	Note 1
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note 1
Soldering Temperature	T_{sol}	+265	°C	Note 2

See attached

NOTES:

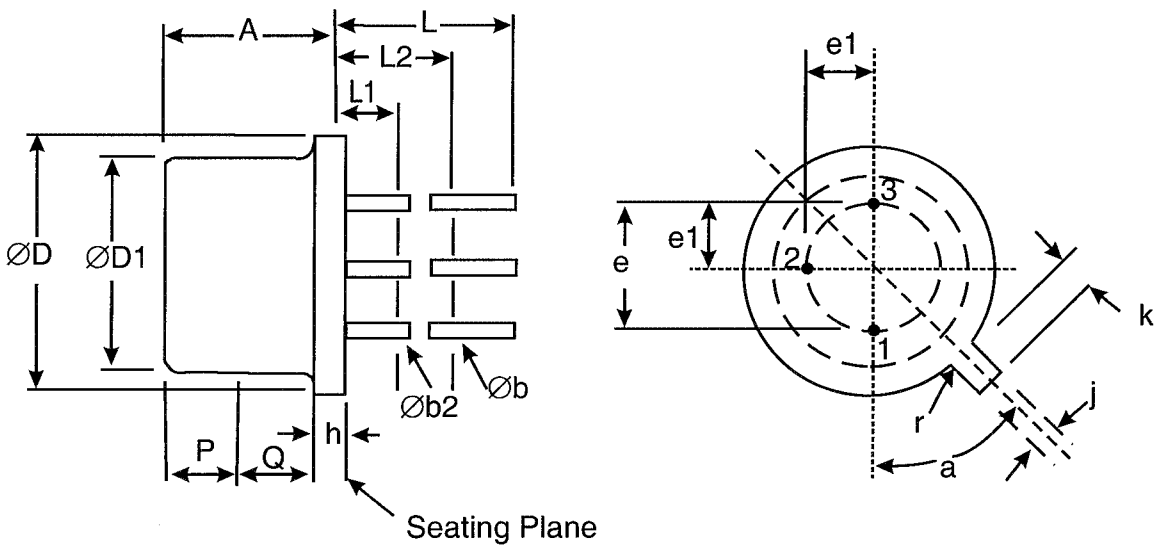
~~1. For $T_{amb} > +25°C$, derate linearly to 0W at +200°C.~~

1. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125°C$ shall be carried out in a 100% inert atmosphere.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND LEAD IDENTIFICATION

Consolidated notes are given following the case drawings and dimensions.

1.6.1 Metal Can Package (TO-5) - 3 lead



Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	175	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	35	°C/W	