

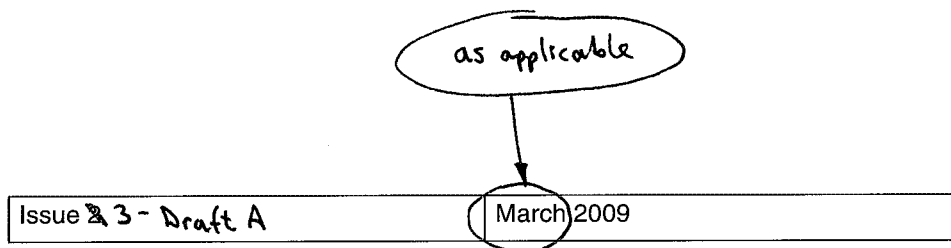


Pages 1 to 15

TRANSISTORS, LOW POWER, NPN

BASED ON TYPE 2N3501

ESCC Detail Specification No. 5201/013





as applicable

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
● 322	Specification up issued to incorporate editorial and technical changes per DCR.

tbd

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CB0}	150	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CE0}	150	V	
Emitter-Base Voltage	V_{EB0}	6	V	
Collector Current	I_C	300	mA	
Power Dissipation	P_{tot1}	1	W	At $T_{amb} \leq +25^{\circ}C$ Note 1
	P_{tot2}	5	W	At $T_{case} \leq +25^{\circ}C$ Note 1
Operating Temperature Range	T_{op}	-65 to +200	$^{\circ}C$	Note 1 & 2
Storage Temperature Range	T_{stg}	-65 to +200	$^{\circ}C$	Note 1 & 2
Soldering Temperature	T_{sol}	+260	$^{\circ}C$	Note 2

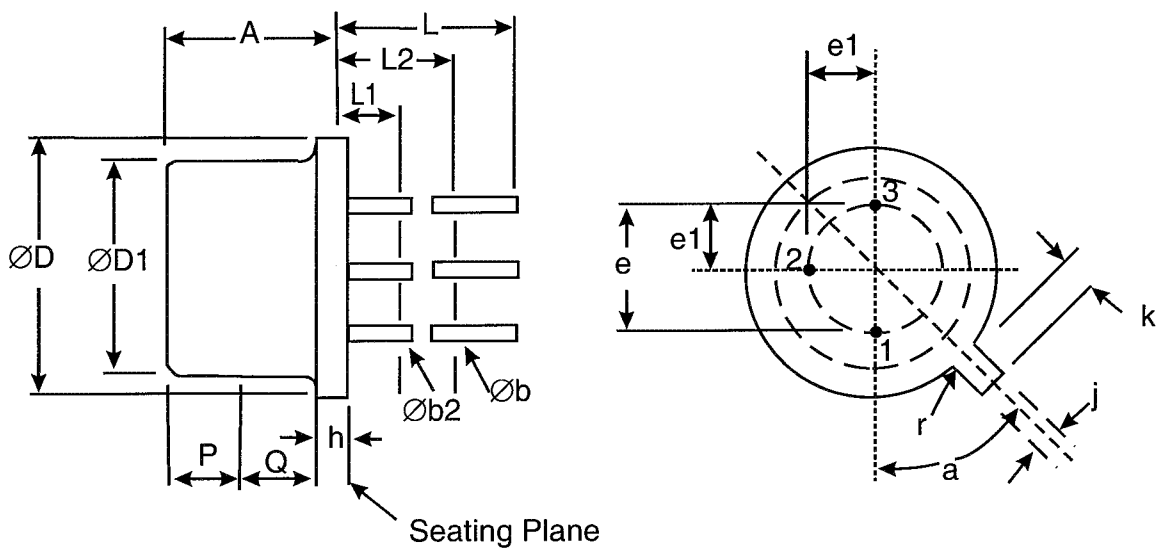
see attached

NOTES:

- ~~1. For T_{amb} or $T_{case} > +25^{\circ}C$, derate linearly to 0W at $+200^{\circ}C$.~~
1. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at $T_{amb} > +125^{\circ}C$ shall be carried out in a 100% inert atmosphere.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.6.1 Metal Can Package (TO-5) - 3 lead



Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	175	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	35	$^{\circ}\text{C}/\text{W}$	