

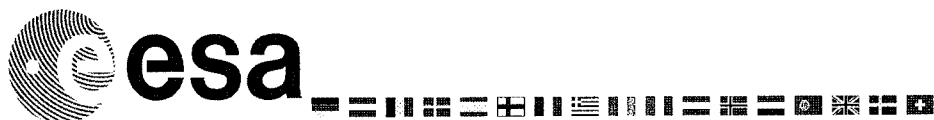
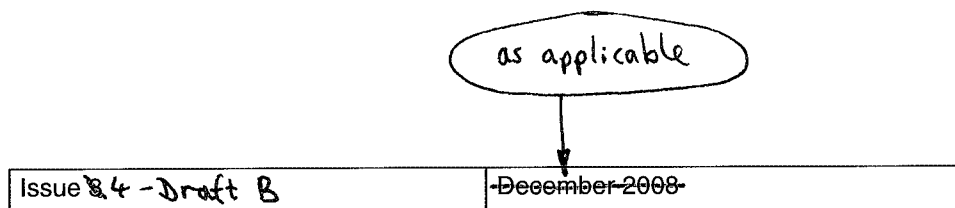


Pages 1 to 17

## TRANSISTORS, LOW POWER, NPN

BASED ON TYPE 2N2222A

ESCC Detail Specification No. 5201/002



Document Custodian: European Space Agency - see <https://escies.org>



as applicable

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**DOCUMENTATION CHANGE NOTICE**

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DCR No.	CHANGE DESCRIPTION
<del>421-447</del>	Specification up issued to incorporate editorial and technical changes per DCR.

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Variant Number	Based on Type	Case	Lead/Terminal Material and/or Finish	Weight max g	V <sub>(BR)CEO</sub> min V	I <sub>hfe</sub>
11	2N2222A	CCP (4 Terminal)	2	0.06	40	3 to 10
12	2N2222A	CCP (4 Terminal)	4	0.06	40	3 to 10

The lead/terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5

MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V <sub>CBO</sub>	75	V	Over entire operating temperature range
Collector-Emitter Voltage	V <sub>CEO</sub>		V	
Variants 01 to 05, 11, 12 Variants 06 to 10		40 50		
Emitter-Base Voltage	V <sub>EBO</sub>	6	V	
Collector Current	I <sub>C</sub>	800	mA	Continuous
Power Dissipation For TO-18 and CCP	P <sub>tot1</sub>	0.5	W	At T <sub>amb</sub> ≤ +25°C *Note 1
<del>For CCP</del>	<del>P<sub>tot2</sub></del>	<del>0.73 (Note 2)</del>	<del>W</del>	<del>At T<sub>amb</sub> ≤ +25°C</del>
For TO-18	P <sub>tot2</sub>	1.8	W	At T <sub>case</sub> ≤ +25°C *Note 1
Operating Temperature Range	T <sub>op</sub>	-65 to +200	°C	Note 2
Storage Temperature Range	T <sub>stg</sub>	-65 to +200	°C	Note 2
Soldering Temperature For TO-18	T <sub>sol</sub>	+260	°C	Note 3
For CCP		+245		

NOTES:

1. For T<sub>amb</sub> or T<sub>case</sub> > +25°C, derate linearly to 0W at +200°C.
2. When mounted on a 15 x 15 x 0.6mm ceramic substrate.
2. For Variants with tin-lead plating or hot solder dip lead finish all testing performed at T<sub>amb</sub> > +125°C shall be carried out in a 100% inert atmosphere.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1. Thermal Resistance, Junction-to-Case only applies to TO-18 packaged Variants.

see attached

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Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	350	°C/W	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	97.2	°C/W	Note 1

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	$I_{CBO}$	3036	$T_{amb}=+150(+0-5)^{\circ}C$ $V_{CB}=60V$ , Bias Condition D	-	10	$\mu A$
Forward-Current Transfer Ratio 2	$h_{FE2}$	3076	$T_{amb}=-55(+5-0)^{\circ}C$ $V_{CE}=10V$ $I_C=10mA$	35	-	-

1. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb}=+22 \pm 3^{\circ}C$ . The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements. The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Collector-Base Cut-off Current	$I_{CBO}$	$\pm 5$ or (1) $\pm 100\%$	-	10	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$\pm 30$ or (1) $\pm 15\%$	-	300	mV
Forward-Current Transfer Ratio 3	$h_{FE3}$	$\pm 15\%$	100	300	-

**NOTES:**

1. Whichever is the greater referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at  $T_{amb}=+22 \pm 3^{\circ}C$ . The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements. The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	$I_{CBO}$	-	10	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	300	mV
Forward-Current Transfer Ratio 3	$h_{FE3}$	100	300	-

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+20 to +50	°C
Power Dissipation	$P_{tot}$	As per Maximum Ratings. <i>operate at the chosen <math>T_{amb}</math> using the</i>	W
Collector-Base Voltage	$V_{CB}$	10 to 40	V

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

*Derate*

*specified  $R_{th(j-a)}$ .*

P      APPENDIX 'A'      S -  
AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control-Chart F2	<p>Special In-process Control Internal Visual Inspection. For CCP packages the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.</p>
Deviations from Room Temperature Electrical Measurements	<p>All AC characteristics (Room Temperature Electrical Measurement Note 2) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
Deviations from High and Low Temperatures Electrical Measurements	<p>All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
Deviations from Screening Tests - Chart F3	<p>Solderability is not applicable unless specifically stipulated in the Purchase Order.</p>