INTEGRATED CIRCUITS, SILICON MONOLITHIC, LOW POWER, CMOS 128K X 8 ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY WITH THREE STATE OUTPUTS

BASED ON TYPE 65608E

ESCC Detail Specification No. 9301/047

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DCR No.	CHANGE DESCRIPTION
	Specification upissued to incorporate editorial and technical changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930104701

- Detail Specification Reference: 9301047
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Access Time (ns)	Case	Lead/Terminal Material and Finish	Weight max g
01	65608E-45	45	MDIL32	G2	4.1
02	65608E-45	45	MFP-F32	G2	2.7
03	65608E-30	30	MDIL32	G2	4.1
04	65608E-30	30	MFP-F32	G2	2.7

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.3	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.5 to V_{DD} +0.3	V	Notes 1, 2
Input Current per Signal Pin per Power Pin	I_{IN}	 ±10 ±50	mAdc	
Output Current (Low)	I_O	±20	mAdc	Note 3
Device Power Dissipation (Continuous)	P_D	1	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+260	^oC	Note 4
Junction Temperature	T_j	+175	^oC	
Thermal Resistance	$R_{th(j-c)}$	3	$^oC/W$	

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional for $4.5V \leq V_{DD} \leq 5.5V$ and for $-0.5V \leq V_{IL} \leq 0.8V$; $2.2V \leq V_{IH} \leq V_{DD} +0.3V$.
2. V_{DD} +0.3V shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

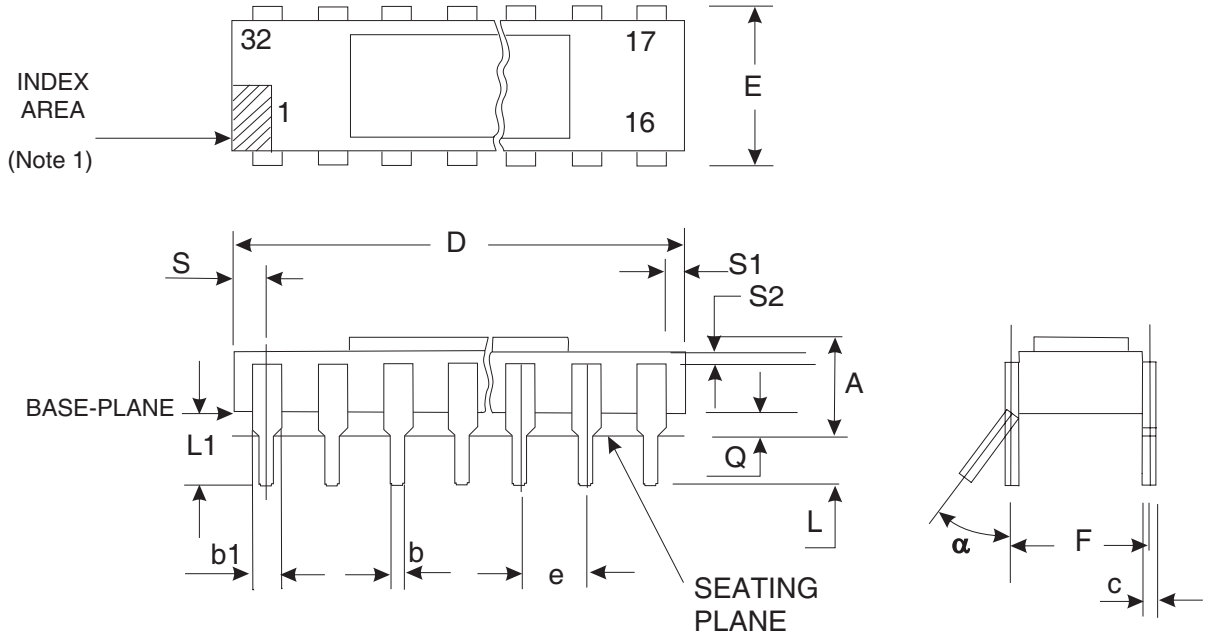
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

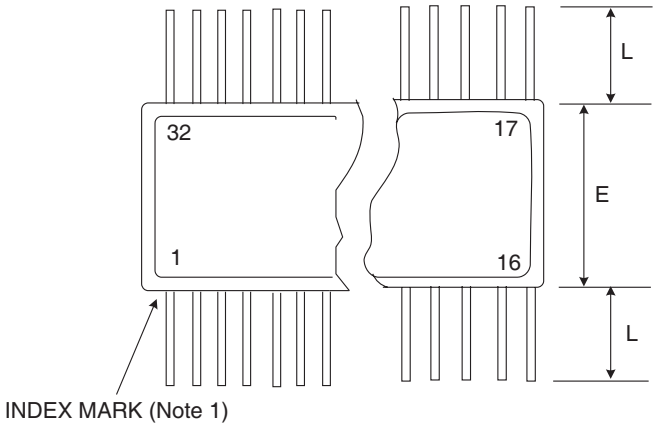
Consolidated Notes are given following the case drawings and dimensions.

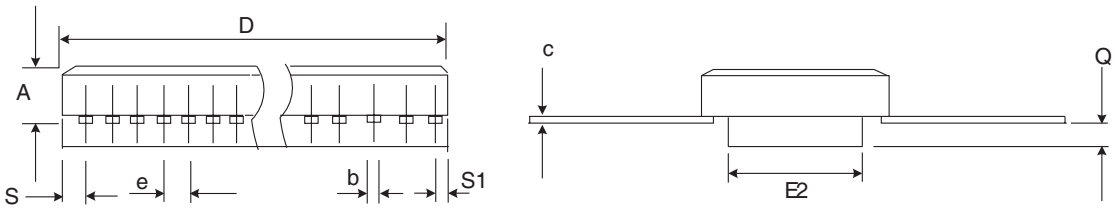
1.7.1 Multilayer Ceramic Dual-in-line Package (MDIL32) - 32 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.92	4.32	5
b	0.4	0.51	2
b1	0.96	1.65	2
c	0.23	0.3	2
D	40.13	41.15	
E	10.16	10.67	
F	9.9	10.41	6
e	2.54 BSC		2, 3
L	3.43	4.2	2, 5
L1	4.44	5.72	2
Q	1.02	1.52	2
S	-	1.65	8
S1	0.13	-	8
S2	0.13	-	2
α	0^o	15^o	2

1.7.2 Flat Leaded Multilayer Flat Package (MFP-F32) - 32 Lead





Symbols	Dimensions mm		Notes
	Min	Max	
A	1.78	2.72	
b	0.38	0.48	2
c	0.076	0.15	2
D	20.62	21.03	7
E	10.26	10.57	7
E2	6.96	7.26	
e	1.27 BSC		2, 4
L	7.37	7.87	2
Q	0.51	0.76	2, 9
S	-	1.14	8
S1	0	-	8

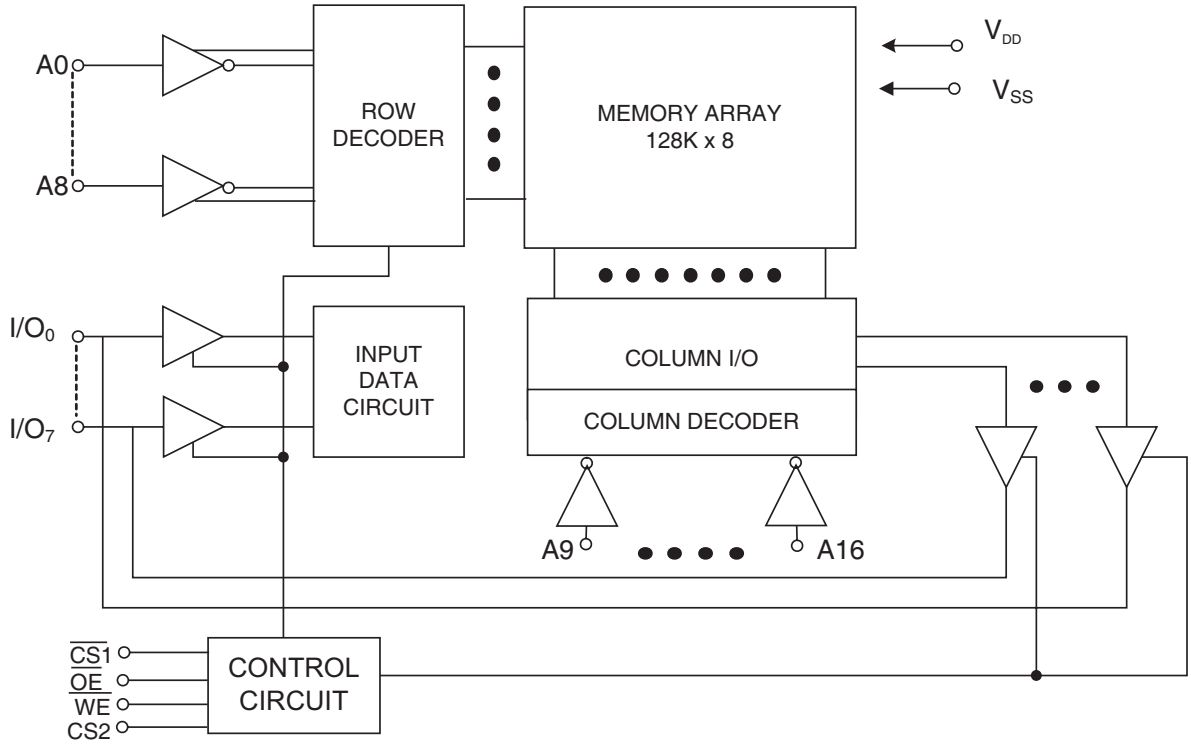
1.7.3 Notes to Physical Dimensions and Terminal Identification

1. Index mark: a notch or terminal 1 identification mark for MFP-F32 package shall be located adjacent to terminal 1 and for MDIL32 shall be in the shaded area.
2. All terminals.
3. 30 places. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. 30 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin

number.

5. Dimensions are measured with the package seated in a seating plane gauge.
6. Dimensions are measured with the leads constrained to be perpendicular to the base plane.
7. This dimension allows for package edge anomalies caused by material protrusions, such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.
   The corner shape (square, notch, radius etc.) may vary at the manufacturer's option from that shown on the drawing.
8. Two places.
9. Dimension shall be measured at the point of exit of the lead from the body.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function
1	Not Connected
2	A16 Input (Address)
3	A14 Input (Address)
4	A12 Input (Address)
5	A7 Input (Address)
6	A6 Input (Address)
7	A5 Input (Address)

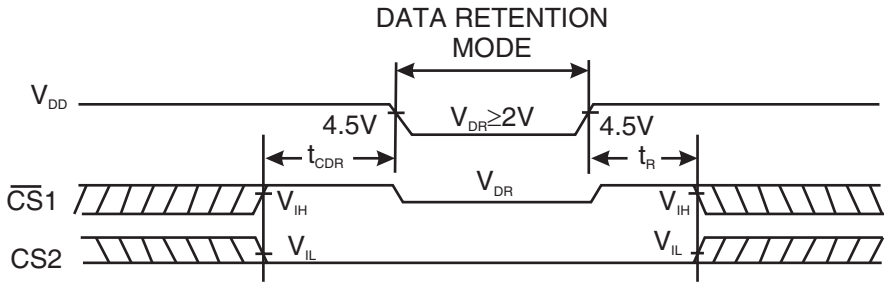
Pin	Function
8	A4 Input (Address)
9	A3 Input (Address)
10	A2 Input (Address)
11	A1 Input (Address)
12	A0 Input (Address)
13	I/O0 Input/Output (Data)
14	I/O1 Input/Output (Data)
15	I/O2 Input/Output (Data)
16	V_{SS}
17	I/O3 Input/Output (Data)
18	I/O4 Input/Output (Data)
19	I/O5 Input/Output (Data)
20	I/O6 Input/Output (Data)
21	I/O7 Input/Output (Data)
22	$\overline{CS}1$ Input (Chip Select)
23	A10 Input (Address)
24	$\overline{OE}$ Input (Output Enable)
25	A11 Input (Address)
26	A9 Input (Address)
27	A8 Input (Address)
28	A13 Input (Address)
29	$\overline{WE}$ Input (Write Enable)
30	CS2 Input (Chip Select)
31	A15 Input (Address)
32	V_{DD}

1.10 TRUTH TABLE AND TIMING DIAGRAMS

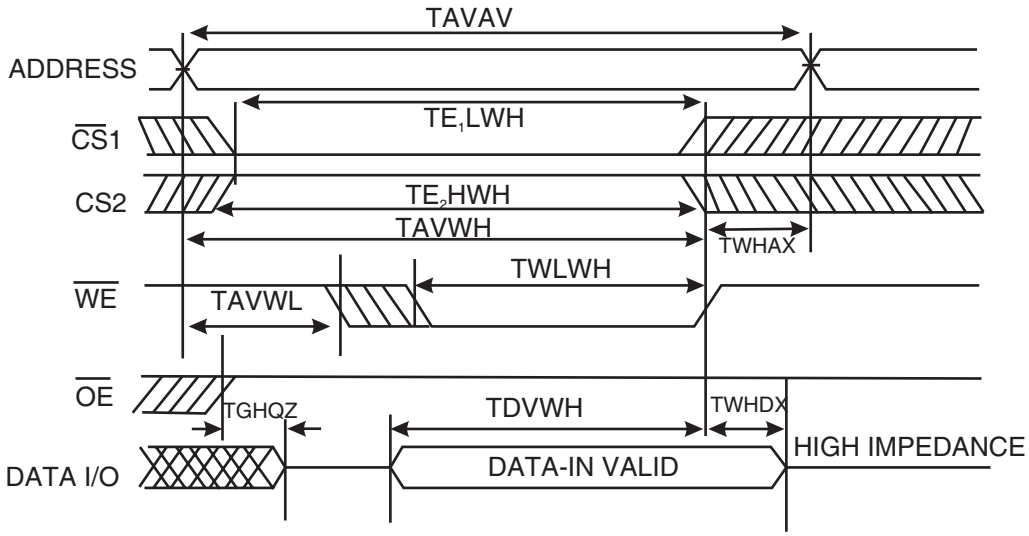
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant and Z = High Impedance.

Inputs				Inputs/Outputs	Mode
$\overline{CS}1$	CS2	$\overline{WE}$	$\overline{OE}$	I/On	
H	X	X	X	Z	Deselected/Power Down
X	L	X	X	Z	Deselected/Power Down
L	H	H	L	Data out	Read
L	H	L	X	Data in	Write
L	H	H	H	Z	Output Disable

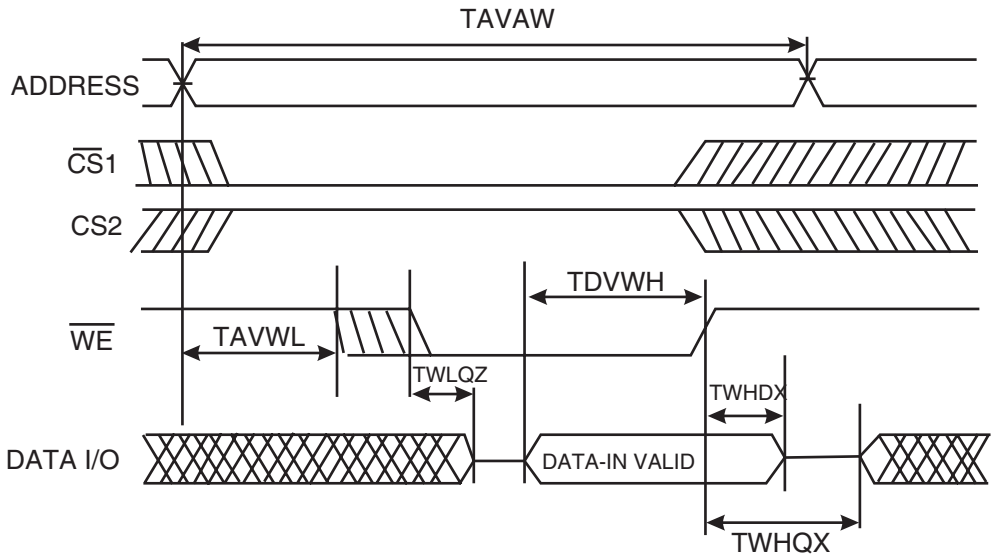
Data Retention



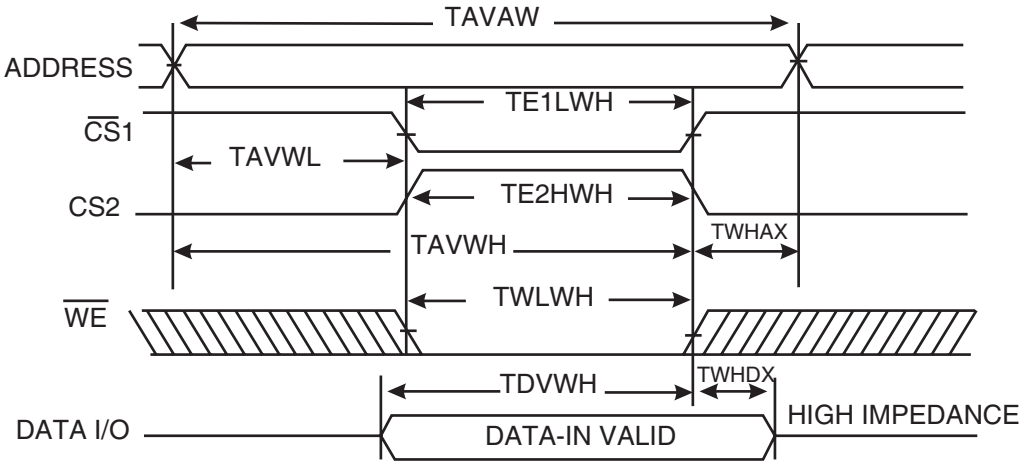
Write Cycle 1: $\overline{WE}$ controlled, $\overline{OE}$ High during Write (Note 1)



Write Cycle 2 : $\overline{WE}$ controlled , $\overline{OE}$ Low (Note 1)



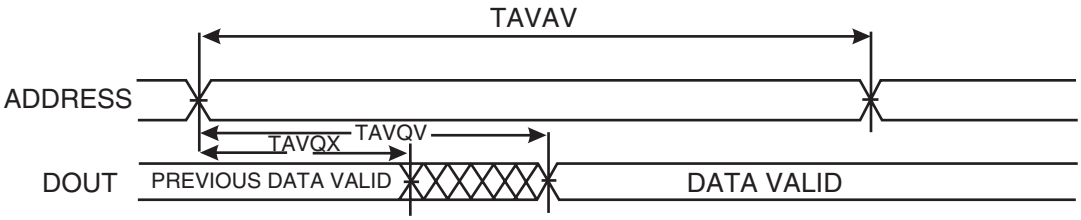
Write Cycle 3 : $\overline{CS1}$ or CS2 controlled (Note 1)



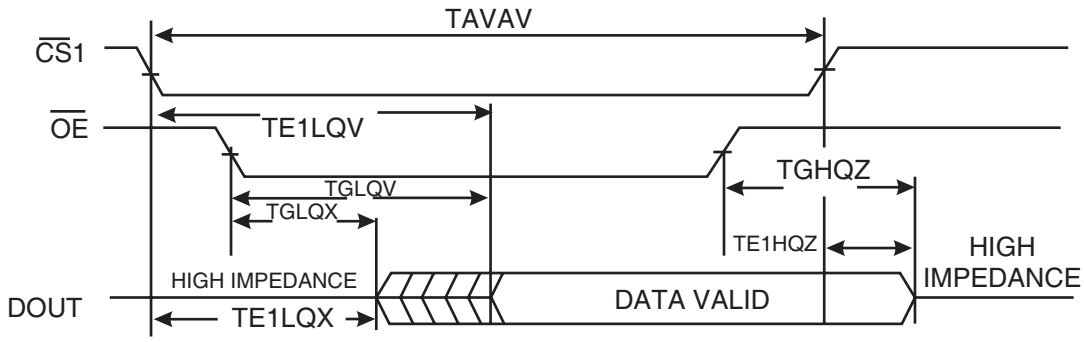
NOTES:

The internal write time of the memory is defined by the overlap of $\overline{CS1}$ Low and CS2 High and $\overline{WE}$ Low. Both signals must be activated to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

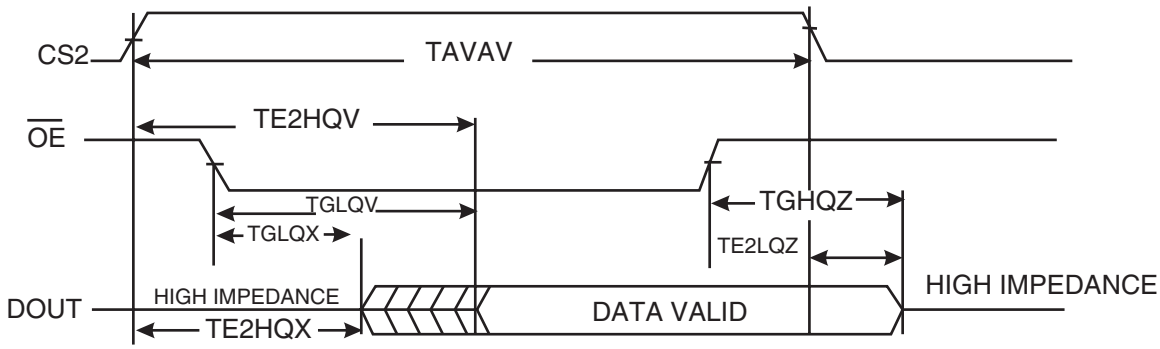
Read Cycle 1



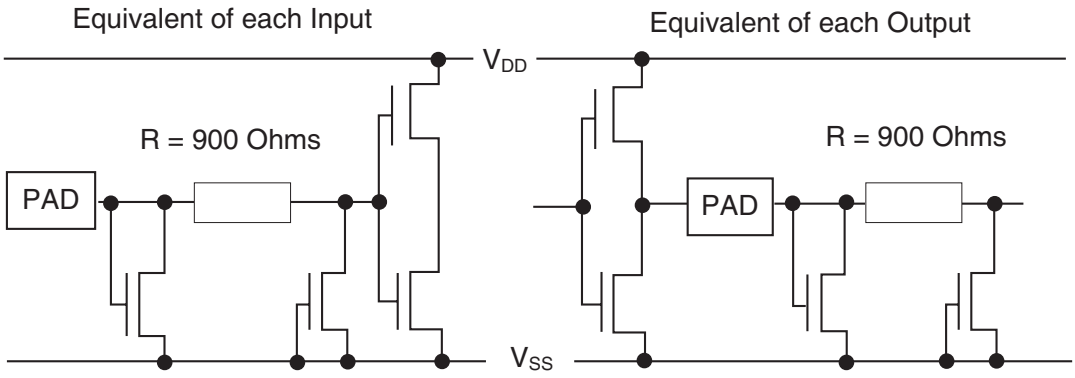
Read Cycle 2



Read Cycle 3



1.11 PROTECTION NETWORKS



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests-Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 4	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage, to V_{SS}	V_{IC}	3008	I_{IN} (Under Test)= -100µA All Other Pins Open V_{DD}= Open,V_{SS}=0V	-0.2	-2	V
Low Level Input Current	I_{IL}	3009	V_{IN}(Under Test)=0V V_{IN}(Remaining Inputs)=5.5V V_{DD}=5.5V, V_{SS}=0V	-	-1	µA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=5.5V V_{IN} (Remaining Inputs)=0V V_{DD}=5.5V, V_{CC}=5.5V	-	1	µA
Output Leakage Current, Third State, Low Level Applied 1	I_{OZL1}	3020	$V_{IN}(\overline{CS}1)$=5V V_{IN}(CS2)=0V V_{IN}(Output)=0V V_{DD}=5.5V, V_{SS}=0V	-	-1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Leakage Current, Third State, Low Level Applied 2	I_{OZL2}	3020	$V_{IN}(\overline{CS}1)$=0V V_{IN}(CS2)=5V $V_{IN}(\overline{WE}, \overline{OE})$=5V V_{IN}(Output)=0V V_{DD}=5.5V, V_{SS}=0V	-	-1	µA
Output Leakage Current, Third State, High Level Applied 1	I_{OZH1}	3021	$V_{IN}(\overline{CS}1)$=5V V_{IN}(CS2)=0V V_{IN}(Output)=5.5V V_{DD}=5.5V, V_{SS}=0V	-	1	µA
Output Leakage Current, Third State, High Level Applied 2	I_{OZH2}	3021	$V_{IN}(\overline{CS}1)$=0V V_{IN}(CS2)=5V, $V_{IN}(\overline{WE}, \overline{OE})$=5V V_{IN}(Output)=5.5V V_{DD}=5.5V, V_{SS}=0V	-	1	µA
Low Level Output Voltage	V_{OL}	3007	V_{IL}=0.8V, V_{IH}=2.2V I_{OL}=8mA V_{DD}=4.5V, V_{SS}=0V Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	V_{IL}=0.8V, V_{IH}=2.2V I_{OH}=-4mA V_{DD}=4.5V, V_{SS}=0V Note 4	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	3005	V_{IL}=0.8V, V_{IH}=2.2V $V_{IN}(\overline{CS}1)$=2.2V V_{IN}(CS2)=0.8V f=0Hz V_{DD}=5.5V, V_{SS}=0V Note 5	-	2	mA
Stand-by Supply Current 2	I_{DDSB2}	3005	V_{IL}=0.8V, V_{IH}=2.2V $V_{IN}(\overline{CS}1)$=5.2V V_{IN}(CS2)=0V f=0Hz V_{DD}=5.5V, V_{SS}=0V Note 5	-	300	µA
Dynamic Operating Supply Current	I_{DDOP}	3005	$V_{IN}(\overline{WE}, \overline{OE}$, CS2)=2.2V $V_{IN}(\overline{CS}1)$=0.8V V_{IN}(Remaining Inputs)=0.2V I_{OUT}=0A V_{DD}=5.5V, V_{SS}=0V Variants 01, 02 f=22.2MHz Variants 03, 04 f=33.3MHz	 - -	 100 130	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Data Retention Current	I_{DDDR}	3005	$V_{IN}(\overline{CS}1)$=1.8V V_{IN}(CS2)=0.2V V_{IN}(Remaining Inputs)=0.2V and 1.8V V_{DD}=2V, V_{SS}=0V Notes 5, 6	-	150	µA
Data Retention Test	-	-	Note 6	-	-	-
Input Capacitance	C_{IN}	3012	V_{IN} =V_{SS}=0V V_{DD}= 0V f= 1MHz Note 7	-	8	pF
Output Capacitance	C_{OUT}	3012	V_{IN} =V_{SS}=0 V_{DD}= 0V f= 1MHz Note 7	-	8	pF
Read Cycle Time	t_{AVAV}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 45 30	 - -	ns
Address Access Time	t_{AVQV}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9 Variants 01, 02 Variants 03, 04	 - -	 45 30	ns
Output Change from Address Time	t_{AVQX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8	5	-	ns
Write Cycle Time	t_{AVAW}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 45 30	 - -	ns
Address Set-up Time	t_{AVWL}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8	0	-	ns
Address Valid to End of Write	t_{AVWH}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 35 22	 - -	ns
Data Setup Time	t_{DVWH}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9 Variants 01, 02 Variants 03, 04	 20 18	 - -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Chip Select 1 Low to End of Write	t_{E1LWH}	3003	V_{CC}=4.5V & 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 35 22	 - -	ns
Chip Select 2 High to End of Write	t_{E2HWH}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 35 22	 - -	ns
Write Enable Low Output Disable Time	t_{WLQZ}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10 Variants 01, 02 Variants 03, 04	 - -	 15 8	ns
Write Enable Low Pulse Width	t_{WLWH}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9 Variants 01, 02 Variants 03, 04	 35 22	 - -	ns
Address Hold from End of Write Time	t_{WHAX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 8	0	-	ns
Data Hold Time	t_{WHDX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9	0	-	ns
Write Enable High Output Enable Time	t_{WHQX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10	0	-	ns
Chip Select 1 Access Time	t_{E1LQV}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9 Variants 01, 02 Variants 03, 04	 - -	 45 30	ns
Chip Select 1 Low Output Enable Time	t_{E1LQX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10	3	-	ns
Chip Select 1 High Output Disable Time	t_{E1HQZ}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10 Variants 01, 02 Variants 03, 04	 - -	 20 15	ns
Chip Select 2 Access Time	t_{E2HQV}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 9 Variants 01, 02 Variants 03, 04	 - -	 45 30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Chip Select 2 High Output Enable Time	t_{E2HQX}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10	3	-	ns
Chip Select 2 Low Output Disable Time	t_{E2LQZ}	3003	V_{DD}=4.5V & 5.5V V_{SS}=0V Note 10 Variants 01, 02 Variants 03, 04	 - -	 20 15	ns
Output Enable Access Time	t_{GLQV}	3003	V_{DD}=4.5V and 5.5V V_{SS}=0V Note 8 Variants 01, 02 Variants 03, 04	 - -	 15 12	ns
Output Enable Low Output Enable Time	t_{GLQX}	3003	V_{DD}=4.5V and 5.5V V_{SS}=0V Note 10	0	-	ns
Output Enable High Output Disable Time	t_{GHQZ}	3003	V_{DD}=4.5V and 5.5V V_{SS}=0V Note 10 Variants 01, 02 Variants 03, 04	 - -	 15 8	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not

under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.

2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	105	4.5 & 5.5	0	0	3	0.5	-0.5	1.5
Checkerboard	105	4.5 & 5.5	0	0	3	0.5	-0.5	1.5
Imag	105	4.5 & 5.5	0	0	3	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (mV)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	105	5.5	0	-300	5.8	0.5	-0.5	1.5
March	105	4.5	0	-300	4.8	0.5	-0.5	1.5
March	105	5.5	0	0	2.2	0.5	-0.5	1.5
March	105	4.5	0	800	3	0.5	-0.5	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	105	4.5	0	0	3	8	-4	Note (b)
Genbl	105	4.5	0	0	3	0.5	-0.5	1.5

FUNCTIONAL TEST 4

Pattern	Timing (ns) Note (a)		V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
	Variant								
	01, 02	03, 04							
March/Comarch	115	90	4.5	0	0	3	0.5	-0.5	1.5
Imag/Checkerboard	115	90	4.5	0	0	3	0.5	-0.5	1.5
March/Comarch	115	90	4.5	0	0	3	0.5	-0.5	1.5
Imag/Checkerboard	115	90	4.5	0	0	3	0.5	-0.5	1.5

(a) A write cycle is followed by a read cycle. The time between start of write and start of read per the truth table is the specified timing parameter. $t_r = t_f \leq 5$ns.

(b) 0.4V for low output level, 2.4V for high output level.

(c) Output load 1 TTL gate equivalent $+C_L < 30$pF.

3. Select address inputs to produce a low level at the pin under test.
4. Select address inputs to produce a high level at the pin under test.
5. Measurements shall be performed with the memory loaded with a background of zeros, then with a

background of ones, for all inputs High, then Low. Only the worst case shall be recorded.

6. Data retention procedure:
   (a) Write memory at V_{DD} = 4.5V with Checkerboard pattern with V_{IL} = 0V and V_{IH} = 3V.
   (b) Power down to V_{DD} = 2V for 250ms, $V_{IN}(\overline{CS}1)$=1.8V or V_{IN}(CS2)=0.2V.
   (c) Restore V_{DD} to 4.5V, wait t_R(operation recovery time), read memory and compare with original pattern.
   (d) Repeat the procedure with $\overline{\text{Checkerboard}}$ pattern.
   (e) t_R = 45ns for Variants 01 and 02, t_R =30ns for Variants 03 and 04.
   (f) During power up and power down transitions, $V_{IN}(\overline{CS}1) \geq V_{DD}$-0.2V or V_{IN}(CS2) $\leq$ 0.2V, V_{IN}(Remaining Inputs) $\leq$ 0.2V or $\geq V_{DD}$-0.2V.
7. Guaranteed but not tested.
8. Measurements shall be performed, on a go-no-go basis, during Functional Test 4.
9. Measurements shall be performed during Functional Test 4 using March pattern at 4.5V and 5.5V.
10. Guaranteed but not tested with an output loading of 5pF.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125(+0-5)°C and T_{amb}=-55(+5-0)°C. The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current, Third State, Low Level Applied 1	I_{OZL1}	±0.1	-	-1	µA
Output Leakage Current, Third State, Low Level Applied 2	I_{OZL2}	±0.1	-	-1	µA
Output Leakage Current, Third State, High Level Applied 1	I_{OZH1}	±0.1	-	1	µA
Output Leakage Current, Third State, High Level Applied 2	I_{OZH2}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	±0.2	-	2	mA

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Stand-by Supply Current 2	I_{DDSB2}	±30	-	300	µA
Data Retention Current	I_{DDDR}	±15	-	150	µA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods, test conditions and limits shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits		Units
		Min	Max	
Functional Test 1	-	-	-	-
Functional Test 2	-	-	-	-
Functional Test 3	-	-	-	-
Input Clamp Voltage, to GND	V_{IC}	-	300	µA
Low Level Input Current	I_{IL}	-	-1	µA
High Level Input Current	I_{IH}	-	1	µA
Output Leakage Current, Third State, Low Level Applied 1	I_{OZL1}	-	-1	µA
Output Leakage Current, Third State, Low Level Applied 2	I_{OZL2}	-	-1	µA
Output Leakage Current, Third State, High Level Applied 1	I_{OZH1}	-	1	µA
Output Leakage Current, Third State, High Level Applied 2	I_{OZH2}	-	1	µA
Low Level Output Voltage	V_{OL}	-	400	mV
High Level Output Voltage	V_{OH}	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	-	2	mA
Stand-by Supply Current 2	I_{DDSB2}	-	300	µA
Dynamic Operating Supply Current Variants 01, 02 Variants 03, 04	I_{CCOP}	 - -	 100 130	mA
Data Retention Current	I_{DDDR}	-	150	µA
Data Retention Test	-	-	-	-

2.6 POWER BURN-IN CONDITIONS

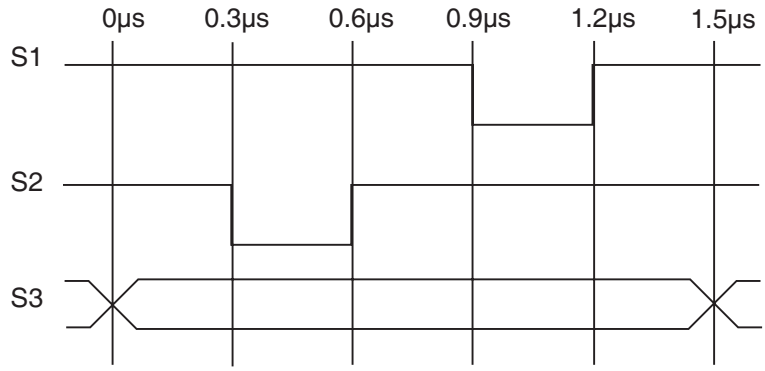
Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Input $\overline{CS}1$	V_{IN}	V_{SS}	V
Input CS2	V_{IN}	V_{DD}	V
Inputs A0 to A16	V_{IN}	$V_{GEN(S3)}$ to $V_{GEN(S19)}$ (Note 1)	V
Input $\overline{OE}$	V_{IN}	$V_{GEN(S1)}$ (Note 2)	V
Input $\overline{WE}$	V_{IN}	$V_{GEN(S2)}$ (Note 2)	V
Inputs/Outputs I/O1, I/O3, I/O5, I/O7	V_{IN}	$V_{GEN(S20)}$ (Note 1)	V
Inputs/Outputs I/O0, I/O2, I/O4, I/O6	V_{IN}	$V_{GEN(S21)}$ (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	$f_{GEN(S3)}$	330 ±20% (Note 4)	kHz
Positive Supply Voltage	V_{DD}	5(+0.5-0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1.

$$f_{GEN(Sn)} = \frac{1}{2} f_{GEN(Sn-1)} \text{ for } n \geq 3$$

2. Input waveforms to indicate required timing and phase relationships:



3. Input Protection Resistor = Output Load = 1kΩ.
4. Duty Cycle = 50 ± 15%, $t_r = t_f \leq 100$ns.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.