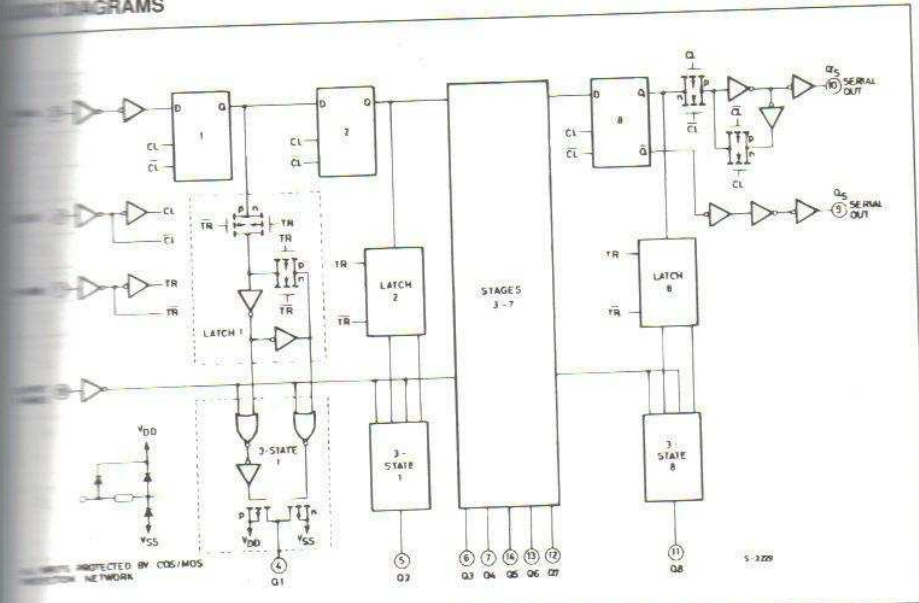


LOGIC DIAGRAMS



TIMING DIAGRAM

