FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL TEST TABLE

PATTERN No.	PIN NUMBERS														D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11 (NOTE 3)	12	13	14	15	8	16
1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	V_{DD}
2	0	0	0	0	0	0	0	0	1	0	0	0	0	0		
3	0	0	0	0	0	0	0	1	0	1	0	0	0	0		
4	0	0	0	0	0	0	0			0	1	0	0	0		
5	0	0	0	0	0	0	0			0	0	0	0	0		
6	0	0	0	0	0	0	0			5461	0	0	0	0		
7	0	1	0	0	1	1	0			0	0	1	0	0		
8	0	1	0	0	1	1	0			5461	0	1	0	0		
9	1	0	1	1	0	0	1			0	0	0	1	1		
10	1	0	1	1	0	0	1			5461	0	0	1	1		
11	1	1	1	1	1	1	1			0	0	1	1	1		
12	0	0	0	0	0	0	0			1	0	0	0	0		

NOTES

1. Figure 4(a) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.
3. From pattern 6 onwards, the figure indicated in the "Pin 11" column is the total number of $\phi 1$ pulses that must be applied to obtain the indicated output conditions.

FIGURE 4(b) - QUIESCENT CURRENT TEST TABLE

PATTERN No.	PIN NUMBERS														I_{DD} TEST	D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11 (NOTE 3)	12	13	14	15		8	16
1	0	0	0	0	0	0	0	0	1	0	1	0	0	0		0	V_{DD}
2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1		
3	0	0	0	0	0	0	0	1	0	5461	0	0	0	0			
4	1	0	1	0	1	1	0			0	0	1	0	0	2		
5	0	1	0	0	1	1	0			5461	0	1	0	0			
6	0	1	0	1	0	0	1			0	0	0	1	1	3		
7	1	0	1	1	0	0	1			5461	0	0	1	1			
8	1	1	1	1	1	1	1			0	0	1	1	1	4		
9	0	0	0	0	0	0	0			0	0	0	0	0	5		

NOTES

1. Figure 4(b) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.
3. The figure indicated in the "Pin 11" column is the total number of $\phi 1$ pulses that must be applied to obtain the indicated output conditions.