FIGURE 3(a) - PIN ASSIGNMENT (CONT'D)

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	4	5	6	7	9	10	12	14	15	16	17	19	20

FIGURE 3(b) - MODE SELECT TABLE

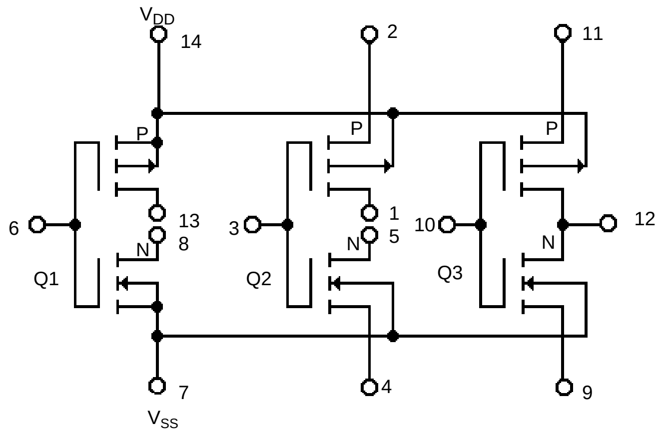
PATTERN NO.	MODE	PIN CONNECTIONS
1	Triple Inverters	14 to 2 to 11; 8 to 13; 1 to 5; 4 to 7 to 9; Positive Logic $Y=\overline{A}$
2	3-Input NOR Gate	13 to 2; 1 to11; 12 to 5 to 8; 7 to 4 to 9; Positive Logic $Y=\overline{A+B+C}$
3	3-Input NAND Gate	1 to 2 to 13; 2 to 14 to11; 4 to 8; 5 to 9; Positive Logic $Y=\overline{ABC}$
4	High Sink-Current Driver	6 to 3 to 10; 8 to 5 to 12; 11 to 14; 7 to 4 to 9
5	High Source-Current Driver	6 to 3 to 10; 13 to 1 to 12; 14 to 2 to 11; 7 to 9
6	High Sink and Source-Current Driver	6 to 3 to 10; 14 to 2 to 11; 7 to 4 to 9; 13 to 8 to 1 to 5 to 12
7	Dual bi-directional Transmission Gating	1 to 5 to 12; 2 to 9; 11 to 14; 8 to 13 to 10; 6 to3

Symbols	Dimensions mm		Notes
	Min	Max	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 12 spaces for flat, dual-in-line and small outline packages.
   16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM



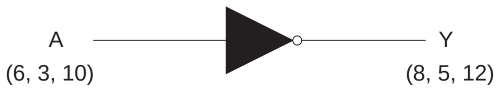
Pin No.	Symbol	Description	Pin No.	Symbol	Discription
1	Q2PS	Q2(P) SOURCE	8	Q1ND	Q1(N) DRAIN
2	Q2PD	Q2(P) DRAIN	9	Q3NS	Q3(N) SOURCE
3	Q2G	Q2 GATES	10	Q3G	Q3 GATES
4	Q2NS	Q2(N) SOURCE	11	Q3PD	Q3(P) DRAIN
5	Q2ND	Q2(N) DRAIN	12	Q3ND/ Q3PS	Q3(N) DRAIN, Q3(P) SOURCE
6	Q1G	Q1 GATES	13	Q1PS	Q1(P) SOURCE
7	V_{SS}	V_{SS}, Q1-Q2-Q3(N) SUBSTRATES, Q1(N) SOURCE	14	V_{DD}	V_{DD}, Q1-Q2-Q3(P) SUBSTRATES, Q1(P) DRAIN

NOTES:

1. Pin numbers relate to FP, DIP and SO packages only
2. For the purpose of testing in accordance with this specification, unless otherwise specified, the component pins shall be connected as follows to configure the component to function as a Triple Inverter (Positive Logic $Y = \overline{A}$) :

V_{DD} = Q2PD = Q3PD (Pin 14 to 2 to 11)
V_{SS} = Q2NS = Q3NS (Pin 7 to 4 to 9)
Q1ND = Q1PS (Pin 8 to 13)
Q2ND = Q2PS (Pin 5 to 1)

EACH INVERTER



1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	Q2PS Output (2Y)	-	11	Q3PD	-
2	Q2PD	Q2PS Output (2Y)	12	Q3ND/Q3PS Output (3Y)	Q1ND Output (1Y)
3	Q2G input (2A)	-	13	Q1PS Output (1Y)	-
4	Q2NS	Q2PD	14	V_{DD}	Q3NS
5	Q2ND Output (2Y)	Q2G input (2A)	15	-	Q3G Input (3A)
6	Q1G Input (1A)	Q2NS	16	-	Q3PD
7	V_{SS}	Q2ND Output (2Y)	17	-	Q3ND/Q3PS Output (3Y)
8	Q1ND Output (1Y)	-	18	-	-
9	Q3NS	Q1G Input (1A)	19	-	Q1PS Output (1Y)
10	Q3G Input (3A)	V_{SS}	20	-	V_{DD}

NOTES:

1. The definition of Input and Output pins is based on configuration of the component to function as a Triple Inverter.

1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level.
2. Positive Logic: $Y = \overline{A}$.
3. The truth table is based on configuration of the component to function as a Triple Inverter.

EACH GATE

INPUT (A)	OUTPUT (Y)
QnG	QnND/QnPS
L	H
H	L

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Threshold Voltage N-Channel	V_{THN}	-	Q3G at Ground Q2NS and Q3NS Connected to V_{SS} All Other Inputs: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA T_{amb}=+125°C T_{amb}=- 55°C	-0.3 -0.7	-3.5 -3.5	V
Threshold Voltage P-Channel	V_{THP}	-	Q3G at Ground Q2PS and Q3PS Connected to V_{DD} All Other Inputs: V_{IN}=-5V V_{SS}=-5V, I_{DD}=10µA T_{amb}=+125°C T_{amb}=- 55°C	0.3 0.7	3.5 3.5	V

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all tests shall be performed with the component configured to function as a Triple Inverter. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD}$ -0.5V, $V_{OL} \leq$ 0.5V. The Maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions:
   (a) All Inputs Q1G = Q2G = Q3G = V_{IH}.
   (b) All Inputs Q1G = Q2G = Q3G = V_{IL}.

4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:-